

MATHEMATICAL SYNTHESIS AND DESIGN OF THIRD
ORDER CHEBYSHEV COMBLINE BAND-PASS
FILTERS WITH TUNABLE TOPOLOGY

by
Tanner Lucas

© Copyright by Tanner Lucas, 2020

All Rights Reserved

A thesis submitted to the Faculty and the Board of Trustees of the Colorado School of Mines in partial fulfillment of the requirements for the degree of Master of Science (Electrical Engineering).

Golden, Colorado

Date _____

Signed: _____

Tanner Lucas

Signed: _____

Dr. Payam Nayeri
Thesis Advisor

Golden, Colorado

Date _____

Signed: _____

Dr. Peter Aaen
Professor and Head
Department of Electrical Engineering

ABSTRACT

A third order Chebychev combline band-pass filter topology is presented along with explicit design equations and circuit transformations for n-th order combline filter designs. The presented design operates at a center frequency of 2.45GHz and is easily tuned to center frequencies within ten percent of the filter's bandwidth. The presented design is the foundation for implementing a digitally tunable combline filter.

TABLE OF CONTENTS

ABSTRACT	iii
LIST OF FIGURES	vii
LIST OF TABLES	ix
LIST OF SYMBOLS	x
LIST OF ABBREVIATIONS	xi
ACKNOWLEDGMENTS	xii
CHAPTER 1 INTRODUCTION	1
1.1 Overview of Cognitive Radio	1
1.2 Motivation	1
1.3 Design Specifications	2
1.4 Design Applications	3
CHAPTER 2 FILTER THEORY	4
2.1 Common Microwave Filters	4
2.2 The Scattering Matrix	4
2.3 The Transmission (ABCD) Matrix	6
2.4 Chebyshev Coefficients	8
2.5 Low-Pass Filter Prototype	9
2.6 Band-Pass Filter Prototype	10
CHAPTER 3 COMBLINE FILTER MODEL	16
3.1 Coupled Microstrip Lines Equivalent Circuit Approximation	16

3.2	Microstrip Coupled Lines Approximation	17
3.3	LPF with Admittance Inverters	20
3.4	BPF with Admittance Inverters	22
3.5	Parallel LC Resonator Approximation	24
3.6	Realizing Admittance Inverters	26
3.7	Scaling Impedances with Physical Implementation in Mind	28
3.8	System Impedance Approximations	31
CHAPTER 4 PHYSICAL REALIZATION		34
4.1	Iteratively Solving for Coupled Microstrip Line Dimensions	34
4.2	Preliminary Design in ADS	35
4.3	Tuning Preliminary Design in ADS	36
4.4	Tuning Practical Layout in ADS	37
4.5	Optimizing Practical Layout in ADS	39
CHAPTER 5 EM CO-SIMULATION AND FURTHER OPTIMIZATIONS		40
5.1	Optimizing with Co-Simulation	40
5.2	Defining Operating Ranges	42
5.3	Maximum Operating Frequency	42
5.4	Minimum Operating Frequency	43
CHAPTER 6 MICROSTRIP FILTER PROTOTYPE		45
6.1	Board Layout	45
6.2	Confidence	47
6.3	Expected Results	47
CHAPTER 7 FUTURE WORK		49

7.1	Analog Tunable Capacitors	49
7.2	Digitally Tunable Varactor Diodes	49
7.3	Testing Fabricated Designs	50
7.4	Simple Cognitive Radio Application	51
CHAPTER 8 CONCLUSIONS		52
REFERENCES CITED		54
APPENDIX MATHEMATICAL SYNTHESIS CODE LISTING		56

LIST OF FIGURES

Figure 1.1	Basic Hardware Architecture of an SDR	2
Figure 2.1	A Two-Port Network Characterized with ABCD Parameters	7
Figure 2.2	Cascading Connection of a Two-Port Network	7
Figure 2.3	Third Order Chebyshev LPF with Unity Characteristic Impedance	9
Figure 2.4	Third Order Chebyshev LPF Results	10
Figure 2.5	Third Order Chebyshev LPF Circuit Schematic	11
Figure 2.6	Third Order Chebyshev BPF with Unity Characteristic Impedance	12
Figure 2.7	Reflections at Port One and Forward Transmission of the Third Order Chebyshev BPF Lumped Element Prototype	14
Figure 2.8	Circuit Schematic of the Third Order Chebyshev BPF Lumped Element Prototype	15
Figure 3.1	Comblin Filter Goal Topology	16
Figure 3.2	Four-Port Microstrip Coupled Line Circuit	17
Figure 3.3	Four-Port Microstrip Coupled Line Equivalent Circuit	18
Figure 3.4	Two-Port Microstrip Coupled Line Circuit	18
Figure 3.5	Two-Port Microstrip Coupled Line Equivalent Circuit	19
Figure 3.6	Two-Port Microstrip Coupled Line Reduced Equivalent Circuit	19
Figure 3.7	Two-Port Microstrip Coupled Line Final Reduced Equivalent Circuit.	20
Figure 3.8	Series Inductor Two-Port Network	21
Figure 3.9	Series Inductor Two-Port Equivalent Circuit	21
Figure 3.10	Third Order Chebyshev LPF with Inverters	22

Figure 3.11	Third Order Chebyshev BPF with Inverters ($\omega_0 = 1$ rad/sec, $Z_0 = 1\Omega$) . . .	23
Figure 3.12	Parallel LC Resonator Approximation	24
Figure 3.13	Admittance Inverter Circuit Model	27
Figure 3.14	Admittance Inverter Realization with Transmission Line Lengths	27
Figure 3.15	Parallel Coupled Line BPF Circuit Model Approximation.	28
Figure 3.16	The Capacitor Network Used to Realize the Real Impedance Matching Inverter	31
Figure 4.1	The Preliminary Schematic Implemented from the Mathematical Synthesis	35
Figure 4.2	Reflections and Transmission Properties of the Preliminary Ideal Microstrip Design	36
Figure 4.3	Reflections and Transmission Properties of the Tuned Preliminary Ideal Microstrip Design	37
Figure 4.4	Reflections and Transmission Properties of the Tuned Ideal Microstrip Design with a Practical Layout	38
Figure 4.5	Reflections and Transmission Properties of the Optimized Ideal Microstrip Design with a Practical Layout	39
Figure 5.1	Reflections and Transmission Properties of the Optimized Microstrip Design from Full EM Simulation	41
Figure 5.2	Higher Frequency Reflections and Transmission Properties of the Optimized Microstrip Design from Full EM Simulation	43
Figure 5.3	Lower Frequency Reflections and Transmission Properties of the Optimized Microstrip Design from Full EM Simulation	44
Figure 6.1	Top View of Third Order Chebyshev BPF Microstrip Realization	46
Figure 6.2	View of Third Order Chebyshev BPF Microstrip Realization on Rogers 5880 Laminate	46
Figure 6.3	Reflections and Transmission Properties of the Optimized Microstrip Design with Available Surface-Mount Capacitors	48

LIST OF TABLES

Table 2.1	Chebyshev Coefficients Used for Third Order Filter ($\omega_0 = 1\text{rad/sec}$)	8
Table 2.2	Lumped Element Values Used for Third Order Chebyshev Low-Pass Filter ($\omega_0 = 1\text{ rad/sec}$)	9
Table 2.3	Lumped Element Values Used for Third Order Chebyshev Band-Pass Filter ($f_0 = 2.447\text{GHz}$)	14
Table 3.1	Lumped Element Values Used for Third Order Chebyshev Band-Pass Filter Prototype with Inverters ($f_0 = 2.447\text{ GHz}$, $Z_0 = 50\Omega$)	23
Table 3.2	Open-Circuited Transmission Line and Parallel Capacitor Values Used for Third Order Chebyshev Band-Pass Filter Prototype with Inverters ($f_0 = 2.447\text{ GHz}$, $Z_0 = 50\Omega$).	26
Table 3.3	Short-Circuited Transmission Line Stubs and Parallel Capacitor Values Used for Third Order Chebychev Band-Pass Filter Circuit Model Approximation ($f_0 = 2.447\text{ GHz}$, $Z_0 = 50\Omega$).	29
Table 3.4	Scaled Impedance Values for the Third Order Chebychev Band-Pass Filter Circuit Model Approximation ($f_0 = 2.447\text{ GHz}$, $Z_0 = 50\Omega$).	30
Table 3.5	Mathematical Synthesis Final Iteration Values for Circuit Model Approximation ($f_0 = 2.447\text{ GHz}$, $Z_0 = 50\Omega$).	31
Table 3.6	System Impedance Approximations for the Third Order Chebychev Band-Pass Filter Circuit Model Approximation ($f_0 = 2.447\text{ GHz}$, $Z_0 = 50\Omega$).	32

LIST OF SYMBOLS

center frequency	ω_0
commensurate frequency	ω_r
ripple factor	γ
decibels	dB
reflection coefficient	Γ
characteristic impedance	Z_0
input impedance	Z_{in}
wavelength	λ
system impedance	Z_{0S}
even-mode system impedance	Z_{0e}
odd-mode system impedance	Z_{0o}

LIST OF ABBREVIATIONS

Radio Frequency	RF
Bit Error Rate	BER
Digital Signal Processing	DSP
General-Purpose Processor	GPP
Field-Programmable Gate Array	FPGA
Software Defined Radio	SDR
Low-Pass Filter	LPF
High-Pass Filter	HPF
Band-Pass Filter	BPF
Pass-Band Ripple	PBR
Keysight Advanced Design System	ADS
Electromagnetic	EM
Surface-Mounted Device	SMD
Direct Current	DC
Vector Network Analyser	VNA

ACKNOWLEDGMENTS

I would like to thank Dr. Payam Nayeri of the Electrical Engineering department at the Colorado School of Mines. As my thesis advisor, he always supported me and my research while challenging me to greater heights.

Additionally, I would like to give a special thanks to Dr. Randy Haupt and Dr. Christopher Coulston of the Electrical Engineering department at the Colorado School of Mines. Thank you for serving as my committee members and taking the time to provide helpful feedback whenever needed.

Furthermore, thank you friends and family for your continual support through this challenging research process.

CHAPTER 1

INTRODUCTION

1.1 Overview of Cognitive Radio

Cognitive radio exists to enable devices to operate more efficiently within their respective local networks. For example, a user would like to receive important data over a congested wireless network as fast as possible with a BER. With the heavy congestion on the network, the user risks receiving corrupt data and has no way of rectifying the issue themselves. Cognitive radio solves this problem, without any user interaction, by identifying and using the frequencies and waveforms that avoid and minimize interference from other communication systems [1]. While not explicitly necessary, SDRs are the most common platforms to efficiently implement cognitive radio capabilities [1–3]. With the advancement in technology, it is common for SDRs to host GPPs in addition to DSPs and FPGAs, and while the physical layer signal processing is implemented by the latter, reasoning software can be executed by the GPPs [1]. SDRs are the perfect platform to implement cognitive radio systems as they offer a full transmit and receive chain, analog to digital conversion, post processing capabilities, and user interface applications. The basic hardware architecture of an SDR is shown in Figure 1.1. Spectrum sensing through energy detection is a common implementation of cognitive radio functionality, and SDRs support this application with their ability to analyze a spectrum digitally [1, 4–6]. A spectrum can be sampled real-time and analyzed before transmit and receive chain parameters are modified for more optimized operation on the current network.

1.2 Motivation

Cognitive radio is an important technology for establishing and maintaining reliable communication links over the saturated spectrum. Cognitive radio is becoming more and more valuable as the air waves become largely congested. In general, cognitive radio aims to more

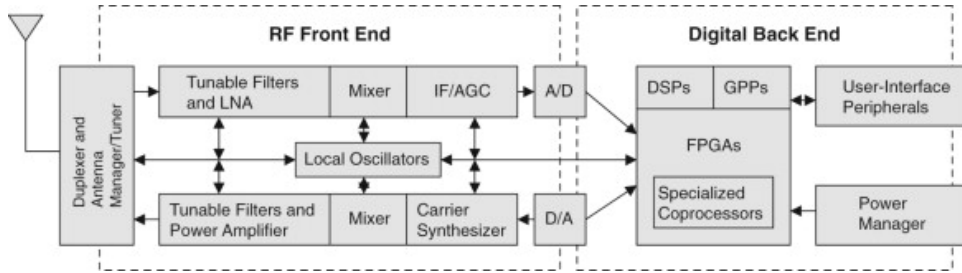


Figure 1.1: Basic Hardware Architecture of an SDR [1].

efficiently utilize available radio spectrum, in a specific area and time of day, as a regulatory framework [2]. Given the variable nature of cognitive radio operation, devices capable of tuning themselves on the fly to maintain communication links are invaluable. A cognitive radio front-end architecture is designed to sample over a wide spectrum and determine available spectrum holes for devices to operate on [6, 7]. As in traditional communication systems, filtering is an important functionality for both the receive and transmit chain. As such, a digitally tunable filter is valuable for cognitive radio receive and transmit chains.

1.3 Design Specifications

The device presented in this paper is a third order Chebyshev combline BPF implemented with microstrip topology. This topology is recognized for its tunability, and it is an ideal choice for higher power cognitive radio applications [8–10]. Since the device is meant to have a Chebyshev response, the filter specifications will be catered to using the Chebyshev polynomials. The center frequency of the filter is 2.45GHz, the operational bandwidth is ten percent, and the pass-band ripple factor is 0.1. Since a Chebyshev response is used, steep skirts in the pass-band are expected. Furthermore, there are expected to be three poles in the pass-band response of the filter [11]. The filter is designed on a Rogers 5880 laminate [12].

1.4 Design Applications

This design is particularly interesting for communication systems due to the nature of its tunable topology. This is especially true for a communication system supporting multiple operating frequencies with a set bandwidth.

Given a scenario where a service provider is attempting to provide coverage to as many users across as many platforms as possible, tunable filtering is extremely useful and cost efficient. For example, a cellular carrier is deploying phased arrays in their infrastructure to react to the needs of their customers. Over the course of a day, signal traffic on the spectrum varies widely. In order to provide the best coverage to the most consumers within a range, tunable filters could be rapidly switched along with the phased arrays' main beams to support multiple cellular protocols across a larger operating spectrum. In order to achieve such a feat statically, an order of magnitude more of antennas and filters would have to be designed and configured in any number of combinations to achieve the same functionality. Such a static implementation is impractical as the hardware overhead is much too high, but cognitive radio, steerable antenna arrays, and tunable filter technology make the additional overhead disappear.

CHAPTER 2

FILTER THEORY

2.1 Common Microwave Filters

A microwave filter is characterized as a two-port network supporting signal transmission in the pass-band of the the filter while attenuating the stop-band. Low-pass, high-pass, and band-pass responses are typical frequency responses desired for communication systems and RF applications.

Low-pass filters (LPF), high-pass filters (HPF), and band-pass filters (BPF), are important in any communication system device chain. LPF's block signals at high frequencies while HPF's block signals at low frequencies. BPF's leverage a combination of LPF and HPF design to deploy a pass-band or stop-band with desired bandwidth, insertion loss, and skirt steepness. There are multiple classic filter responses that are used to design LPF's, HPF's, and BPF's. A few classic filter responses include Butterworth and Chebyshev responses [11]. This paper presents a practical BPF design with a Chebyshev response.

2.2 The Scattering Matrix

In order to quantify the behavior of a passive device, scattering parameters are leveraged. The scattering matrix gives a complete description of the device network as seen at the device's N ports [11]. Scattering parameters are a metric of the ratio of the voltage waves reflected from the ports to the voltage waves incident to the ports. For example, S_{11} is the ratio of the reflected signal voltage at port one to the incident signal voltage at port one. This metric indicates the amount of power transmitted, through port one from port one, at the frequencies of interest [11].

The scattering matrix for a general N -port network is defined in Equation 2.1, and it is generalized in Equation 2.2 [11].

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & \ddots & & \vdots \\ \vdots & & \ddots & \vdots \\ S_{N1} & \dots & \dots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix} \quad (2.1)$$

$$[V^-] = [S] [V^+] \quad (2.2)$$

To calculate a specific element of the scattering matrix, Equation 2.3 is used [11].

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+ = 0 \text{ for } k \neq j} \quad (2.3)$$

By driving port j with an incident voltage wave and measuring the reflected voltage wave amplitude at port i , S_{ij} can be calculated. To achieve this, all incident waves on the other ports are set to zero by terminating them with matched loads. Therefore, S_{ii} is equivalent to the reflection coefficient (Γ_i) looking into port i when the remaining ports incident voltages are set to zero [11]. Since S_{ii} is the reflection coefficient looking into the i -th port, S_{ij} is the transmission coefficient from the j -th port to the i -th port when all other ports are terminated with matched loads. Furthermore, the power incident to the i -th port and power transmitted away from the i -th port are shown in Equation 2.4 [11, 13].

$$P_i^\pm = \frac{1}{2} \left| \frac{V_i^\pm}{Z_o} \right|^2 \quad (2.4)$$

Conveniently, since scattering parameters are defined as the ratio of voltage waves incident to a given port and voltage waves reflected from a given port, the reflection coefficient seen at each port can be determined. This relationship holds for the i -th port so long as every other port is terminated with a matched load [11]. Furthermore, the reflection coefficient seen at a port can be expressed in terms of the input impedance (Z_{in}) at that port and the characteristic impedance, and this relationship is shown in Equation 2.5 [11, 13].

$$S_{ii} = \left. \frac{V_i^-}{V_i^+} \right|_{V_k^+ = 0, k \neq i} = \Gamma_i \Big|_{V_k^+ = 0, k \neq i} = \left. \frac{Z_{in,i} - Z_o}{Z_{in,i} + Z_o} \right|_{Z_o \text{ on port } k} \quad (2.5)$$

While designing an RF filter, scattering parameters are a very direct way to quantify the filter's performance at the desired operating frequencies. The corresponding scattering matrix, for a two-port RF filter network, is shown in Equation 2.6.

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \quad (2.6)$$

During the design process of any RF filter network, S_{11} and S_{21} are the best indicators of the filter's performance. Specifically, S_{11} is desired to be low across the operating bandwidth which indicates low reflection looking into port one with a matched load at port two. Additionally, S_{21} displays the transmission of power from port one to port two, and it is desired to be very close to 0 **dB** which indicates low power loss across the desired frequency band. The scattering parameters are the primary indicator to determine if the RF filter was designed to the desired specifications. For example, the pass-band ripple (PBR) can be verified from the power transmitted through port two from port one. Another useful tool for designing RF filters is the transmission matrix.

2.3 The Transmission (ABCD) Matrix

The transmission matrix is defined as a 2×2 matrix which gives a direct linear transformation between the voltage and current values at port one and the voltage and current values at port two. The transmission matrix is also known as an ABCD matrix, and these ABCD parameters are very useful for designing two-port systems. This is especially true since multiple two-port networks can be cascaded together yielding a system equivalent transmission matrix. Cascading multiple linear two-port devices can be characterized as the product of the devices' transmission matrices.

Using Figure 2.1 as a reference, the voltage and current at port one are related to the voltage and current at port two with Equation 2.7 [11].

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (2.7)$$

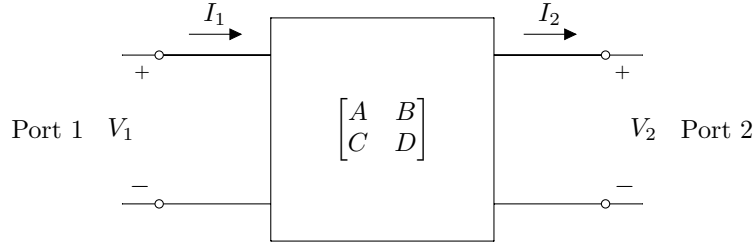


Figure 2.1: A Two-Port Network Characterized with ABCD Parameters [11]

To reiterate, since passive RF devices behave linearly, multiple transmission matrices can be cascaded to outline the behavior of the devices. An example of a cascade connection of a two port network is shown in Figure 2.2, and the corresponding cascaded transmission matrices are shown in Equation 2.8 [11].

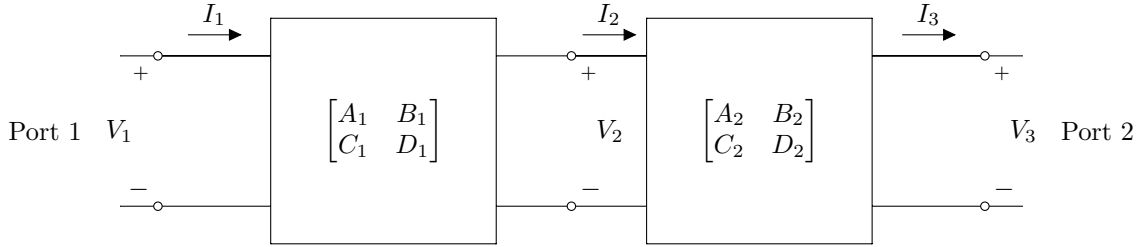


Figure 2.2: Cascading Connection of a Two-Port Network [11]

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (2.8)$$

The transmission matrix is an important tool for passive RF device design, and it is leveraged during the mathematical synthesis of a pair of grounded coupled microstrip lines. In order to leverage the scattering and transmission matrices, it is good practice to design an ideal lumped element circuit model with the desired response. The desired response for the device presented is a Chebyshev response, and in order to design a lumped element Chebyshev prototype, the n Chebyshev coefficients must be known, corresponding to the order of the filter.

2.4 Chebyshev Coefficients

The filter presented in this paper is designed with a classic Chebyshev response. This filter response is popular for BPF design due to the steep pass-band skirts, selected bandwidth, and specified insertion loss. This allows the designer to ensure specifications are met during the filter design process. The Chebyshev coefficients are calculated for a filter with a ripple factor (γ) of 0.1. Given a specified ripple factor, Equation 2.9 can be used to determine the PBR. The PBR, in decibels, is calculated using Equation 2.10, and the PBR is 0.04321 **dB** for a ripple factor of 0.1.

$$PBR = (1 + \gamma^2) \quad (2.9)$$

$$PBR_{dB} = 10 \log_{10}(PBR) \quad (2.10)$$

With a defined ripple factor and PBR, the Chebyshev polynomials can be used to generate the Chebyshev coefficients for an n -th order filter [14]. The calculated Chebyshev coefficients for a third order device with a ripple factor of 0.1 are shown in Table 2.1. These coefficients

Table 2.1: Chebyshev Coefficients Used for Third Order Filter ($\omega_0 = 1 \text{ rad/sec}$)

Coefficients	Values	Ripple Factor (γ)
g_0	1	0.1
g_1	0.85158	0.1
g_2	1.10316	0.1
g_3	0.85158	0.1
g_4	1	0.1

correspond to the lumped element impedances of a third order LPF, and they generate the desired Chebyshev response at center frequency of 1 *rad/sec*. These coefficients serve as the foundation of the third order combline BPF presented.

2.5 Low-Pass Filter Prototype

The device presented is a third order BPF with Chebyshev response, however the best starting point for the circuit model is a third order LPF with Chebyshev response. Once the lumped element LPF is modeled, the circuit can be easily transformed to a lumped element BPF circuit. From Table 2.1, a lumped element third order LPF circuit prototype can be created, where each port is terminated with unity characteristic impedance. The described lumped element LPF circuit is shown in Figure 2.3. The values assigned to each lumped

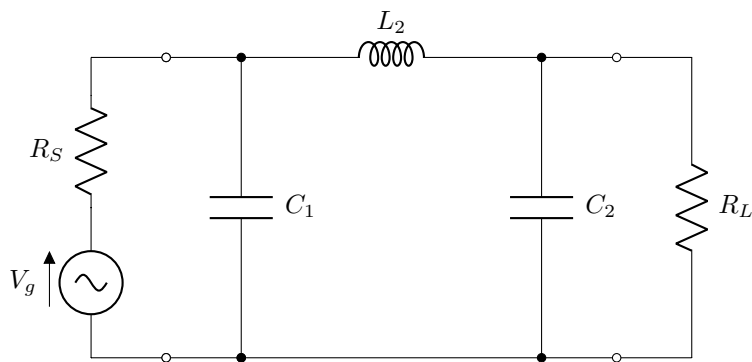


Figure 2.3: Third Order Chebyshev LPF with Unity Characteristic Impedance

element in Figure 2.3 are shown in Table 2.2.

Table 2.2: Lumped Element Values Used for Third Order Chebyshev Low-Pass Filter ($\omega_0 = 1$ rad/sec)

Coefficients	Element	Value	Unit
g_0	R_S	1	Ohms (Ω)
g_1	C_1	0.85158	Farads (F)
g_2	L_1	1.10316	Henrys (H)
g_3	C_2	0.85158	Farads (F)
g_4	R_L	1	Ohms (Ω)

To verify the circuit, ADS was used to model the LPF [15]. The simulation results are shown in Figure 2.4, and they validate the Chebyshev coefficients in Table 2.1. The

schematic created for the third order Chebyshev LPF prototype is shown in Figure 2.5.

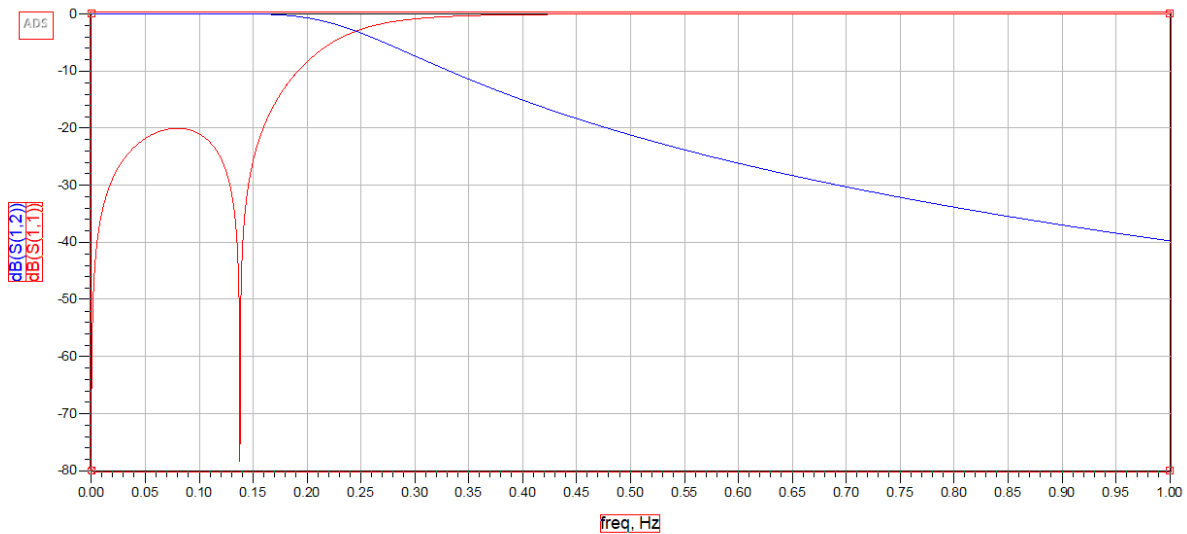


Figure 2.4: Third Order Chebyshev LPF Results

Plotting S_{11} from 0-1 rad/sec displays the desired Chebyshev response with transmission below 20 **dB** up to $\omega_0 = 1 rad/sec$. Both the transmission from port one to port two and the reflection at port one display the desired Chebyshev response. The ADS circuit schematic in Figure 2.5 is identical to the circuit in Figure 2.3 and used the Chebyshev coefficients outlined in Table 2.2. The LPF Chebyshev lumped element model is important as it is the starting point for designing a lumped element BPF with Chebyshev response at the desired operating frequency.

2.6 Band-Pass Filter Prototype

In order to achieve the desired Chebyshev response at the desired center frequency and characteristic impedance, the lumped element values in Table 2.2 must be used to calculate the lumped elements for the third order Chebyshev BPF prototype at the desired center frequency. Furthermore, once the lumped elements for the BPF prototype are calculated, they must be scaled to the desired characteristic impedance.

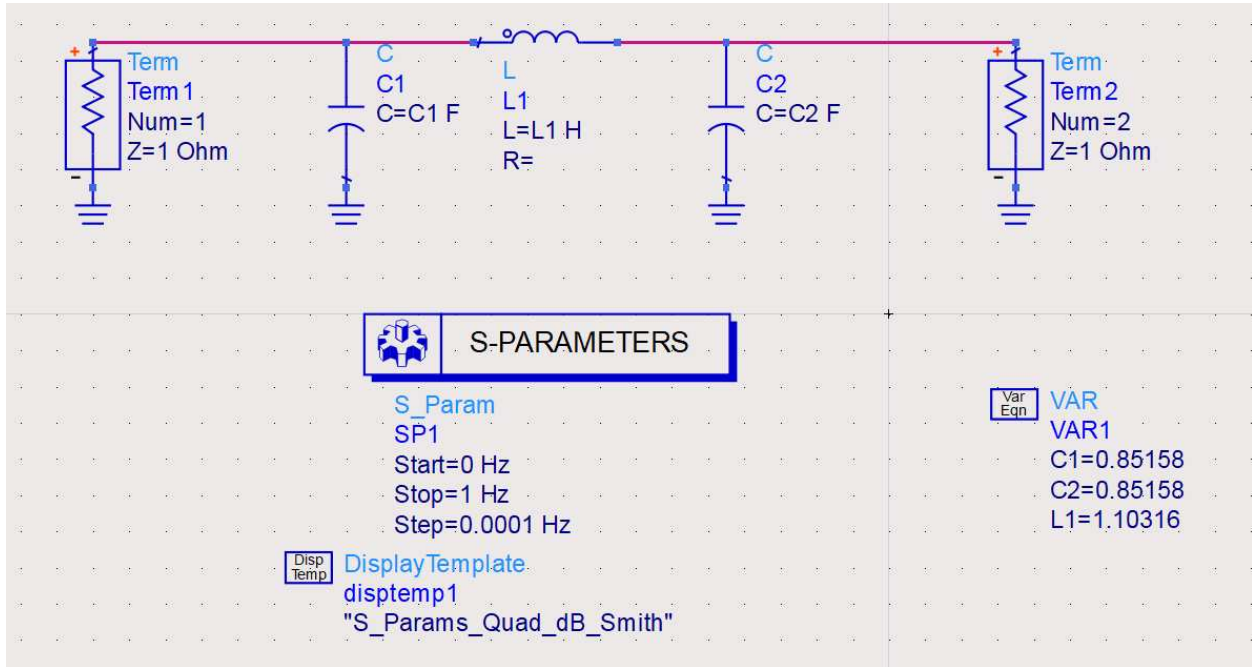


Figure 2.5: Third Order Chebyshev LPF Circuit Schematic

Since LPFs block signals operating above a cutoff frequency and HPFs block signals operating below a certain cutoff frequency, BPFs combine both filter functions and block all signals above and below a desired operating bandwidth. An LPF circuit model is shown in Figure 2.3, and in order to change the LPF into a HPF circuit model the shunt capacitors would be replaced with shunt inductors and the series inductor replaced with a series capacitor [11]. Since a BPF combines the characteristics of LPF and HPF circuit functions, the BPF circuit model used is shown in Figure 2.6. This is not the only BPF circuit configuration, but it is the starting point for the device presented in this paper.

In order to calculate the lumped elements at the desired operating frequency for the BPF lumped element Chebyshev prototype, Equations 2.11a, 2.11b, 2.11c, and 2.11d are used [11]. In Equation 2.11a, the center frequency ω_0 is calculated as the geometric mean of the upper and lower frequencies of the desired bandwidth. In this case a ten percent bandwidth is desired at an operating frequency of 2.45 GHz, so ω_1 would be 2.3275 GHz and ω_2 would be 2.5725 GHz. It is important to note that the equations are given in terms of

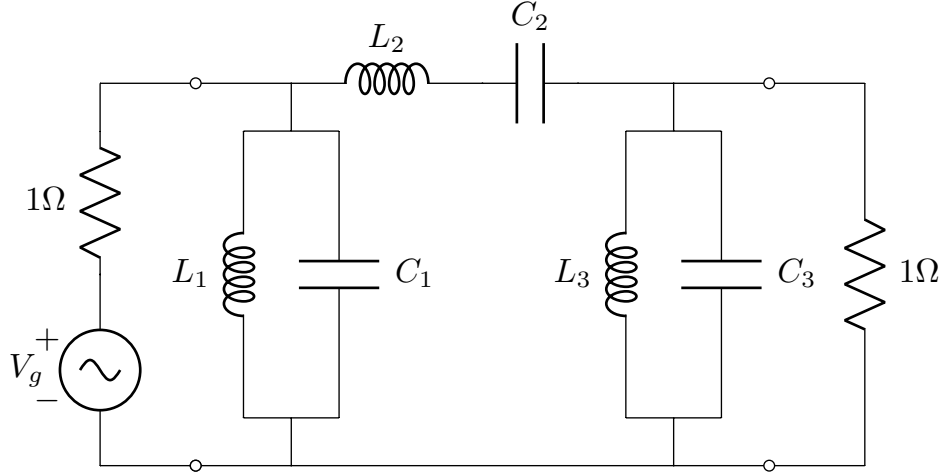


Figure 2.6: Third Order Chebyshev BPF with Unity Characteristic Impedance

angular frequency. To calculate the parallel inductor and capacitor values from the reference values in Table 2.2, a scaling factor, α , is used. The scaling factor, α , is calculated using 2.11b. To calculate the lumped element values of the parallel LC resonators in Figure 2.6, Equation 2.11c is used. Likewise, to calculate the series lumped element values, Equation 2.11d is used.

$$\omega_0 = \sqrt{\omega_1 \omega_2} \quad (2.11a)$$

$$\alpha = \frac{\omega_0}{\omega_2 - \omega_1} \quad (2.11b)$$

$$C_p = \frac{\alpha C_1}{\omega_0}, \quad L_p = \frac{1}{\alpha C_1 \omega_0} \quad (2.11c)$$

$$C_s = \frac{1}{\alpha L_2 \omega_0}, \quad L_s = \frac{\alpha L_2}{\omega_0} \quad (2.11d)$$

Additionally, the impedance must be scaled with reference to the desired characteristic impedance. The values in Table 2.2 are matched to a characteristic impedance of 1Ω , but the desired characteristic impedance is 50Ω . In order to scale the reactive lumped elements with reference to the desired characteristic impedance, Equations 2.12a, 2.12b, 2.12c and

2.12d are used [11].

$$C' = \frac{C}{R_o} \quad (2.12a)$$

$$L' = R_o L \quad (2.12b)$$

$$R'_s = R_o \quad (2.12c)$$

$$R'_L = R_o R_L \quad (2.12d)$$

The third order Chebyshev BPF prototype lumped element values are shown in Table 2.3. All of the lumped element values are scaled to the desired characteristic impedance of 50Ω using Equations 2.12a, 2.12b, 2.12c and 2.12d. The calculated lumped element values are validated in Figure 2.7. The schematic used to generate the results in Figure 2.7 is shown in Figure 2.8. The reflections at port one and the forward transmission from port one to port two are shown in Figure 2.7. The plot showing the reflections at port one has two markers at the edges of the desired bandwidth. Both of these markers show the response is below 20 dB and within the desired operating bandwidth. Additionally, there are three zeroes in the reflection plot, which is characteristic of a third order Chebyshev response. There are three poles in the forward transmission plot, but the scale of the plot makes them impossible to see. The forward transmission plot is intersected with markers at the edges of the desired bandwidth too, and the measured response is around 0.04 dB . Comparing this to the design specifications, the lumped element third order Chebyshev BPF prototype is perfect. Therefore, the lumped element values in Table 2.3 provide a valid starting point for the combline circuit model.

Table 2.3: Lumped Element Values Used for Third Order Chebyshev Band-Pass Filter ($f_0 = 2.447\text{GHz}$)

Coefficients	Element	Value	Unit
g_0	R_S	50	Ω
g_1	L_1	0.38237	nH
g_1	C_1	11.0638	pF
g_2	L_2	35.8313	nH
g_2	C_2	0.118068	pF
g_3	L_3	0.38237	nH
g_3	C_3	11.0638	pF
g_4	R_L	50	Ω

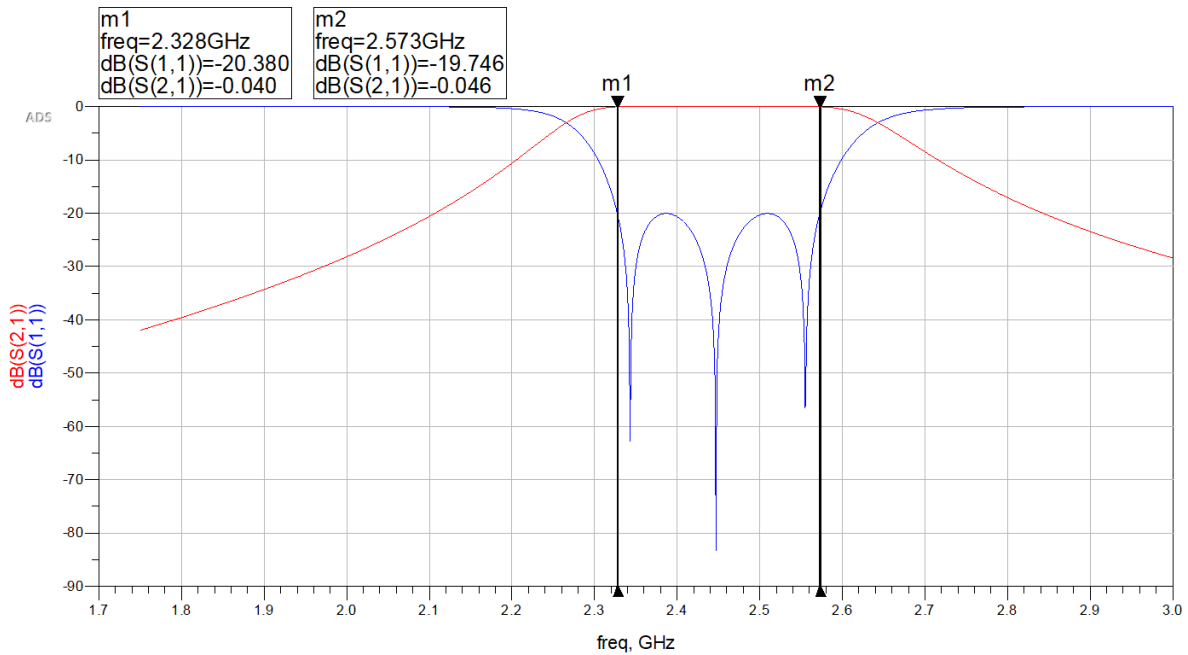


Figure 2.7: Reflections at Port One and Forward Transmission of the Third Order Chebyshev BPF Lumped Element Prototype

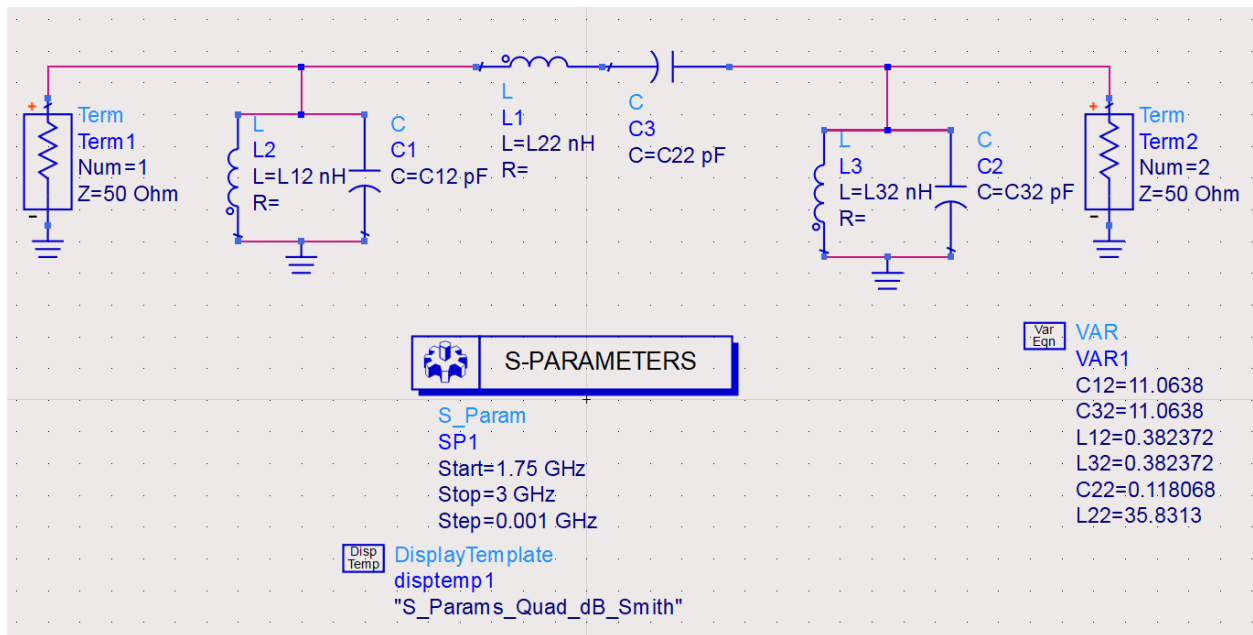


Figure 2.8: Circuit Schematic of the Third Order Chebyshev BPF Lumped Element Prototype

CHAPTER 3
COMBLINE FILTER MODEL

3.1 Coupled Microstrip Lines Equivalent Circuit Approximation

Tunable RF filters have numerous applications in many industries such as defense, aerospace, and communications, and the comblines topology is among the most popular realizations as it is easily miniaturized, cost effective, and easily implemented [8–11, 16, 17]. Microstrip technology is leveraged to implement such designs. The comblines filter topology is nontrivial to represent as lumped elements, and a mathematical synthesis procedure is presented to achieve comblines filter design parameters from a Chebyshev lumped element band-pass filter prototype. This design procedure outlines the design of a third order Chebyshev band-pass filter realized with comblines microstrip sections, and the same procedure can easily be applied to higher order filter realizations. Since the design implements a Chebyshev response, steep response skirts are expected with application specific pass-band ripple.

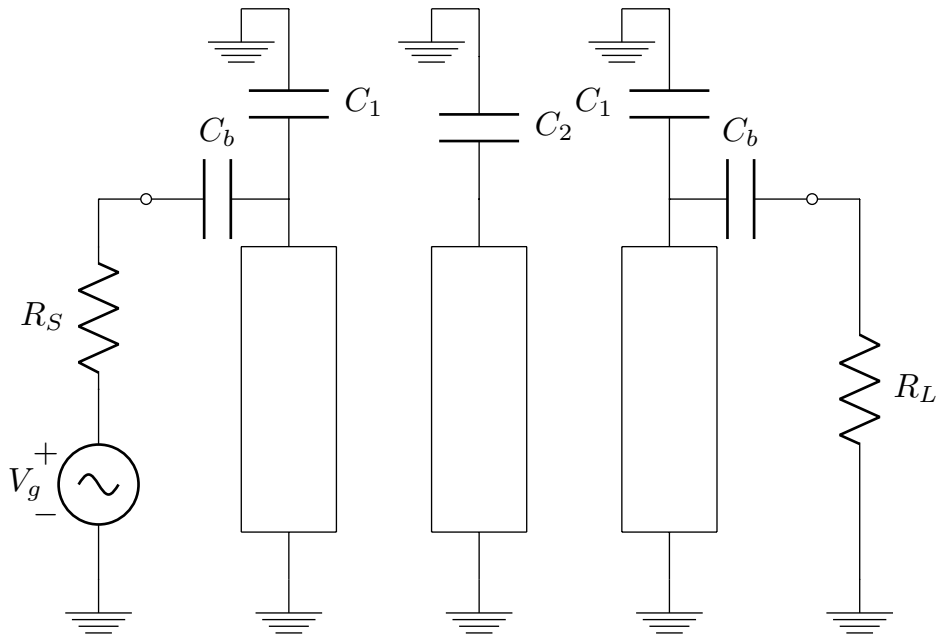


Figure 3.1: Comblines Filter Goal Topology

The topology shown in Figure 3.1 is ideal as it permits multiple degrees of freedom while tuning the device. This chapter outlines how the model in Figure 3.1 is approximated with known circuit elements. Specifically, an approximation for the coupled microstrip lines is presented along with an approximation of even and odd mode system impedances for the core of the filter. This topology is easy to fabricate as the circuit model in Figure 3.1 is made of three microstrips and is symmetric about the center combline. Additionally, the operating frequency of the third order Chebyshev BPF, in Figure 3.1, can be adjusted by varying the values of the surface mount capacitors, C_b , C_1 , and C_2 .

3.2 Microstrip Coupled Lines Approximation

In order to realize a circuit model equivalent to the topology shown in Figure 3.1, an approximate model for a pair of coupled microstrip lines must be realized. There is no direct set of equations relating lumped elements to a pair of coupled microstrip lines. Instead, a circuit model approximating the behavior of microstrip coupled lines is used. A four-port network made of two microstrip coupled lines is shown in Figure 3.2.

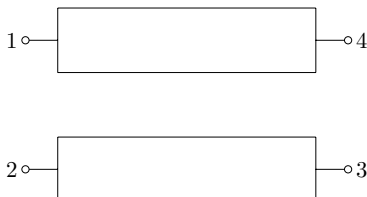


Figure 3.2: Four-Port Microstrip Coupled Line Circuit

There is an exact equivalent circuit to the pair of microstrip coupled lines from Figure 3.2, but it does not serve as an easy starting point for deriving an approximate circuit model to the topology shown in Figure 3.1 [11, 16]. Instead an approximate equivalent circuit, to the four-port microstrip coupled lines, is used as a starting point, and it is shown in Figure 3.3. The topology in Figure 3.1 is made of three combline sections grounded on one end and connected to a capacitor on the other. This configuration is realized by shorting ports three and four, in Figure 3.2, to ground. The coupled microstrip lines with ports three and four

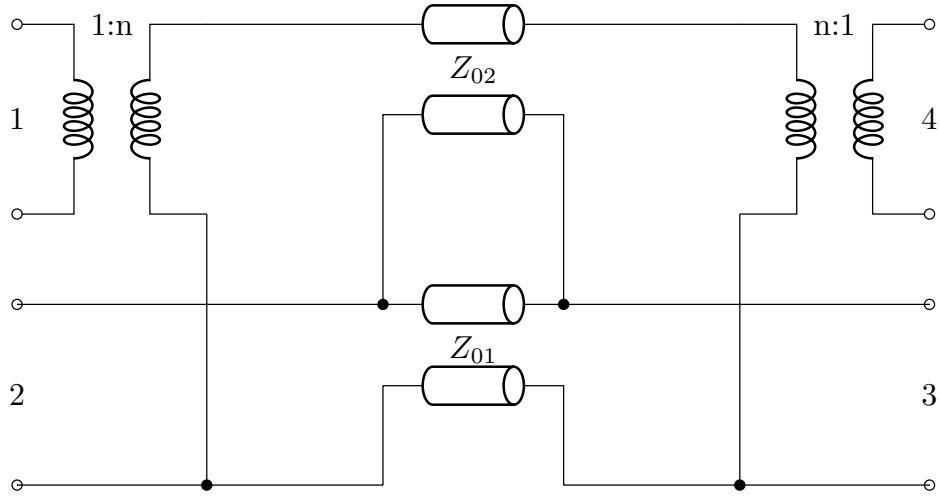


Figure 3.3: Four-Port Microstrip Coupled Line Equivalent Circuit

grounded are shown in Figure 3.4, and this configuration change turns the four-port network from Figure 3.2 into a two-port network. The equivalent circuit to the two-port network in Figure 3.4 is shown in Figure 3.5.

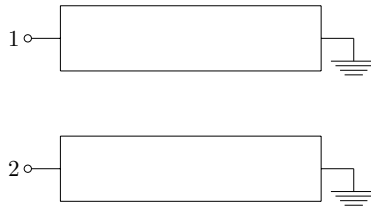


Figure 3.4: Two-Port Microstrip Coupled Line Circuit

By grounding ports three and four in Figure 3.4, the equivalent circuit in Figure 3.5 is able to be simplified. Specifically, the shorted transformer at port three, in Figure 3.3, is dropped, and the two transmission lines are realized as shunt capacitances. The reduced equivalent circuit described above is shown in Figure 3.6. The transformer at port one of Figure 3.6 is not necessary and difficult to realize and is instead replaced with another parallel shunt capacitance.

As such, the final reduced circuit model for a pair of microstrip coupled lines is shown in Figure 3.7. This is an ideal circuit model as the two parallel shunt capacitances fulfill

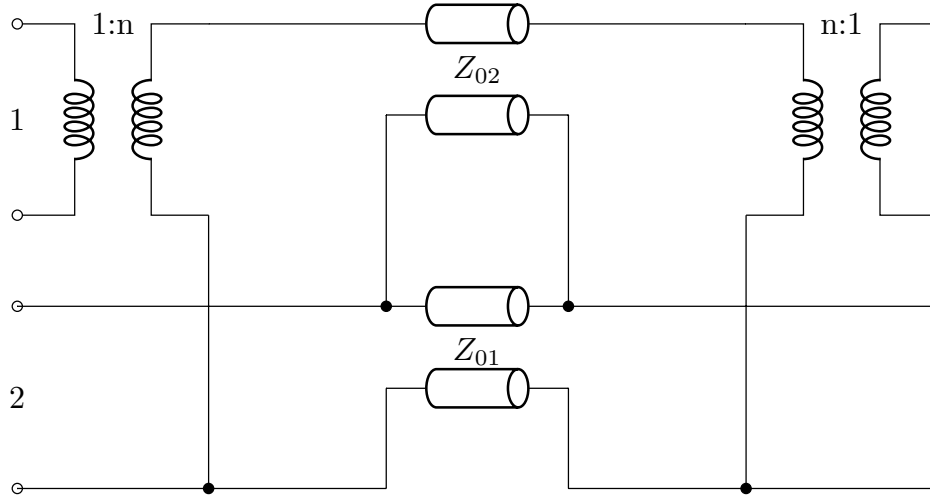


Figure 3.5: Two-Port Microstrip Coupled Line Equivalent Circuit

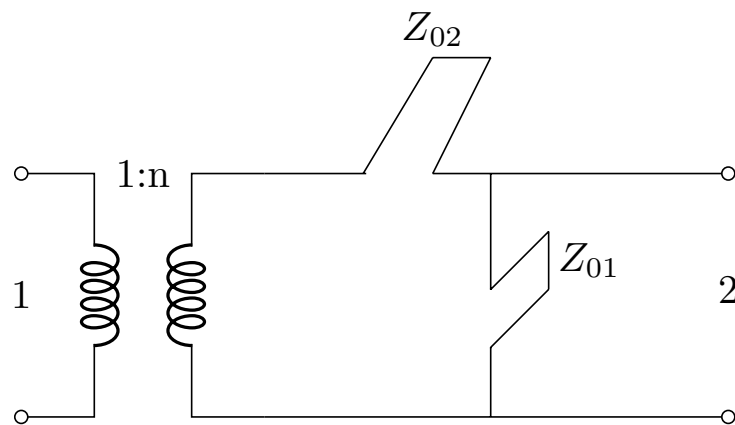


Figure 3.6: Two-Port Microstrip Coupled Line Reduced Equivalent Circuit

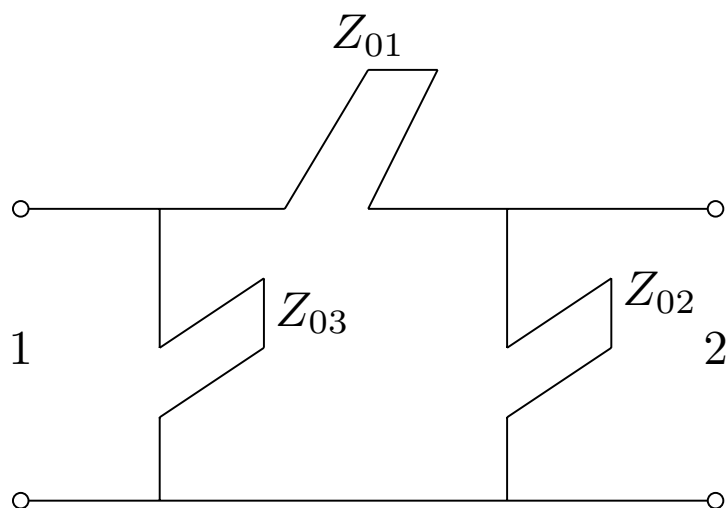


Figure 3.7: Two-Port Microstrip Coupled Line Final Reduced Equivalent Circuit.

the two microstrip lines, and the series shunt capacitance satisfies some impedance introduced from the spacing between the two coupled microstrip lines [8, 10]. Using the circuit model in Figure 3.7 as a target, the following subsections outline the circuit transformations used to realize a third order Chebyshev BPF approximation constructed with a series of pi configurations of shunt capacitances.

3.3 LPF with Admittance Inverters

Chapter two outlines the ideal third order Chebyshev BPF using lumped element capacitors and inductors. In RF applications, surface mount capacitors are not too lossy and provide good performance. However, the same is not true for inductors. Surface-mount inductors are very lossy at higher frequencies when physically realized, and it is desired to implement the needed inductance with alternative methods. Specifically, the series inductor from the third order LPF prototype can be represented as a series of impedance inverters, capacitors, and transformers. This equivalent circuit is verified using the ABCD parameters of each section cascaded together. The two-port series inductor network is shown in Figure 3.8.

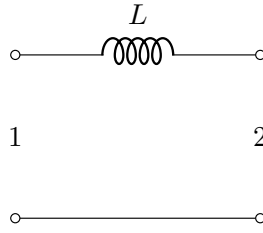


Figure 3.8: Series Inductor Two-Port Network

Using ABCD parameters of simple two-port networks, the equivalent two-port network to the series inductor network, shown in Figure 3.8, is shown in Figure 3.9 [11]. The two-port network shown in Figure 3.9 consists of two impedance inverters, a capacitor in parallel, and a phase shifting transformer. As mentioned previously, cascading the ABCD parameters of each of these components, in the order presented in Figure 3.9, yields the equivalent ABCD parameters of the series inductor network of Figure 3.8.

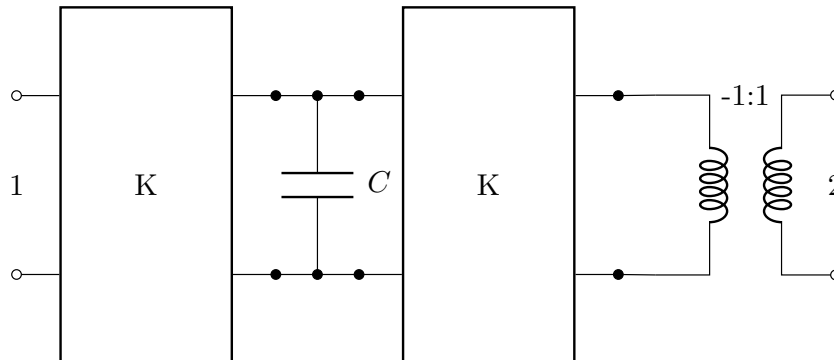


Figure 3.9: Series Inductor Two-Port Equivalent Circuit

The cascaded ABCD parameters equating the networks in Figure 3.8 and Figure 3.9 are shown in Equation 3.1a [11]. This list of linear transformations equate the series inductor to the parallel capacitor and impedance inverter values with Equation 3.1b. In order to solve for the parallel capacitance in Figure 3.9, the impedance inverter values are set to 50Ω to match the characteristic impedance of the input and output transmission lines. The equivalent third order Chebyshev LPF prototype with impedance inverters, matched to unity

characteristic impedance, is shown in Figure 3.10.

$$\begin{bmatrix} 1 & sL \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 0 & jK \\ j/K & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC & 0 \end{bmatrix} \begin{bmatrix} 0 & jK \\ j/K & 0 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} = \begin{bmatrix} 1 & sCK^2 \\ 0 & 1 \end{bmatrix} \quad (3.1a)$$

$$L = CK^2 \quad (3.1b)$$

This new equivalent circuit is preferred to the original third order LPF prototype because the lossy series inductor is replaced by admittance inverters and a parallel capacitor [8, 10]. The transformer in 3.1a is dropped from the equivalent circuit in Figure 3.10 because all it does is introduce a 180° phase shift. This added phase shift does not affect the response of the filter, and it can be corrected for in software if needed. Therefore, the transformer in the equivalent series inductor network is removed from the LPF model in Figure 3.10. Again, it is easy to find the values for the third order Chebyshev BPF with inverters from the LPF model in Figure 3.10.

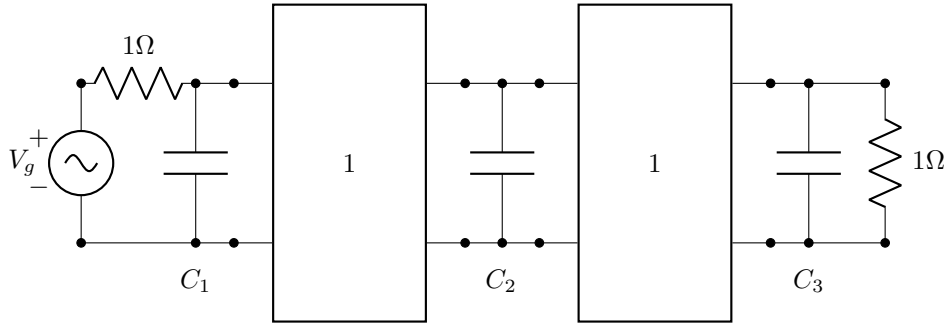


Figure 3.10: Third Order Chebyshev LPF with Inverters

3.4 BPF with Admittance Inverters

Scaling and frequency shifting is applied in the same way as prior, but all of the starting elements are parallel capacitors. Additionally, the center capacitor is calculated from Equation 3.1b, and the center LC resonator values must be calculated from this capacitance. With this in mind, Equations 2.11a, 2.11b, and 2.11c are used to calculate the lumped element values of the parallel LC circuits for the third order Chebyshev BPF with inverters.

This step may seem counter intuitive because lumped inductors are introduced back into the circuit model. However, it is an unavoidable step moving from a lumped element third order Chebyshev LPF model to a BPF circuit model. The lumped elements in the LPF must be replaced with either parallel or series LC circuits to achieve the combination of low-pass and high-pass filtering desired from a BPF.

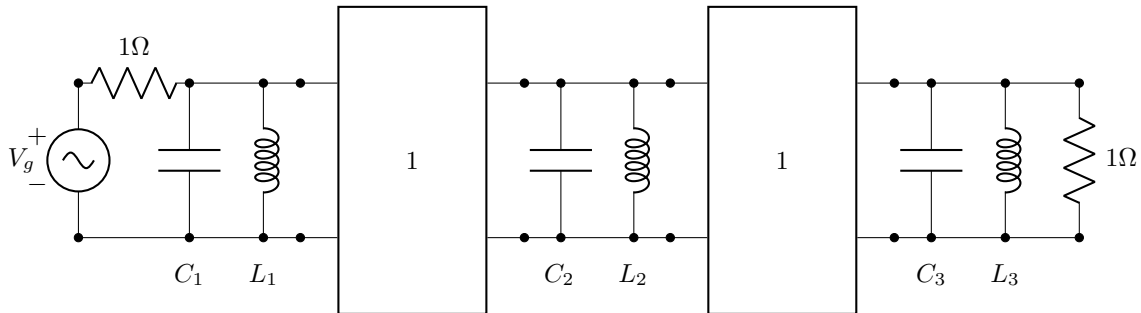


Figure 3.11: Third Order Chebyshev BPF with Inverters ($\omega_0 = 1$ rad/sec, $Z_0 = 1\Omega$).

Table 3.1: Lumped Element Values Used for Third Order Chebyshev Band-Pass Filter Prototype with Inverters ($f_0 = 2.447$ GHz, $Z_0 = 50\Omega$)

Element	Value	Unit
R_S	50	Ω
C_1	11.06394	pF
L_1	0.38237	nH
K	50	-
C_2	14.33253	pF
L_2	0.29517	nH
K	50	-
C_3	11.06394	pF
L_3	0.38237	nH
R_L	50	Ω

The third order Chebyshev BPF with impedance inverters is shown in Figure 3.11. This BPF circuit model is matched to a unity characteristic impedance, however the values for

this prototype are shown in Table 3.1, matched to a 50Ω characteristic impedance. All of the capacitor values are very reasonable. The values for the scaled impedance inverters are denoted as K in Table 3.1. The impedance inverters are frequency independent, so they do not need to be scaled by a factor of the operating frequency. Since the capacitors in Figure 3.10 are replaced with parallel LC resonators, it is necessary to approximate the response of the LC resonator with alternate components. Approximating the response of the LC resonator with an alternate circuit is natural and useful as it eliminates the parallel lumped inductor from each stage of the circuit model.

3.5 Parallel LC Resonator Approximation

A parallel LC resonator circuit is very lossy due to the lumped inductor. Instead, it is common practice to use short-circuited lengths of transmission lines [11]. Short-circuited lengths of transmission lines behave as parallel resonant circuits at lengths of multiples of $\lambda/2$. This behavior is ideal for a design specific to a single operating frequency range, but this topology lends itself to tunability via the surface mount capacitors depicted in Figure 3.1. Instead of calculating the equivalent short-circuited length of transmission line to the parallel LC resonator circuit, the parallel LC resonator circuit is approximated with a short-circuited transmission line in parallel with a lumped capacitor. The parallel short-circuited transmission line in parallel with a lumped capacitor is shown in Figure 3.12. The

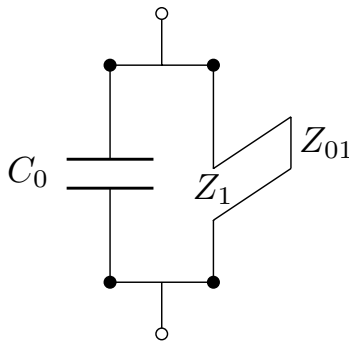


Figure 3.12: Parallel LC Resonator Approximation

labelling Z_1 , in Figure 3.12, corresponds to the input impedance of the transmission line,

and the labelling Z_{01} corresponds to the characteristic impedance of the line.

The most straightforward way to equate the responses of Figure 3.12 to a parallel LC resonator circuit is to set their input admittances and the derivatives of their input admittances equal to one another. The two unknown values are C_0 and Z_{01} from Figure 3.12. With two unknowns and a set of two equations, it is trivial to solve the system of equations. The input admittance of the LC resonator circuit and its derivative are shown as Equations 3.3a and 3.3b. The input admittance of the short-circuited transmission line in parallel with a lumped capacitor and its derivative are shown in Equations 3.3c and 3.3d. The system of equations that describe setting the input admittances of the parallel LC resonator circuit and the short-circuited transmission line in parallel with a lumped capacitor is shown in Equations 3.2a and 3.2b [11].

$$Y_{in} = Y'_{in} \quad (3.2a)$$

$$\frac{\partial Y_{in}}{\partial \omega} = \frac{\partial Y'_{in}}{\partial \omega} \quad (3.2b)$$

$$Y_{in} = \frac{j(\omega^2 LC - 1)}{\omega L} \quad (3.3a)$$

$$\frac{\partial Y_{in}}{\partial \omega} = \frac{j(\omega^2 LC + 1)}{\omega^2 L} \quad (3.3b)$$

$$Y'_{in} = \frac{j(\omega C_0 Z_{01} \tan(\frac{\pi}{2} \frac{\omega}{\omega_r}) - 1)}{Z_{01} \tan(\frac{\pi}{2} \frac{\omega}{\omega_r})} \quad (3.3c)$$

$$\frac{\partial Y'_{in}}{\partial \omega} = j \frac{1}{2} \frac{2C_0 Z_{01} \tan^2(\frac{\pi}{2} \frac{\omega}{\omega_r}) \omega \omega_r + \pi + \pi \tan^2(\frac{\pi}{2} \frac{\omega}{\omega_r})}{Z_{01} \tan^2(\frac{\pi}{2} \frac{\omega}{\omega_r}) \omega_r} \quad (3.3d)$$

There is an additional design parameter that must be addressed while solving this system of equations. The term ω_r , in Equations 3.3c and 3.3d, is referenced as the commensurate frequency. The commensurate frequency is the frequency at which the short-circuited transmission line resonates with reference to the circuit's input impedance. For this design, the commensurate frequency is specified as $2\omega_0$, and this design specification is ideal for reduc-

ing Equations 3.3c and 3.3d as the tangent functions evaluate to 1. To solve the system of equations for C_0 and Z_{01} , Equation 3.2a can be used to represent C_0 in terms of Z_{01} . Then C_0 can be replaced, in Equation 3.2b, with the C_0 representation in terms of Z_{01} . Once Z_{01} is solved for in terms of only known values, C_0 can be solved for.

$$C_0 = C - \frac{4}{\omega_r^2 L} + \frac{2}{\omega_r Z_{01}} \quad (3.4a)$$

$$Z_{01} = \frac{\omega_r L}{4} \left(1 + \frac{\pi}{2}\right) \quad (3.4b)$$

The short-circuited transmission line characteristic impedance, Z_{01} , and the parallel capacitor, C_0 , are solved for using Equations 3.4b and 3.4a. This process is completed for each parallel LC resonator circuit in Figure 3.11, and the updated circuit model values are shown in Table 3.2. At this stage in the mathematical synthesis, the inverters must be realized.

Table 3.2: Open-Circuited Transmission Line and Parallel Capacitor Values Used for Third Order Chebyshev Band-Pass Filter Prototype with Inverters ($f_0 = 2.447$ GHz, $Z_0 = 50\Omega$).

Element	Value	Unit
R_S	50	Ω
C_{01}	8.61354	pF
Z_{01}	7.56605	Ω
K	50	-
C_{02}	11.15822	pF
Z_{02}	5.84058	Ω
K	50	-
C_{03}	8.61354	pF
Z_{03}	7.56605	Ω
R_L	50	Ω

3.6 Realizing Admittance Inverters

The admittance inverters in Figure 3.11 must be realized as some configuration of physically realizable impedances. To accomplish this, the admittance inverter will be represented

as a pi configuration of impedances, shown in Figure 3.13. This admittance inverter circuit

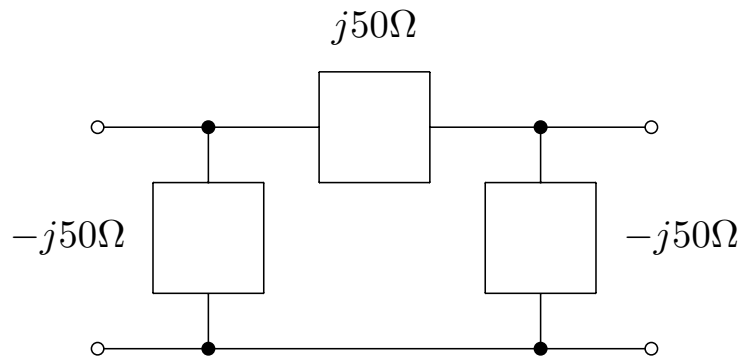


Figure 3.13: Admittance Inverter Circuit Model

model can easily be realized with short-circuited and open-circuited lengths of transmission lines. Specifically, the parallel reactances are realized with parallel open-circuited lengths of transmission line, and the series reactance is realized with a series short-circuited length of transmission line. This realization is shown in Figure 3.14, and it is extremely useful for the combline model realization as the large negative open-circuited transmission line can be combined in parallel with the short-circuited impedance. Since the reactance from the admittance inverter realization is a large negative value, combining it with a smaller positive reactance in parallel results in a positive reactance.

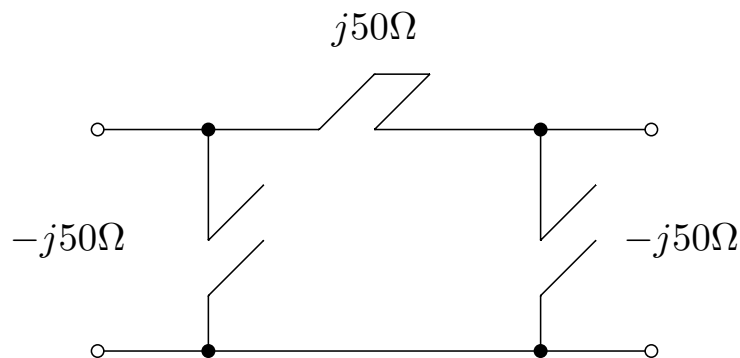


Figure 3.14: Admittance Inverter Realization with Transmission Line Lengths

After realizing the admittance inverters and combining the open and short-circuited lengths of transmission lines in parallel, the third order Chebyshev combline BPF circuit

model is realized in Figure 3.15. This circuit model approximates the core of the BPF in

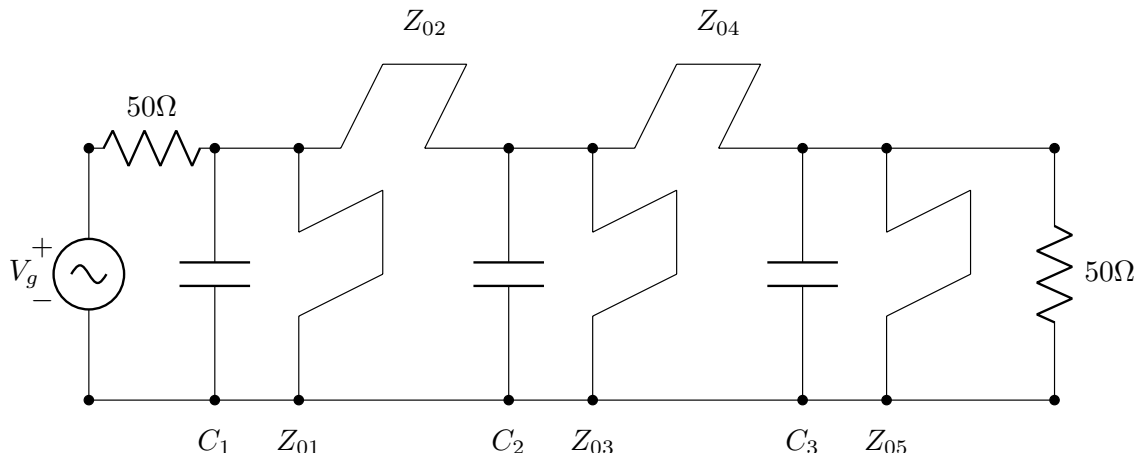


Figure 3.15: Parallel Coupled Line BPF Circuit Model Approximation.

Figure 3.1, and it is clear that there are two pairs of coupled microstrip lines modeled in Figure 3.15. The pi configuration approximation of a pair of grounded coupled microstrip lines, shown in Figure 3.7, is repeated twice in Figure 3.15 by sharing the center short-circuited transmission line in parallel, Z_{03} . The values for the third order Chebyshev combline BPF circuit model approximation are shown in Table 3.3. At this stage in the design process, a circuit model approximation to Figure 3.1 has been realized, but the impedance values in Table 3.3 are not practical for physical realization. Specifically, the short-circuited stubs in parallel have low impedance values, and the lower the impedance value, the wider the microstrip line section will be. The impedance values in Figure 3.15 must be scaled to practical fabrication values.

3.7 Scaling Impedances with Physical Implementation in Mind

The impedances of the short-circuited stubs in Figure 3.15 are too low and would result in impractical physical dimensions. To address this issue, all impedance values are scaled by the same factor. The substrate used for the design is a Rogers 5880 laminate with effective permeativity close to 2.2. Given the electromagnetic properties of the substrate, it is desired to have impedances between 80Ω and 100Ω . This will ensure the physical realizations of the

Table 3.3: Short-Circuited Transmission Line Stubs and Parallel Capacitor Values Used for Third Order Chebychev Band-Pass Filter Circuit Model Approximation ($f_0 = 2.447$ GHz, $Z_0 = 50\Omega$).

Element	Value	Unit
R_S	50	Ω
C_{01}	8.61354	pF
Z_{01}	8.91509	Ω
Z_{02}	50	Ω
C_{02}	11.15822	pF
Z_{03}	10.84959	Ω
Z_{04}	50	Ω
C_{03}	8.61354	pF
Z_{05}	8.91509	Ω
R_L	50	Ω

short-circuited stubs are practical for fabrication purposes and tolerances. The microstrip lines in Figure 3.1 are roughly approximated with the shunt stubs, Z_{01} , Z_{03} , and Z_{05} , in Figure 3.15. The series stubs approximate the impedance introduced by the coupling effects of the microstrip lines, and therefore it is not necessary for their impedance values to fall within a set range. The shunt stubs, on the other hand, should have characteristic impedances between 80Ω and 100Ω . To achieve this, the largest shunt impedance is scaled to 100Ω , and all of the other circuit components are scaled by the same factor. The scaled circuit values are shown in Table 3.4.

Scaling the circuit values in Figure 3.15 made the short-circuited shunt stubs practical for fabrication purposes, but this step introduced another complication. The complication introduced is that the source and load resistances have also been scaled. This means that the core of the BPF is matched to the scaled R_S and R_L instead of the desired characteristic impedance of 50Ω . To combat this issue, a transforming inverter is added after the source resistance and before the load resistance. This inverter could be a quarter wave transformer

Table 3.4: Scaled Impedance Values for the Third Order Chebychev Band-Pass Filter Circuit Model Approximation ($f_0 = 2.447$ GHz, $Z_0 = 50\Omega$).

Element	Value	Unit
R_S	460.84688	Ω
C_{01}	0.93453	pF
Z_{01}	82.16982	Ω
Z_{02}	460.84688	Ω
C_{02}	1.21062	pF
Z_{03}	100	Ω
Z_{04}	460.84688	Ω
C_{03}	0.93453	pF
Z_{05}	82.16982	Ω
R_L	460.84688	Ω

with characteristic impedance as the geometric mean between the source resistance and the input resistance of the filter core.

Instead, an admittance inverter is used because purely resistive loads are being matched from the perspective of the admittance inverter. Since only resistive loads are being matched, the inverter is realized as a series and parallel capacitor, shown in Figure 3.16.

$$Y_{in} = \frac{R_L}{K^2} \quad (3.5a)$$

$$C_b = \sqrt{\frac{1}{\omega^2(K^2 - R_L^2)}} \quad (3.5b)$$

$$C_a = \frac{-1}{C_b R_L^2 \omega^2 + \frac{1}{C_b}} \quad (3.5c)$$

The parallel capacitance, C_a , can be negative, suggesting an inductance, but the negative value is combined in parallel with a positive capacitance yielding another positive capacitance. Given the circuit model in Figure 3.16, the values C_a and C_b are solved for using Equations 3.5a, 3.5b, and 3.5c. An inverter, with impedance equal to the geometric mean of the desired characteristic impedance and the filter core, is inserted after the source and

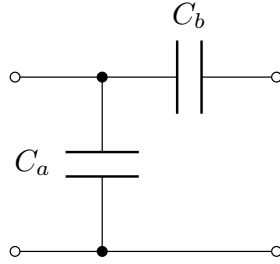


Figure 3.16: The Capacitor Network Used to Realize the Real Impedance Matching Inverter

before the load. The inverter is realized as a network of capacitors, and the new parallel capacitors are combined with the existing capacitances, C_{01} and C_{03} . The final reduced circuit model approximation values are shown in Table 3.5.

Table 3.5: Mathematical Synthesis Final Iteration Values for Circuit Model Approximation ($f_0 = 2.447$ GHz, $Z_0 = 50\Omega$).

Element	Value	Unit
R_S	50	Ω
C_b	0.44041	pF
C_{01}	0.49274	pF
Z_{01}	84.66622477	Ω
Z_{02}	552.15511833	Ω
C_{02}	0.88776	pF
Z_{03}	100	Ω
Z_{04}	552.15511833	Ω
C_{03}	0.49274	pF
Z_{05}	84.66622477	Ω
C_b	0.44041	pF
R_L	50	Ω

3.8 System Impedance Approximations

At this stage in the mathematical synthesis process, a circuit model has been developed to approximate the topology shown in Figure 3.1. This circuit model is comprised of two

series feed capacitors at either port, three parallel capacitor and short-circuited shunt resonators, and two short-circuited shunt capacitances in series alternating with the resonators. The coupled microstrip lines in Figure 3.1 are approximated by the pi configuration of parallel and series short-circuited shunt capacitances. The system impedance of the coupled microstrip lines can be approximated from the equivalent circuits for the combline sections in Figure 3.5 [11, 16, 18, 19]. The pi configuration of short-circuited shunt capacitances in Figure 3.7 is used in conjunction with the circuit in Figure 3.5 to approximate the system impedance of the pair of grounded coupled microstrip lines in Figure 3.4. The equations used to approximate the system impedance of the network in Figure 3.4 are Equations 3.6e, 3.6f, and 3.6g. The equations yield two approximations for the system impedance of the network in Figure 3.4, and the geometric mean of the two approximations is taken as the system impedance approximation. The system impedance approximations from this step are listed in Table 3.6. The dimensions of the coupled microstrip lines in Figure 3.1 are synthesized

Table 3.6: System Impedance Approximations for the Third Order Chebyshev Band-Pass Filter Circuit Model Approximation ($f_0 = 2.447$ GHz, $Z_0 = 50\Omega$).

Symbol	Value	Unit
Z_{0S1}	85.66	Ω
Z_{0S2}	74.07	Ω
Z_{0S}	79.65	Ω
Z_{0e}	91.05	Ω
Z_{0o}	69.68	Ω

from the calculated system impedance approximation. Monolithic python code to determine the complete circuit model parameters presented is shown in Listing A.1. At this stage, the circuit is ready to be modeled and simulated in ADS, and the mathematical synthesis of a circuit model approximation of the topology in Figure 3.1 is complete.

$$n = 1 + \frac{Z_{012}}{Z_{011}} \tag{3.6a}$$

$$k = \frac{1}{n} \quad (3.6b)$$

$$Z_{01} = n \frac{Z_{011} Z_{022}}{Z_{011} + Z_{022} + Z_{012}} \quad (3.6c)$$

$$Z_{02} = n Z_{012} \quad (3.6d)$$

$$Z_{0S1} = Z_{01} \sqrt{1 - k^2} \quad (3.6e)$$

$$Z_{0S2} = Z_{02} \frac{k^2}{\sqrt{1 - k^2}} \quad (3.6f)$$

$$Z_{0S} = \sqrt{Z_{0S1} Z_{0S2}} \quad (3.6g)$$

$$Z_{0o} = Z_{0S} \sqrt{\frac{n-1}{n+1}} \quad (3.6h)$$

$$Z_{0e} = \frac{Z_{0S}^2}{Z_{0o}} \quad (3.6i)$$

CHAPTER 4

PHYSICAL REALIZATION

At this stage in the design process, the dimensions for the microstrip coupled lines are approximated from the system impedances estimated previously. The circuit model is complete, and ADS is the primary tool used to complete the design by tuning and optimizing the microstrip layout. In order to realize the microstrip dimensions corresponding to the system impedance estimations from the previous chapter, a set of empirical equations is used to iteratively solve towards the correct dimensions of a pair of coupled microstrip lines. ADS is used to create a schematic and layout from the calculated microstrip dimensions, and simulations are run on the preliminary ADS design. It is expected that the preliminary simulation does not yield desired results, and the dimensions and capacitor values must be tuned to achieve the desired results. The simulation results and design steps taken in this chapter are achieved through schematic simulation with microstrip models. These simulations are not completely accurate and the objective of this stage of the design process is to achieve the desired response before conducting full electromagnetic simulations. ADS is an ideal tool for this design step as it is very easy to quickly iterate over simulations and tune values to achieve the desired response.

4.1 Iteratively Solving for Coupled Microstrip Line Dimensions

There is a set of empirical equations to solve for the system impedance of a pair of coupled microstrip lines configured like the pair of coupled lines in Figure 3.2. The same set of equations is also used to synthesize the dimensions of the same pair of coupled microstrip lines given a system impedance approximation. There are empirical equations for synthesizing the dimensions of a pair of coupled microstrip lines [18, 19]. ADS implements a version of these synthesis equations in the LineCalc tool [15]. The estimated system impedance, shown in Table 3.6, is provided to the LineCalc tool to synthesize the width, length, and spacing

between a pair of symmetric coupled microstrip lines. It is important that the synthesis is conducted at the desired operating frequency of 2.45GHz. The EM properties of the Rogers 5880 laminate, used to fabricate the design, are also provided for the synthesis. With the approximate length, width, and spacing for the pair of coupled microstrip lines, a preliminary design can be created in an ADS schematic.

4.2 Preliminary Design in ADS

The preliminary design is implemented with lumped capacitors, three coupled microstrip lines, and ports terminating into 50Ω . The physical dimensions yielded from the synthesis are used to define the three coupled microstrip lines, and the capacitances calculated during the final steps of chapter three are used for the ideal capacitors. The widths of the three coupled microstrip lines are equal as the pair of coupled lines is repeated, sharing the center microstrip line of the structure. This property is useful for manufacturing purposes as the design is simplified. The lumped capacitors and microstrip lines are grounded. The circuit schematic of the preliminary design is shown in Figure 4.1. The preliminary simulation yields the results shown in Figure 4.2.

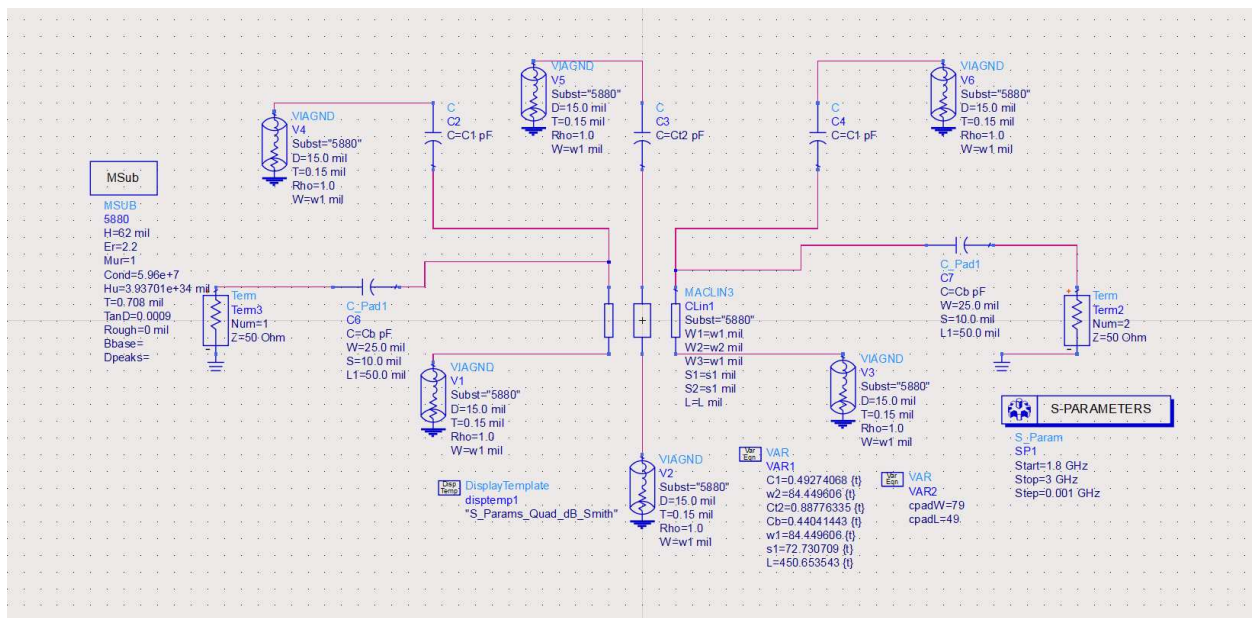


Figure 4.1: The Preliminary Schematic Implemented from the Mathematical Synthesis

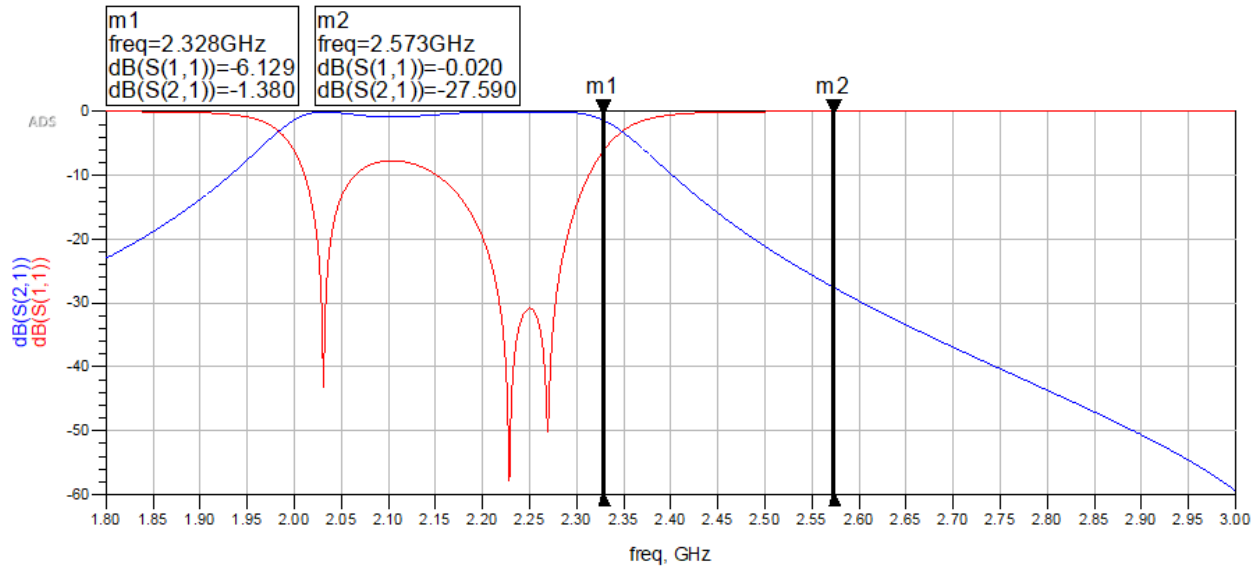


Figure 4.2: Reflections and Transmission Properties of the Preliminary Ideal Microstrip Design

The results in Figure 4.2 are not ideal, but they are very promising. The desired operating pass-band is indicated by the two markers shown in Figure 4.2. The filter response is not centered on 2.45GHz, but it does have a response close to a third order Chebyshev response which is indicated by the three zeroes in the reflections at port one. These results are not ideal, however, because the pass-band bandwidth is too large with additional losses. At this point, the values of the preliminary design can be tuned to achieve the desired design specifications.

4.3 Tuning Preliminary Design in ADS

The desired design specifications, for the preliminary design, are achieved through tuning the physical dimensions of the microstrip lines and the lumped element capacitor values. Through this tuning process, it is observed that decreasing the length of the three coupled microstrip lines shifts the filter operating frequency up. Additionally, increasing the spacing between the three coupled microstrip lines decreases the bandwidth of the filter response. The characteristic Chebyshev response is corrected by slightly shifting the lumped capacitor

values. This tuning process was beneficial, and the desired response for the third order Chebyshev BPF is achieved and shown in Figure 4.3

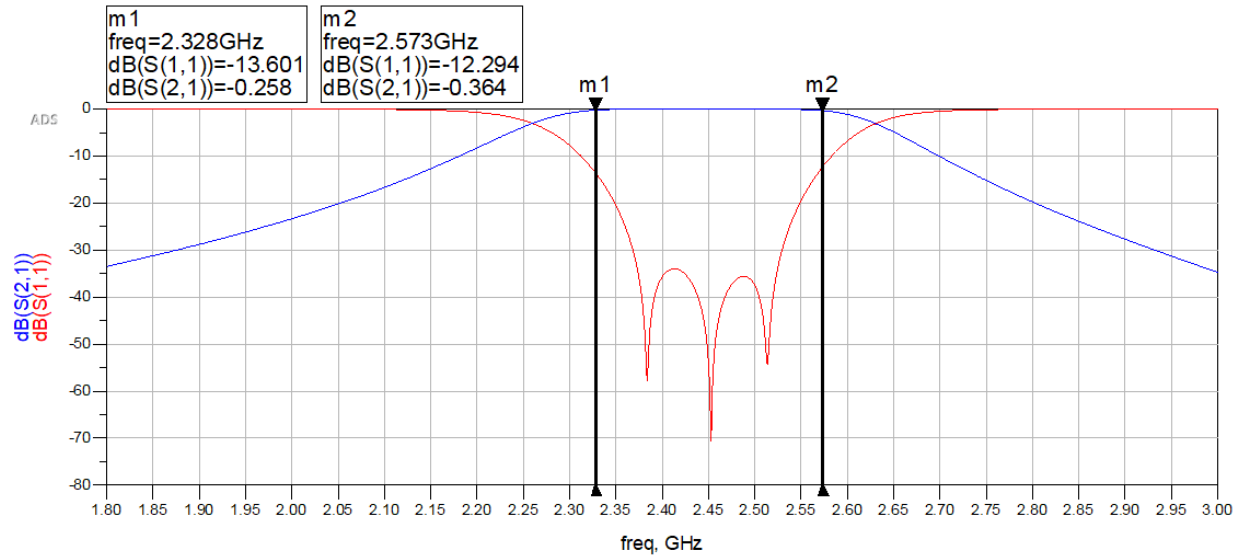


Figure 4.3: Reflections and Transmission Properties of the Tuned Preliminary Ideal Microstrip Design

The results shown in Figure 4.3 are promising as the response is clearly a Chebyshev response with the desired bandwidth. The filter skirts are not too steep, but the results from tuning the preliminary design validate the design procedure. The results in Figure 4.3 are promising, but the preliminary ADS design is not practical. The landing pads for surface mount capacitors are missing. The vias used to ground the three coupled microstrip lines and the capacitors have not been implemented. Furthermore, a feed matching a 50Ω characteristic impedance to the filter core has not been implemented. It is important to consider the practicality of physical dimensions and layout of the ADS design so the device can be fabricated accurately and efficiently.

4.4 Tuning Practical Layout in ADS

The preliminary design is adapted to a practical physical layout by implementing a proper feed, landing pads for surface mount capacitors, and grounding vias. The lumped capacitors from the preliminary design are replaced with landing pads for capacitors with the 0805 SMD

package. Vias are then added to each of the three coupled microstrip lines and the three SMD landing pads that need to be grounded. ADS LineCalc is used to synthesize the width of a 50Ω microstrip line, and the feed is implemented with a quarter wavelength length of tapered microstrip line. The line is tapered from the width matching the 50Ω characteristic impedance to the width of the 0805 SMD landing pad. All of these design changes introduce losses into the filter, and the new layout must be re-tuned. The results of the simulation for the practical layout of the preliminary design are shown in Figure 4.4.

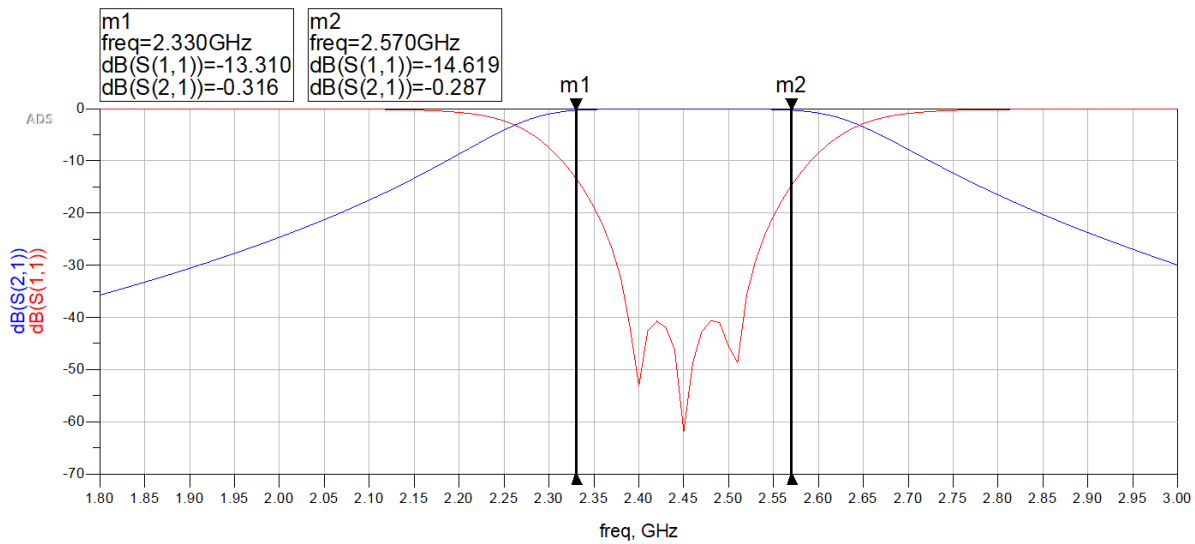


Figure 4.4: Reflections and Transmission Properties of the Tuned Ideal Microstrip Design with a Practical Layout

It is important to re-tune the design parameters after adding new features to the design layout. Each additional section of microstrip line changes the overall system impedance of the filter. Vias introduce additional inductance to the circuit and can shift the center frequency of the design. If tuning is not conducted after introducing additional features, the desired filter response could be lost completely. The response in Figure 4.4 is tuned to retain the desired Chebyshev response, but the overall performance of the filter is not perfect. In order to achieve the most desirable filter response, the design is optimized using gradient steepest descent.

4.5 Optimizing Practical Layout in ADS

ADS is used to optimize the practical layout before moving to complete EM simulation. Complete EM simulations are more time consuming, so it is important to have a strong starting point to reduce the number of iterations needed for full EM simulations. To optimize the filter response of the practical filter layout, goals are set for the pass-band response. Once the goals are set according to the desired filter response, ADS iterates towards a solution with zero error by systematically running the simulation while sweeping parameterized variables. The variables parameterized for this optimization are the dimensions of the three coupled microstrip lines and the lumped capacitor values. The results from these optimizations are shown in Figure 4.5, and the response is promising. The pass-band is centered on 2.45GHz with very little loss, and the response bandwidth is meets the specifications for the filter. This is a strong starting point moving forward with full EM simulations in ADS.

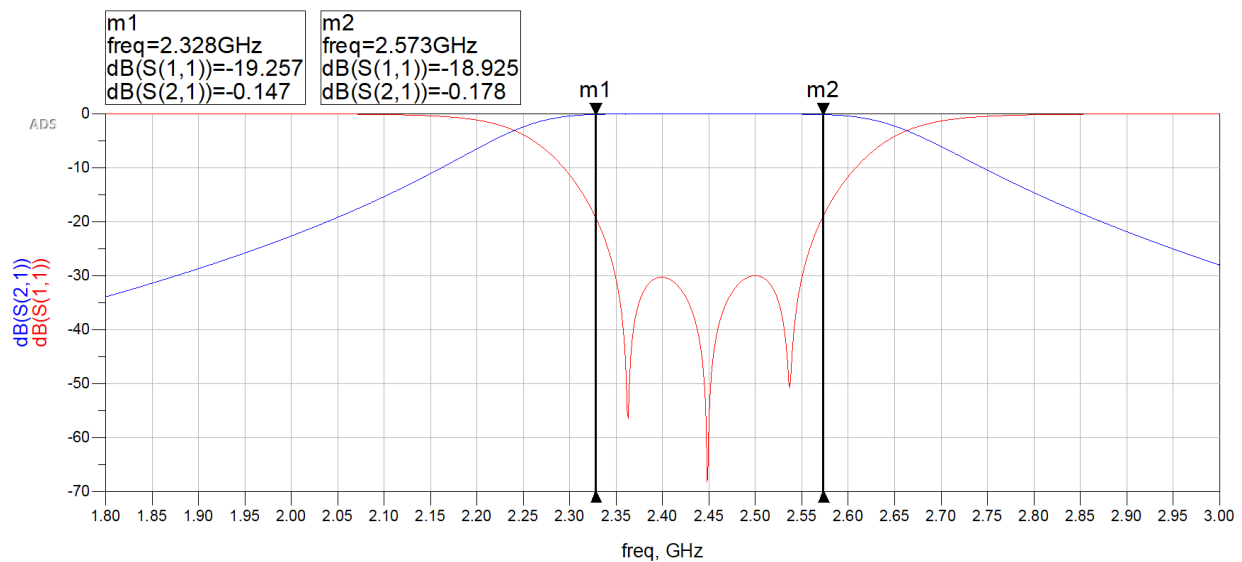


Figure 4.5: Reflections and Transmission Properties of the Optimized Ideal Microstrip Design with a Practical Layout

CHAPTER 5

EM CO-SIMULATION AND FURTHER OPTIMIZATIONS

Full EM simulations are important for solidifying the expected behavior of a device before fabrication. Results generated from ideal microstrip line behaviors ignore the effects of coupling between lines and components. It is very important to account for losses and coupling between all microstrip sections before fabricating any device. If this step is overlooked, the fabricated device likely will not perform. To ensure this design is ready for fabrication, the practical layout is generated and a full EM simulation is conducted. This simulation data is then used to create a co-simulation where the surface mount capacitor values and the dimensions of the combline sections are parameterized for tuning and optimization. Once the response of the filter is comparable to the response in Figure 4.5, the design is ready for fabrication. This step is also used to gauge the tunability of the third order Chebyshev BPF design with combline topology.

5.1 Optimizing with Co-Simulation

Since this design relies on surface-mount capacitors, a standard EM simulation is not sufficient. Instead, ports are defined for each terminal and each connection from lumped components. With the ports defined, a standard EM simulation is conducted to generate the reference data set for subsequent co-simulations. Once the standard EM simulation finishes, a symbol describing the physical layout of the design and its port connections is defined. This symbol is then used in another schematic where lumped capacitors are connected to the defined ports. Each coupled microstrip has two ports defined that are connected to ground and a lumped capacitor. The lumped capacitor values are set based on the capacitor values used to generate the filter response in Figure 4.5. Once all ports are terminated with their corresponding components, the co-simulation is executed from the new schematic.

After the simulation completes, the response looks similar to the filter response in Figure 4.2. Since the full EM simulation accounts for coupling between microstrip lines and inductance introduced from the presence of vias, the operating frequency of the filter is shifted downward and additional losses are present. Much like the process in chapter four, the physical parameters and capacitor values are tuned until the EM co-simulation yields the desired response of a third order Chebyshev combline BPF. This process is a lot more time consuming because for every iteration, the full EM simulation must be executed. The tuning and optimization steps in chapter four are justified further because of the results from the first co-simulation. If the tuning and optimization steps from chapter four were skipped, the co-simulation results would be even further from the desired response, and it would take that much longer to achieve the desired response using the full EM simulator in ADS.

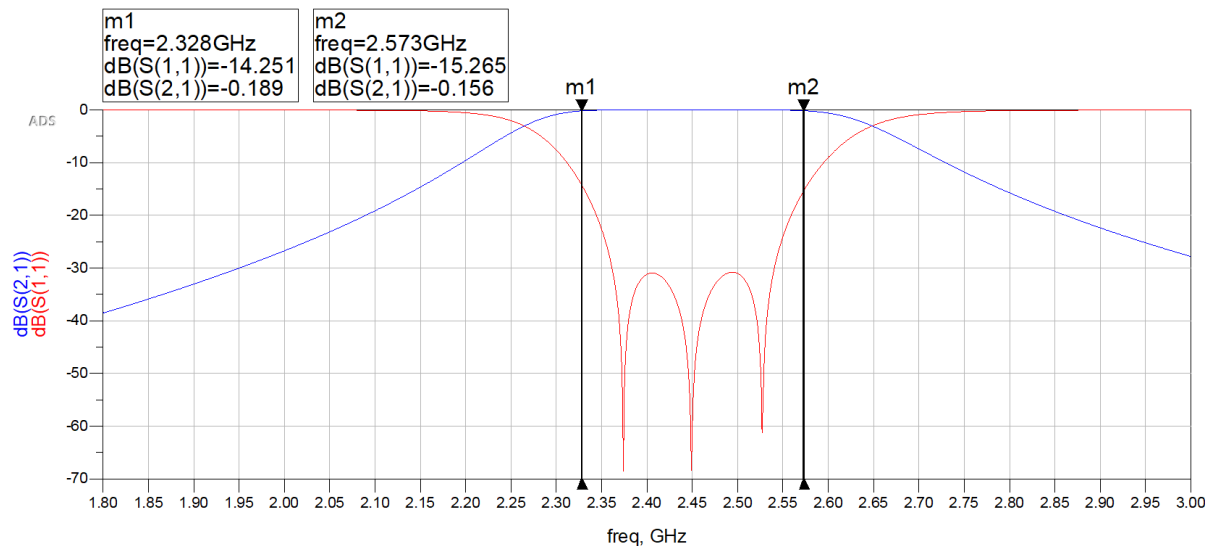


Figure 5.1: Reflections and Transmission Properties of the Optimized Microstrip Design from Full EM Simulation

Upon completion of this optimization step, the co-simulation yields the results in Figure 5.1. The response in Figure 5.1 meets all of the design requirements for the third order Chebyshev combline BPF. The pass-band response has very little loss, and the filter skirts are fairly steep. The Chebyshev response is almost perfectly symmetrical, and the pass-band

ripple is very low. At this point, the tunability of the filter with realistic capacitor values is tested.

5.2 Defining Operating Ranges

Once the design for the third order Chebyshev combline BPF is fabricated, there will be three degrees of freedom used for setting the center frequency of the filter and shaping the response. There are five surface mount capacitors present in the design, but since the layout is symmetric the outer pairs of capacitors will be set to the same values respectively. This effectively yields three degrees of freedom as there are two feed capacitors, two outer combline capacitors, and once capacitor on the center combline. The capacitances, C_b , C_1 , and C_2 , used to achieve the filter response in Figure 5.1 are 0.106pF, 1.062pF, and 1.422pf respectively. These are perfectly reasonable capacitor values, and they serve as the midpoint for the range of operation of the presented combline design. The maximum and minimum desired operating frequencies are 10 percent above and below the center frequency of the BPF. Therefore, the capacitors, C_b , C_1 , and C_2 , are varied to achieve this desired tuning range, and the transmission and reflection properties for each case are presented.

5.3 Maximum Operating Frequency

The maximum desired operating frequency is 2.7GHz, and the capacitor values for C_b , C_1 , and C_2 to achieve this operating frequency are 0.052pF, 0.867pF, and 1.147pF respectively. The results from tuning this device are shown in Figure 5.2, and the results are very good. The tuned response is outlined with markers against the original response. The tuned filter response is well within acceptable operating parameters. The center frequency is 2.6GHz, and a ten percent pass-band bandwidth is maintained. The capacitor values are also very reasonable.

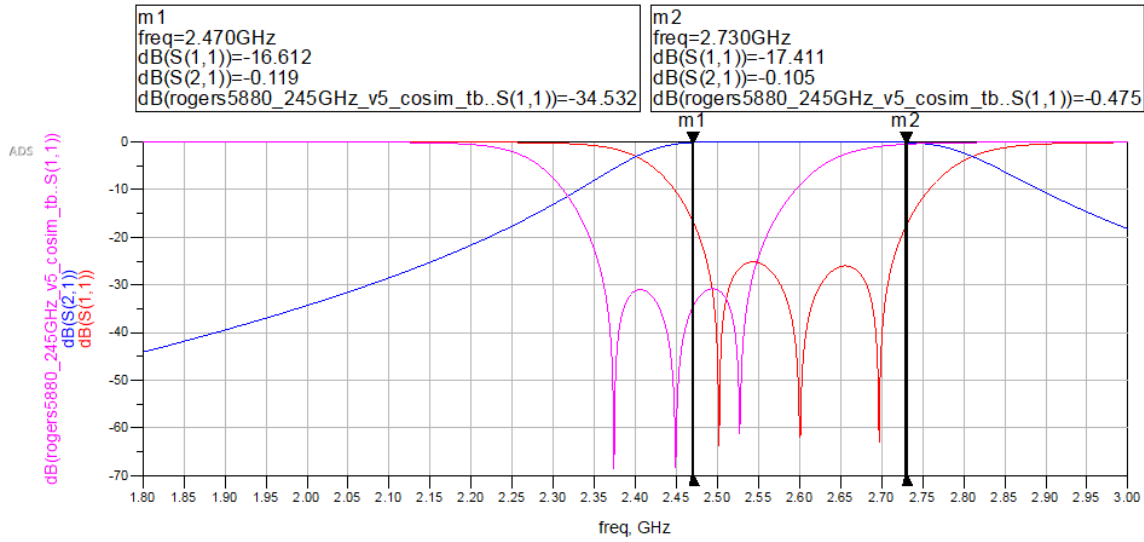


Figure 5.2: Higher Frequency Reflections and Transmission Properties of the Optimized Microstrip Design from Full EM Simulation

5.4 Minimum Operating Frequency

The minimum desired operating frequency is 2.2GHz, and again these capacitor values are reasonable. The capacitor values for C_b , C_1 , and C_2 achieving the minimum desired operating frequency are 0.135pF, 1.327pF, and 1.762pF respectively. The response corresponding to these capacitor values is outlined with markers in Figure 5.3, and the responses from the previous two sets of capacitor values are overlaid on the plot. The pass-band ripple is not as good in this plot, but the response is still well within an acceptable operating range.

Since the responses of the three sets of tuned capacitors yielded acceptable results, the topology likely supports an even larger range of operating frequencies. A full set of EM simulations yielded desirable results, and the third order Chevychev combline BPF layout is ready for fabrication.

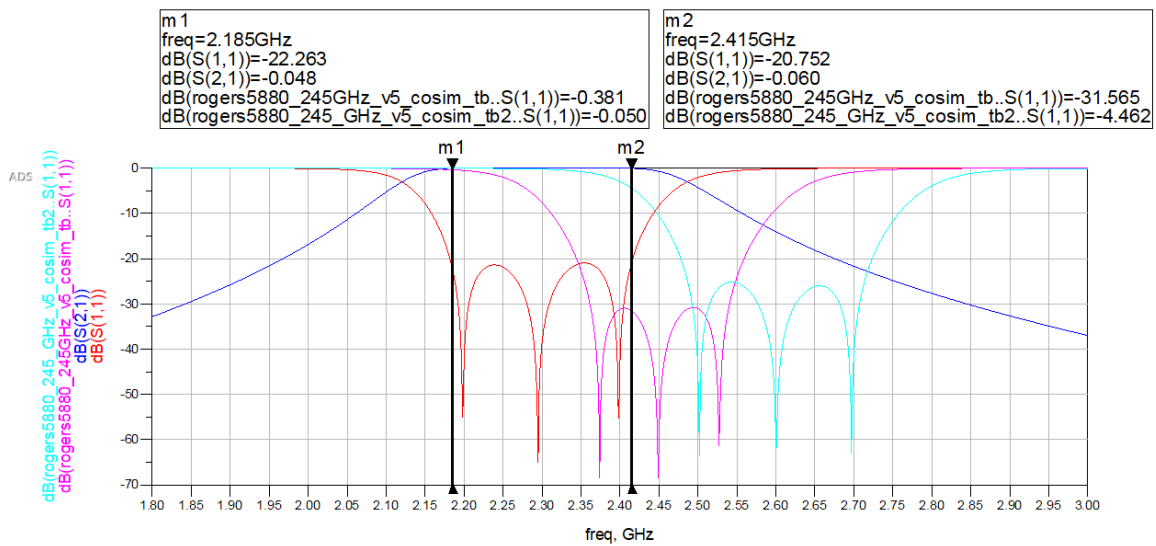


Figure 5.3: Lower Frequency Reflections and Transmission Properties of the Optimized Microstrip Design from Full EM Simulation

CHAPTER 6

MICROSTRIP FILTER PROTOTYPE

The design has been completed in simulation and is ready for fabrication. The microstrip layout presented is designed for fabrication on Rogers 5880 laminate with half-ounce copper cladding and standard vias to the ground plane. This substrate has a dielectric constant of 2.2 with loss tangent of 0.0009. It is 62 mil thick, and is a great choice for low loss and high performing designs. The complete design dimensions are outlined below.

6.1 Board Layout

The top view of the final board layout is shown in Figure 6.1. This image is not to scale and is larger to show the details of the board. From port one to port two, the design is 2.511 inches wide. All of the combines are equal in width and length, and the spacing between them is equal. The tapered feeds are one quarter wavelengths long, and they are 0.190 inches wide at each port to match 50Ω at the center frequency of the design. Each combline is 0.125 inches wide and separated from one another by 0.098 inches. Each combline section is 0.231 inches long. Each via has a landing pad width of 0.025 inches and a length of 0.015 inches. To match the 0805 SMD package specifications, each capacitor landing pad is 0.094 inches from end to end with a width of 0.043 inches. The spacing separating each side of the capacitor landing pads is 0.032 inches. On each of the outer two combline sections, a T-junction section of microstrip is added to interface the capacitor pads perpendicularly while feeding the combline.

The design layout on the Rogers 5880 laminate is visualized in Figure 6.2. The vias are shown at each combline section and at each capacitor landing pad. The substrate is 0.062 inches thick with half ounce copper cladding for the microstrip lines. The design should perform well based on the final simulation optimization results from chapter five.

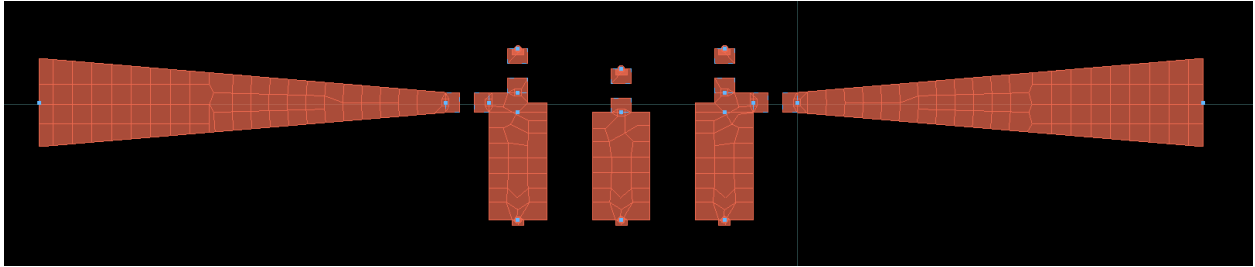


Figure 6.1: Top View of Third Order Chebyshev BPF Microstrip Realization

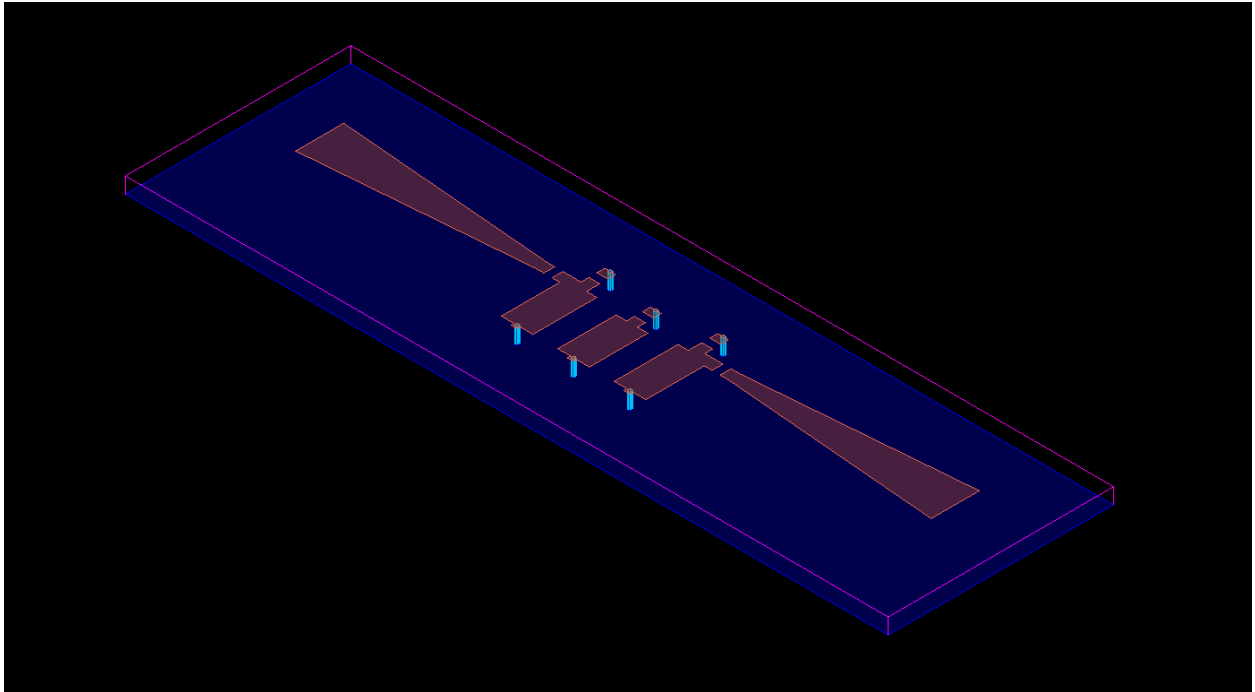


Figure 6.2: View of Third Order Chebyshev BPF Microstrip Realization on Rogers 5880 Laminate

6.2 Confidence

The results from momentum are compelling enough that the board will function properly within a low percentage of error given appropriate surface mount capacitor values. The center frequency will likely be shifted downward, at the capacitor values determined in chapter five, due to inductance introduced from the fabrication process. Any additional conductor at the vias will add inductance, and small fabrication errors will change the behavior slightly. However, given the tunable nature of the device, the surface mount capacitor values from chapter five can be changed slightly to achieve the desired performance. Additionally, the response of the device is unlikely to achieve a perfect Chebychev response when using static surface-mount capacitors. This is because surface-mount capacitors are typically not available with error below 0.05pF. To address this, the optimized design was simulated with surface-mount capacitor values immediately available. The results of this simulation are shown in Figure 6.3 where C_b , C_1 , and C_2 are 0.2pF, 1.3pF, and 1.8pF respectively, which are the closest surface-mount capacitor values available for the lower range of operating range presented in chapter five. Each surface-mount capacitor used has a tolerance of 0.05pF. Immediately it is apparent that two of the Chebychev filter resonances have been absorbed into the inaccuracy of the chosen surface-mount capacitors. However, the filter is still operating within acceptable design specifications. The operating bandwidth is ten percent of the center frequency with very good forward transmission in the pass-band. Furthermore, with mechanically tunable surface-mount capacitors, the response can easily be fine-tuned, and therefore the design is practical for fabrication with all dimensions well within manufacturing tolerances.

6.3 Expected Results

The fabricated design is expected to perform well as the full EM simulation yielded excellent results along with Rogers 5880 being a high quality laminate. The performance of the design will be evaluated by collecting frequency sweep measurements across the ports of

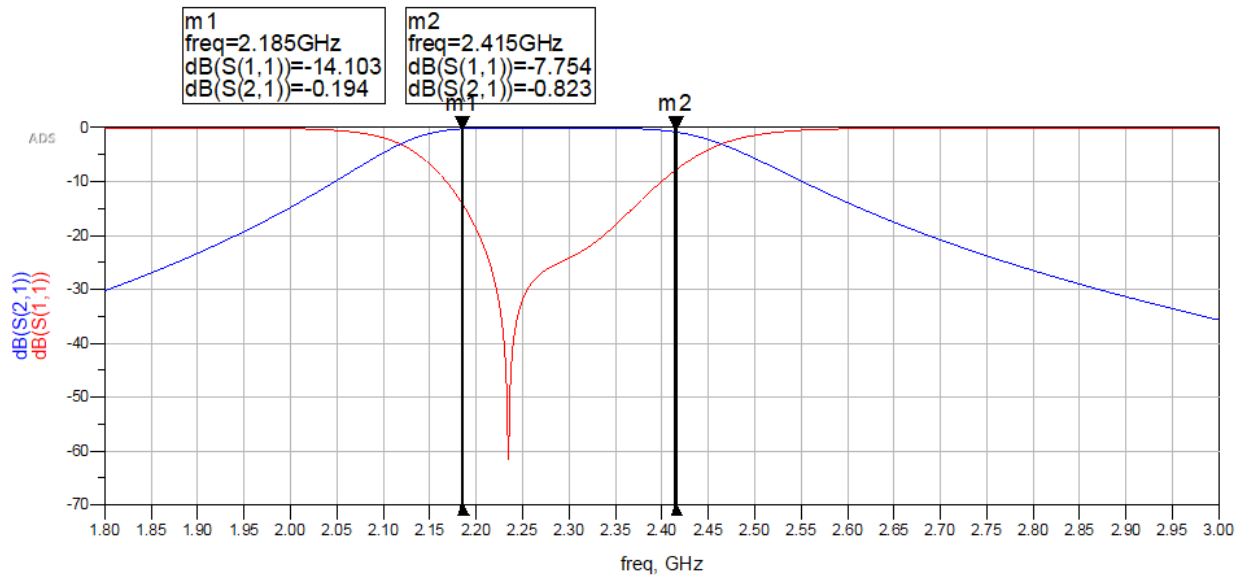


Figure 6.3: Reflections and Transmission Properties of the Optimized Microstrip Design with Available Surface-Mount Capacitors

the device. The tunability of the device will be explored by configuring the three fabricated boards in the minimum, center, and maximum operating ranges outlined in chapter five and performing the sweep measurements with all three devices. Since there are three copies of the board initially, surface mount capacitors at each operating range are soldered to each board and the performance can be measured. It is unlikely the perfect Chebyshev responses in Figure 5.3 will be measured, but the desired center frequency and filter bandwidth will be observed. It is likely that one or two of the resonances will be lost in the tolerances of the surface-mount capacitors, but the filter will still operate within design specifications. The design presented is the foundation for the design process of n -th order Chebyshev combline BPF's, and there is still a lot of work to be done.

CHAPTER 7

FUTURE WORK

A third order Chebyshev combline BPF was presented, and the design can easily be extended to higher order alternative topologies. The presented design leverages surface-mount capacitors to generate the desired Chebyshev filter response. Surface-mount capacitors are used to calibrate static instances of the design, but the topology is ideal for tunability. In simulation, it is evident that tuning the surface-mount capacitor values shifts the center frequency of the filter. Redesigning the board layout for analog tunable capacitors or digitally tunable varactor diodes would enable the user to tune the third order Chebyshev combline BPF to the desired operating frequency without having to change any layout parameters. Furthermore, each of these design iterations would be tested for usability and performance.

7.1 Analog Tunable Capacitors

To implement analog tunability on the presented third order Chebyshev combline BPF, the layout must be changed to accommodate such a surface-mount capacitor. Most analog tunable capacitors have a larger footprint than the standard surface-mount capacitor. This would not pose an issue though as the footprint can be designed using ADS and the layout optimized with a capacitance across the new footprint. Once the design is re-optimized and fabricated, the analog tunability of the filter can be verified against simulation results. Verifying this functionality is grounds to move forward with implementing a design which could be tuned digitally with actively biased varactor diodes.

7.2 Digitally Tunable Varactor Diodes

Given that the design supports a range of operating frequencies within the design specifications, the filter topology can be overhauled to support actively biased varactor diodes, enabling digital tuning. This is non-trivial work because the design will no longer be a

passive device. A footprint for the varactor diode would have to be created in ADS, and a feed line for each varactor diode would have to be added to the layout. Additionally, since the varactor diode is an active device, appropriate RF chokes and DC blocks would have to be implemented to preserve the filtered signal. Along with the difficulties of introducing active components to the design, providing the voltage to correctly bias the circuit is difficult. Once the design is tuned and optimized in ADS, it can be fabricated and tested. Once the device is tested, its operating frequency ranges can be profiled to support software-defined filter operation. Another consideration for future work is determining a solution to feed the varactor diodes to achieve the desired capacitance seen by the filter. Implementing the design with digitally tunable varactor diodes introduces functionality desirable for cognitive radio applications. Cognitive radio technology leverages programmable devices to modify transmit and receive chain parameters quickly. An implementation of a digitally tunable BPF adds robustness to any cognitive radio system.

7.3 Testing Fabricated Designs

The design presented in this paper must be fabricated and tested. As mentioned in chapter six, the presented design will be fabricated multiple times to verify the center operating frequency along with the minimum and maximum desired frequencies. Once the boards are fabricated, surface-mount capacitors are chosen to achieve the center, minimum, and maximum operating frequency ranges. These capacitors are manually soldered to each board, and RF coaxial connectors are soldered to the two feeds of each board. Then the S-parameters of the devices can be measured and recorded using a VNA. At this stage, the measured results are plotted against simulated results to gauge the percent error introduced by the fabrication and preparation of each board. This procedure will be conducted for the analog tunable surface-mount capacitor design as well as the digitally tunable active varactor diode design.

The analog tunable surface-mount capacitor design and the digitally tunable varactor diode design will only have to be fabricated once as they will be tested to achieve the

minimum and maximum operating frequency ranges achieved by the static surface-mount capacitor designs. All of the testing will be conducted using a standard VNA, and the varactor diodes will be driven with the appropriate biasing voltages from a bench power supply. Once the varactor diode design's operating frequency range is profiled, a solution to digitally provide appropriate source voltages to the varactor diodes will be explored.

7.4 Simple Cognitive Radio Application

Once the design of the digitally tunable third order Chebyshev combline BPF is completed and profiled, it can be used in a cognitive radio system. A practical cognitive radio system could be implemented with an SDR, two mono-pole antennas operating from 1.9 GHz to 3 GHz, and the digitally tunable BPF inline with the transmit chain of the system. One of the mono-pole antennas could be configured on a receiving channel of the SDR, and the other mono-pole antenna could be connected to the output port of the digitally tunable BPF inline with a transmitting channel of the SDR. The receive channel samples the spectrum of possible operating frequencies of the transmit chain and leverages spectrum sensing algorithms to determine which center frequency contains the lowest congestion. The digitally tunable BPF is then configured to operate on the low congestion band. This is a simple system but would solidify the functionality and capabilities of the digitally tunable filter.

CHAPTER 8

CONCLUSIONS

The mathematical synthesis and design of a third order Chebyshev combline BPF was presented. The topology of the filter was chosen because it allows the device to be tuned to different center frequencies. Tuning the filter response is achieved by adjusting the capacitor values at the feeds and at each of the combline sections. The design presented uses standard surface mount capacitors to achieve a static filter response, but the design could easily be adapted to support variable analog or varactor diode capacitors. The mathematical synthesis of the third order Chebyshev combline BPF was illustrated by determining an approximate circuit model representation of three parallel coupled microstrip lines. This synthesis was developed from known transformations and approximations from other works.

Once the circuit model approximation was determined, an approximation for the system impedance of the circuit was calculated. Then the dimensions of corresponding coupled microstrip lines were synthesized from the calculated system impedance approximation. With the physical dimensions realized, ADS was used to simulate the design with the capacitor values calculated from the mathematical synthesis. The initial simulation results did not meet the design parameters of the BPF, but they were promising as the pass-band featured a rough Chebyshev response with reasonable bandwidth. The dimensions of the layout and the capacitor values were manually tuned to achieve the desired response before implementing a practical microstrip topology. Landing pads for the surface-mount capacitors, feed lines, and vias were placed appropriately to achieve a feasible realization before simulating and tuning the design again. The desired Chebyshev response was achieved again before running full EM simulations on the design. Full EM simulations are more accurate as they account for coupling effects between microstrip sections, and they are also more time consuming.

The first full EM simulation was run with a layout optimized with ideal circuit model simulations, and the results were similar to the initial simulation results. The pass-band was shifted down from the desired operating frequency, a rough Chebyshev response was observed, and the bandwidth was acceptable. Again, the dimensions of the layout and capacitor values were tuned to achieve a decent Chebyshev response at the desired operating frequency. Then the design was optimized to achieve the BPF filter design requirements. At this point, the dimensions of the microstrip layout were rounded to the nearest thousandth of an inch for fabrication purposes, and the tuning capabilities of the device were estimated. Estimates of the minimum and maximum operating frequencies of the design were presented, and the device maintained a desirable pass-band across the varying operating frequencies.

Future work outlining design modifications to enable analog and digital tuning were presented. Along with alterations to the layout, a testing plan was presented to verify the functionality of each fabricated device. Testing would be conducted to verify static operation cases, operation utilizing analog tunability, and operation leveraging digital tunability. Furthermore, a simple cognitive radio system was outlined to showcase the abilities of a digitally tunable BPF.

The third order Chebyshev combline BPF serves as a foundation for designing digitally tunable n -th order Chebyshev combline BPF's. The mathematical synthesis presented was validated through simulation results, and the combline topology is verified to be ideal for tuning filter operating frequencies while maintaining desired response characteristics. Cognitive radio is an important technology for navigating the already congested spectrum by adaptively and intelligently configuring operating parameters of a system's transmit and receive chains. Digitally tunable filtering is very useful for cognitive radio systems, and the third order Chebyshev combline BPF presented is a strong foundation for developing and implementing digitally tunable BPF's.

REFERENCES CITED

- [1] Bruce A. Fette. *Cognitive Radio Technology*. Elsevier Inc., 2nd edition, 2009. ISBN 978-0-12-374535-4.
- [2] Thomas Jordbru, Henning Idsøe, Linga Reddy Cenkeramaddi, Baltasar Beferull-Lozano, and Mohamed Hamid. Radio measurements on a customized software defined radio module: A case study of energy detection spectrum sensing. In *2017 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, pages 1–6, May 2017. doi: 10.1109/I2MTC.2017.7969681.
- [3] J. C. Merlano-Duncan, Tadilo Endeshaw Bogale, and Long Bao Le. SDR Implementation of Spectrum Sensing for Wideband Cognitive Radio. In *2015 IEEE 82nd Vehicular Technology Conference (VTC2015-Fall)*, pages 1–5, September 2015. doi: 10.1109/VTCFall.2015.7391127.
- [4] Iker Sobron, Paulo S. R. Diniz, Wallace A. Martins, and Manuel Velez. Energy Detection Technique for Adaptive Spectrum Sensing. *IEEE Transactions on Communications*, 63(3):617–627, March 2015. ISSN 1558-0857. doi: 10.1109/TCOMM.2015.2394436. Conference Name: IEEE Transactions on Communications.
- [5] Sheetal Kalambe, Padma Lohiya, and P. Malathi. Performance evolution of energy detection spectrum sensing technique used in cognitive radio. In *2014 International Conference on Signal Propagation and Computer Technology (ICSPCT 2014)*, pages 786–790, July 2014. doi: 10.1109/ICSPCT.2014.6884975.
- [6] Mahmood Abdulsattar. Energy Detection Technique for Spectrum Sensing in Cognitive Radio: A Survey. *International journal of Computer Networks & Communications*, 4: 223–242, September 2012. doi: 10.5121/ijcnc.2012.4514.
- [7] D. Cabric, Shridhar Mishra, and Robert Brodersen. Implementation issues in spectrum sensing for cognitive radio. In *Conference Record - Asilomar Conference on Signals, Systems and Computers*, volume 1, pages 772–776 Vol.1, December 2004. ISBN 978-0-7803-8622-8. doi: 10.1109/ACSSC.2004.1399240.
- [8] I.C. Hunter and J.D. Rhodes. Electronically Tunable Microwave Bandpass Filters. *IEEE Transactions on Microwave Theory and Techniques*, 30(9):1354–1360, September 1982. ISSN 1557-9670. doi: 10.1109/TMTT.1982.1131260. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

- [9] S.R. Chandler, I.C. Hunter, and J.G. Gardiner. Active varactor tunable bandpass filter. *IEEE Microwave and Guided Wave Letters*, 3(3):70–71, March 1993. ISSN 1558-2329. doi: 10.1109/75.205668. Conference Name: IEEE Microwave and Guided Wave Letters.
- [10] S. Caspi and J. Adelman. Design of combline and interdigital filters with tapped-line input. *IEEE Transactions on Microwave Theory and Techniques*, 36(4):759–763, April 1988. ISSN 1557-9670. doi: 10.1109/22.3583. Conference Name: IEEE Transactions on Microwave Theory and Techniques.
- [11] David M. Pozar. *Microwave Engineering*. John Wiley & Sons, Inc., University of Massachusetts at Amherst, 4th edition, 2012. ISBN 978-1-118-21363-6. OCLC: 915311644.
- [12] *RT/duroid 5870/5880 High Frequency Laminates*. Rogers Corporation, 2017. URL <https://rogerscorp.com/-/media/project/rogerscorp/documents/advanced-connectivity-solutions/english/data-sheets/rt-duroid-5870---5880-data-sheet.pdf>. Revised 1306 060117.
- [13] Janusz A. Dobrowlski. *Microwave Network Design Using the Scattering Matrix*. Artech House, 2010. ISBN 9781608071296. URL <http://library.books24x7.com/mines.idm.oclc.org/toc.aspx?bookid=42769>.
- [14] Forester W. Isen. *DSP for MATLAB and LabVIEW III: Digital Filter Design*. Morgan & Claypool, 2008. ISBN 9781598298970.
- [15] Keysight Technologies. Pathwave advanced design system (ads). <https://www.keysight.com/us/en/products/software/pathwave-design-software/pathwave-advanced-design-system.html>, 2020. Accessed: 2020-03-04.
- [16] Rajesh Mongia. *RF and Microwave Coupled-Line Circuits*. Boston: Artech House, 2nd edition, 2007. ISBN 1-59693-157-4.
- [17] Daniel Alex Ramirez. Tunable Combline Filter and Balun: Design, Simulation, and Test. Master’s thesis, University of South Florida, March 2017.
- [18] Luis Costa and Martti Valtonen. Implementation of Single and Coupled Microstrip Lines in APLAC. Address: Circuit Theory Laboratory, P.O. Box 3000, FIN-02015 HUT, Finland, December 1997.
- [19] Stefan Jahn. Parallel coupled microstrip lines. <http://qucs.sourceforge.net/tech/node77.html>, December 2007.

APPENDIX
MATHEMATICAL SYNTHESIS CODE LISTING

Listing A.1: Python Code Used for the Mathematical Synthesis of the Circuit Model Approximation

```
# Author: Tanner Lucas
# Date: 01/02/2020
# Description: Code used for the mathematical synthesis of a third
order chebyshev bandpass filter.
# Design goals and choices are read from the provided configuration
file, and even and odd mode system impedances
# as well as geometry approximations are yielded.

import math
import numpy as np

def calculate_chebychev_coefficients(n, eps):
    """
    description - given the order of the filter and the ripple factor
    of the filter, determine the corresponding chebychev
    coefficients
    """
    if (np.floor(n) != n):
        print("Error: 'n' must be an integer representing the order of
        the filter")

    elif (np.floor(eps) == eps):
        print("Error: input 'epsilon' must be a numeric value
        representing the desired ripple factor")

    else:
        Rdb = 10*np.log10(1+math.pow(eps,2))
        beta = np.log(1/np.tanh(Rdb/(2*20*np.log10(np.e))))
        gamma = np.sinh(beta/(2*n))

        # initialize the array of chebychev coefficients
        g = np.zeros(n+2)

        # if the order is odd, set g0 and gn to 1
        if (np.mod(n,2) == 1):
            g[0] = 1
```

```

        g[n+1] = 1

# otherwise set them based on the provided equation.
else:
    g[0] = pow(np.tanh(beta/4), 2)
    g[n+1] = pow(np.tanh(beta/4), 2)

a = np.zeros(n)
b = np.zeros(n)
for i in range(n):
    b[i] = math.pow(gamma,2)+math.pow(np.sin((i+1)*np.pi/n), 2)
    a[i] = np.sin((2*(i+1)-1)*np.pi/(2*n))

g[1] = 2*a[0]/gamma

# print(a)
# print(b)
for k in range(1,n):
    g[k+1] = (4*a[k-1]*a[k])/(b[k-1]*g[k])

return g

def lpf_to_bpf_parallel(g, f, bw, n):
    C = np.zeros(n)
    L = np.zeros(n)
    omega_1 = 2*np.pi*(f-f*(bw/2))
    omega_2 = 2*np.pi*(f+f*(bw/2))
    omega_0 = np.sqrt(omega_1*omega_2)
    alpha = omega_0/(omega_2-omega_1)
    for k in range(n):
        C[k] = alpha*g[k]/omega_0
        L[k] = 1/(alpha*g[k]*omega_0)

    return L, C

def parallel_lc_to_parallel_shunt_and_cap(L, C, f, n):
    omega = 2*np.pi*f
    omega_r = 2*omega
    Z0 = np.zeros(n)
    C0 = np.zeros(n)
    for k in range(n):
        Z0[k] = (omega_r*L[k]/4)*(1+np.pi/2)
        C0[k] = C[k] - (4/(math.pow(omega_r,2)*L[k])) + (2/(omega_r*Z0[k]))

```

```

        # print("L: {},\tC: {},\tZ0: {},\tC0 {}".format(L[k], C[k], Z0[
            k], C0[k]))

    return C0, Z0

def main():
    # define constants
    Z0 = 50 # characteristic impedance of 50 ohms
    ZL = 50 # the load impedance is 50 ohms
    n = 3 # order of the filter
    f = 2.45e+9 # target center frequency of filter
    eps = 0.1 # desired ripple factor not in dB
    bw = 0.1 # bandwidth of passband

    imp_range = 100

    print("Synthesis_Config:_")
    print("\tZ0:\t\t{}".format(Z0))
    print("\tZL:\t\t{}".format(ZL))
    print("\tn:\t\t{}".format(n))
    print("\tf:\t\t{}".format(f))
    print("\t\teps:\t\t{}".format(eps))
    print("\tbw:\t\t{}".format(bw))
    print("\n")

    g = []
    g = calculate_chebychev_coefficients(n, eps)

    print("Chebychev_Coefficients:_")
    print(g)
    print("\n")

    # with the chebychev coefficients, scale them to 50 ohms still at
    # f0= 1Hz
    Li = np.ones(n-2)
    Ci = np.ones(n-1)

    Li[0] = g[2]*Z0
    Ci[0] = g[1]/Z0
    Ci[1] = g[3]/Z0

    print("Scaled_Chebychev_Coefficients_For_LPF:_")
    print("Li: {}".format(Li))
    print("Ci: {}".format(Ci))
    print("\n")

    # change Li into the combination of inverters and capacitors

```

```

# L = CK^2

K = Z0
Cp = np.ones(n)
Invp = np.ones(n-1)
Cp[0] = Ci[0]
Cp[1] = Li[0]/pow(K,2)
Cp[2] = Ci[1]
Invp = Invp*Z0

print("Values for LPF prototype with inverters and no inductors:")
print("Ci: {}".format(Cp))
print("Invi: {}".format(Invp))
print("\n")

Cb = np.zeros(n)
Lb = np.zeros(n)
Lb, Cb = lpf_to_bpf_parallel(Cp, f, bw, n)
print("Values for the Scaled and Frequency shifter BPF prototype
      with inverters:")
print("Lb: {}".format(Lb))
print("Cb: {}".format(Cb))
print("Invi: {}".format(Invp))
print("\n")

C0 = np.zeros(n)
Z = np.zeros(n)

C0, Z = parallel_lc_to_parallel_shunt_and_cap(Lb, Cb, f, n)

print("C0 and Z of parallel Cap and Shunt Lines:")
print("C0: {}".format(C0))
print("Z: {}".format(Z))
print("Invi: {}".format(Invp))
print("\n")

# scale values such that C's match and Z's match
sca = Z[0]/Z[1]
ZI = np.zeros(n-1)
Zii = np.zeros(n)
Cii = np.zeros(n)

ZI[0] = Invp[0]*pow(sca,0.5)
ZI[1] = Invp[1]*pow(sca,0.5)

Zii[0] = Z[0]
Zii[1] = Z[1]*sca

```

```

Zii[2] = Z[2]

Cii[0] = C0[0]
Cii[1] = C0[1]/sca
Cii[2] = C0[2]

print("Inverters, Caps, and Shunts after scaling to match")
print("Cii: {}".format(Cii))
print("Zii: {}".format(Zii))
print("ZI: {}".format(ZI))
print("\n")

# realize the inverters
Zt = np.zeros(n-1)
Cp = np.zeros(n)
Zp = np.zeros(n)

# no changes necessary for the top impedances or parallel
  capacitances
Cp = Cii

Zt[0] = ZI[0]
Zt[1] = ZI[1]

Zp[0] = pow(pow(Zii[0], -1)+pow(-ZI[0], -1), -1)
Zp[1] = pow(pow(Zii[1], -1)+pow(-ZI[0], -1)+pow(-ZI[1], -1), -1)
Zp[2] = pow(pow(Zii[2], -1)+pow(-ZI[1], -1), -1)

print("BPF prototype inverters realized")
print("Cp: {}".format(Cp))
print("Zp: {}".format(Zp))
print("Zt: {}".format(Zt))
print("\n")

# scale every impedance to within range 80 to 100
sc = imp_range/Zp[1]

Zs = np.zeros(n)
Zts = np.zeros(n-1)
Cs = np.zeros(n)

Zs[0] = Zp[0]*sc
Zs[1] = Zp[1]*sc
Zs[2] = Zp[2]*sc

Zts[0] = Zt[0]*sc
Zts[1] = Zt[1]*sc

```

```

Cs[0] = Cp[0]/sc
Cs[1] = Cp[1]/sc
Cs[2] = Cp[2]/sc

Rs = Z0*sc

print("BPF_prototype_inverters_realized_scaled")
print("Cs: \t {}".format(Cs))
print("Zs: \t {}".format(Zs))
print("Zts: \t {}".format(Zts))
print("Rs: \t {}".format(Rs))
print("\n")

K = pow((Z0*Rs), 0.5)
print("K: {}".format(K))

Cb = pow(pow(2*np.pi*f, 2) * (pow(K, 2) - pow(ZL, 2)), -0.5)
Ca = ((-1/(2*np.pi*f*Cb)) / (pow(ZL, 2) + 1 / (pow(2*np.pi*f, 2) * pow(Cb, 2)))) / (2*np.pi*f)

print("capacitor_network_matching_desired_system_impedance_to_
      filter_core")
print("Ca: \t {}".format(Ca))
print("Cb: \t {}".format(Cb))
print("\n")

Cx = np.zeros(n)
Cxs = np.zeros(n-1)
Zx = np.zeros(n)
Zxt = np.zeros(n-1)

Cx[0] = Cs[0]+Ca
Cx[1] = Cs[1]
Cx[2] = Cs[2]+Ca

Cxs[0] = Cb
Cxs[1] = Cb
Zx = Zs
Zxt = Zts

print("Updated_circuit_values_from_matching_inverter")
print("Cx: \t {}".format(Cx))
print("Cxs: \t {}".format(Cxs))
print("Zx: \t {}".format(Zx))
print("Zxt: \t {}".format(Zxt))
print("\n")

```

```

# physical realization and system impedance

n = 1 + Zxt[0]/Zx[0]
k = 1/n

Z02 = n*Zxt[0]
Z01 = n*(Zx[0]*Zx[1]/(Zx[0]+Zx[1]+Zxt[0]))

print("equivalent_combine_sections_calculated_parameters")
print("n: \t{}".format(n))
print("k: \t{}".format(k))
print("Z02: \t{}".format(Z02))
print("Z01: \t{}".format(Z01))
print("\n")

# system impedance estimations
ZS1 = Z01*pow(1-pow(k,2),0.5)
ZS2 = Z02*pow(k,2)/(pow(1-pow(k,2),0.5))

ZS = pow(ZS1*ZS2,0.5)

Z0o = ZS*pow((n-1)/(n+1),0.5)
Z0e = pow(ZS,2)/Z0o

print("system_impedance_approximations")
print("ZS1: \t{}".format(ZS1))
print("ZS2: \t{}".format(ZS2))
print("ZS: \t{}".format(ZS))
print("Z0o: \t{}".format(Z0o))
print("Z0e: \t{}".format(Z0e))

if __name__ == '__main__':
    main()

```