Improving an Algorithm for Quantum Computers

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Introduction

Quantum computers have the possibility to transform the world due to their applications in drug discovery, artificial intelligence, cyber-security, materials science, and more. However, there are still a few hurdles researchers need to cross before quantum computers can revolutionize these fields. One area of active research is to develop quantum algorithms: specifically applying quantum computers to real-world problems. The main hurdle for algorithms is that many require near-perfect machines to achieve a useful result. Because current quantum computers still have a lot of noise, researchers have developed many new algorithms that are useful even with nouse. By simulating different types of noisy quantum computers using high performance computing, this work illustrates what hardware design decisions will enable quantum computers to address more problems.

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Quantum computers get their name from using two, uniquely quantum mechanical behaviors, *entanglement* and *superposition*, neither of which are used in classical computing. Unfortunately, this fundamental paradigm shift empowering quantum computers also introduces substantial complexity when designing and implementing algorithms. A classical algorithm, such as adding two numbers, is built out of collections of classical "gates" (AND, NOR, XOR, etc.) acting on bits. Similarly, quantum algorithms are also composed of gates acting instead on *qubits*. A qubit is a quantum system which contains two states and can be in any superposition of them. Because there are an infinite number of superpositions for a single qubit, quantum gates must precisely set the qubit to the correct state. This poses a challenge as gates are rarely 100% accurate due to unwanted interaction with the environment. Algorithms, which can contain

thousands of gates, are severely impacted by small errors in gates.

Currently, quantum computing is in the noisy intermediate scale quantum (NISQ) [1] era,where noise and errors are still prevalent despite rapid advancement. Many NISQ algorithms call for gates which generate only a small fraction of full entanglement between two qubits. Implementing this type of gate on hardware often requires two to three full entangling gates, causing a significant bottleneck as each gate adds a large amount of error to the algorithm. By optimizing gates at the hardware level, it is possible to implement these fractional gates natively, as with continuous gates [2]. Error divisible gates (EDG) take this a step further by enabling these *fractions of gates* to have *fractions of error* when compared to full entangling gates [3].

In this paper, we demonstrate the superior performance of EDG when applied to a noisy algorithm compared to existing gate protocols. The algorithm we use is the variational quantum eigen solver(VQE).VQE accepts a quantum mechanical model described by a *Hamiltonian* and approximates important values of the model, such as the minimum energy. VQE has received a lot of attention for its strong performance despite large amounts of noise in current NISQ hardware. To begin, we outline VQE and the antiferromagnetic Heisenberg model. Then, using numerical simulation, we show that EDG outperforms existing gate models when used in a VQE calculation and examine future paths of research.

Background

Variational Quantum Eigensolver

By using layers of carefully chosen gates to approximate the ground state of a Hamiltonian of interest, H_P, VQE provides accurate estimates of its ground state energy, even with substantial error and for "difficult" Hamiltonians [4]. A classical optimizer minimizing $E = \langle \psi (T)|H_P|\psi (T)\rangle$ with T as the total run time will then return approximations for the minimum energy. If $|\psi (T)\rangle$ is exactly prepared as the ground-state, E will be the exact minimum energy, but this is unlikely in practice due to noise. We approximate $|\psi(T)\rangle$ by evolving under N discrete time steps, with state evolution given by

$$|\psi(t+dt)\rangle \approx e^{-idtH(t)}|\psi(t)\rangle, \qquad (1)$$

where $dt=T/N$. We choose $H(t)=(1-t/T)H_S+ (t/T)H_P$, with a Hamiltonian H_S with a simple ground state, and the problem Hamiltonian.

These choices have achieved good results in VQE calculations without the added complication of large parameter spaces [4], motivating optimizing over only two parameters: the total run time T and the number of layers N.

Antiferromagnetic Heisenberg Model

We used VQE to find the ground state energy of the 1D antiferromagnetic Heisenberg model of interacting spins,

$$H_P = \sum_{i=0}^{N_{qb}-2} (\sigma_i^x\sigma_{i+1}^x + \sigma_i^y\sigma_{i+1}^y + \sigma_i^z\sigma_{i+1}^z), \quad (2)$$

with the number of qubits used in the algorithm, N_{qb}, chosen to be even. This is a many-body problem which, while analytically solved in 1D by the Bethe ansatz, is an active area of research for more interesting connectivities, such as frustrated lattices in 2D [5]. This problem is therefore an interesting candidate to demonstrate the benefit of EDG for noisy quantum algorithms.
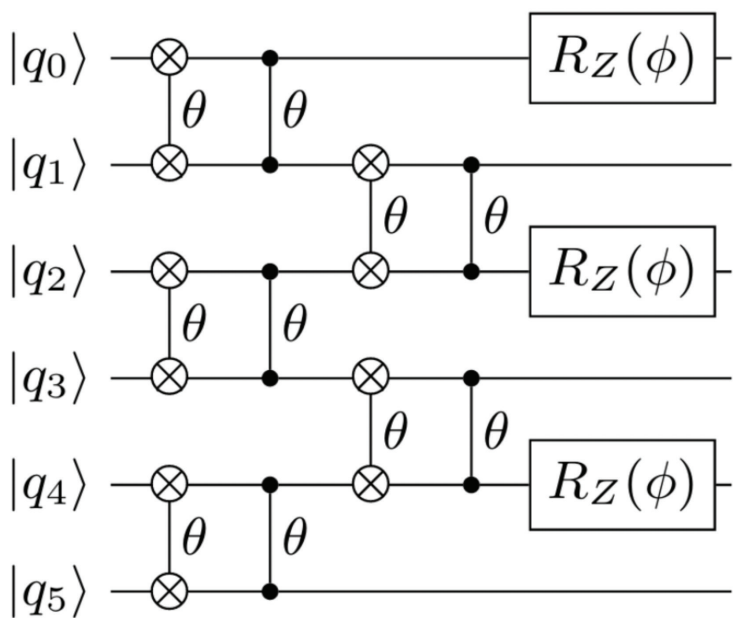

Figure 1 *Quantum circuit diagram for a single layer of VQE with N_{qb}=6. The partial iSWAP and controlled phase gates implement the H_P evolution, while the Z rotations implement the H_S evolution.*

Methodology

For our simple Hamiltonian, we set

$$H_S = \sum_{i \text{ even}}^{N_{qb}-1} \sigma_i^z. \qquad (3)$$

Additionally, implementing equation (1) on physical hardware requires additional approximation. Here we use the the Trotter decomposition [6]

$$e^{-idt(A+B)} = e^{-idtA}e^{-idtB} + O(dt^2). \qquad (4)$$

The circuit from this decomposition is shown in Figure 1.

The optimizer chooses values of N and T in the ranges [2,20] and [0,10N], respectively. We assumed that the primary errors could be modeled as depolarizing noise at a rate of 1% for a two-qubit gate and 0.1% for a one-qubit gate, similar to current error rates of superconducting qubit hardware [7]. The simulations were run using density matrix simulations in QuEST [8], using NLopt's NLOPT_GN_CRS2_LM global optimization routine [9] [10]. To compare EDG and current gate protocols, we ran the VQE calculation in three regimes:

> **1. Stock gate set:** Partial gates *are not* native to the hardware, requiring approximately 4 single-qubit gates and 2 two-qubit gates [3]. Effective 2.4% error rate for two-qubit gates.
>
> **2. Continuous gate set:** Partial gates *are* native to the hardware, requiring only 1 gate. Effective 1% two-qubit error rate [2].
>
> **3. Error divisible gate set:** EDGs are native, resulting in the gate error being proportional to the fraction of gate applied [3].

Results

In Figure 2, the EDG set clearly outperforms the other gate sets. In particular, Table 1 demonstrates the EDG set is optimal with larger N, using more VQE layers. These results validate the noise-free intuition that VQE algorithms find the ground state when applying numerous, small fractions of gates.

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However, it is only in the EDG set where the benefit of increased N outweighs the penalty of having more gates total. With the two other gate types, too many applications proliferates errors, so the optimum number of layers is $N = 2$, the minimum allowed circuit depth.
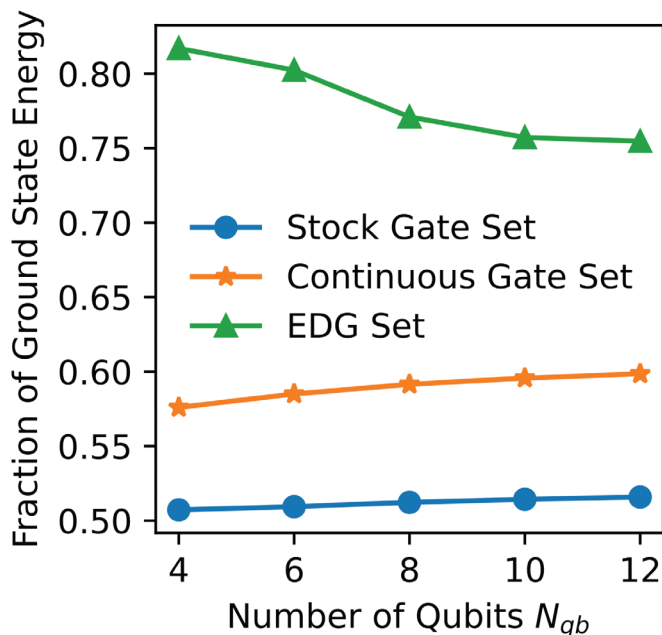
Future Work and Conclusions

In the future, we aim to run VQE using EDG on physical hardware. There will presumably be difficulties in its implementation that could impact the ability for VQE to succeed. How the simplistic noise model used in the simulation compares to the performance on hardware is of interest as well. We would also like to observe the optimal choices for the parameters T and N, when in the presence of increased hardware complexity.

***Figure 2** Fraction of ground state achieved for different error regimes.*

	$N_{qb} = 10$		$N_{qb} = 12$	
	T	N	T	N
Stock Gate Set	11.79	2	0.76	2
Continuous Gate Set	11.80	2	11.81	2
EDG Set	2.06	10	1.894	8

Table 1 *Optimum values for T and N for N_{qb} = 10,12 as found by VQE.*

We demonstrated how a current quantum algorithm's performance can be increased drastically through hardware improvements.

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EDG was initially proposed to take advantage of the small fractions of full gates present in current NISQ algorithms, even before fault-tolerance. Beyond VQE calculations, an EDG set as described here will likely report better results for "deep" circuits. Further advancements in algorithm design and hardware design, as well as continued collaboration will continue to evolve the capabilities of algorithms and nourish the second coming quantum revolution.

Paul Varosy graduated from Mines with a B.S. in Engineering Physics and minors in Quantum Engineering and Mathematical Sciences in 2023. He started performing research through the First-Year Innovation & Research Scholar Training (FIRST) program. This sparked Paul's love for quantum information science, where he participated in projects across quantum algorithms, benchmarking, and superconducting circuits with Prof. Eliot Kapit in the Physics department. As a result of this research, he was awarded the prestigious Goldwater and Astronaut Scholarships. He will continue researching experimental quantum information by pursuing a Ph.D. in Applied Physics at Stanford University.

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