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APPLICATIONS OF SOLID STATE AND INTEGRATED CIRCUIT TECHNOLOGY TO MULTICHANNEL ANALYZERS

By

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ABSTRACT

This thesis describes some of the necessary circuits for use in a multichannel analyzer; in particular those circuits needed in a pulse height analyzer and Mössbauer data analyzer are described. The circuits that concern a pulse height analyzer are a serial shift register memory, a timing and synchronization circuit, and an analog pulse stretcher circuit. The circuits that could be used in a Mössbauer data analyzer are a parallel shift register memory, a timing and synchronization circuit, and a memory address selector. A high frequency voltage follower circuit is also described; this circuit could be used as a buffer stage or in a sample and hold application. Finally, the implementation of these circuits in both types of analyzers is discussed.

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CHAPTER 1

INTRODUCTION

This thesis treats the development of some of the circuits required for a multichannel analyzer. Initially these circuits were to be applied to a Mössbauer data analyzer for research that Dr Joseph A. Moyzis, Jr , was conducting at the time. The organization of the memory, timing and synchronization, and memory address selector are all based upon the criteria of Dr. Moyzis. Approximately midway in the development of the Mössbauer data analyzer, Dr Moyzis left the Colorado School of Mines; consequently, there was no longer a need for a Mössbauer data analyzer.

The pulse height analyzer research and design was started in an effort to develop a useful tool and to minimize the time lost in the development of the Mössbauer data analyzer. The memory configuration, pulse stretcher, and the timing and synchronization circuit have been developed and tested for the pulse height analyzer The pulse height analyzer is to have 100 channels capable of storing 10^5 counts per channel with input pulses from 0 to 10 volts high and 0.5 μs wide.

Chapter 2 deals with solid state shift register memories. This type of memory was selected because of its low cost and high flexibility. The memory may be used either as a small serial type memory or as a large parallel type memory. The memory has the capability of addition

of counts, subtraction of counts, readout for an analog display, and readout for a numeric display. Finally, there is an explanation of how the memory is applied in a Mössbauer data analyzer and in a pulse height analyzer.

Chapter 3 describes the timing and synchronization circuits for a pulse height analyzer and a Mössbauer data analyzer. These circuits provide the two-phase clocks for the memory, the preset load command, and the count enable command. The timing and synchronization circuit for the pulse height analyzer allows a maximum of one count to be added into the memory per address; this circuit is compared with the timing and synchronization circuit for the Mössbauer data analyzer, which accumulates more than one count in the memory per address. The timing and synchronization circuit allows the memory to be digitally synchronized with other circuits for added stability.

The pulse stretcher circuit is described in Chapter 4. This circuit, which is used only in a pulse height analyzer, accepts a 0 to 10 volt pulse of 0.5 μs minimum duration and stretches it for 0.2 ms maintaining a linear relationship between the input and output voltages.

The memory address selector, as described in Chapter 5, was designed for use in a Mössbauer data analyzer. This circuit selects the the part of the memory within which data are to be stored. The circuit cycles the memory at a high shift frequency until the start location in the memory is reached; the circuit then cycles the memory at a slower shift frequency through the addresses where data are to be stored; finally the circuit cycles the remaining addresses in the memory at

the high shift frequency. This circuit minimizes delays inherent in using one part of a large shift register memory.

Chapter 6 discusses a high frequency voltage follower This circuit was developed for the pulse stretcher circuit; however, the final version of the pulse stretcher did not require the high frequency voltage follower. This circuit accepts a 0 to -5 volt signal and has a bandwidth of 5 MHz.

Chapter 7 is a block description of a pulse height analyzer and shows the application of the circuits that have been developed for the pulse height analyzer. The description also explains the circuits that have to be developed to make a working pulse height analyzer

Chapter 8 deals with a Mössbauer data analyzer and explains how the circuits that have been developed would be used in a Mössbauer data analyzer. The description also outlines the circuits needed to make a complete Mössbauer data analyzer.

CHAPTER 2

SOLID STATE SHIFT REGISTER MEMORIES

Theory of Operation:

Shift Registers: A shift register can be analyzed as a series of J-K flip-flops.[§] Figure 1 gives a block diagram of a shift register composed of J-K flip-flops, and the waveform for the shift pulse.

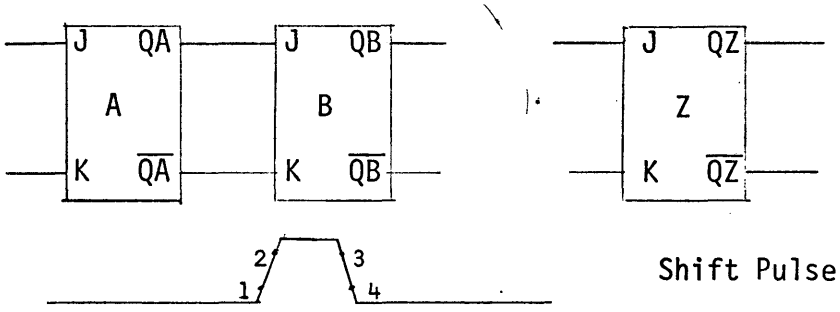


Figure 1

The operation of a shift register begins at point 1 of the shift pulse; at this point the slave is isolated from the master. At point 2 the values of QA and $\overline{QA}$ from flip-flop A are entered into the master of flip-flop B by way of the J and K inputs of B. This sequence also occurs in the remaining flip-flops, each receiving the data from the previous stage. At point 3 the J and K inputs are disabled, and the values of J and K are locked into the master. At point 4 the information stored in the master is transferred into the slave. The QB and $\overline{QB}$ outputs of the B flip-flop

[§]See Appendix.

now assume the value that QA and $\overline{QA}$ had before the shift pulse arrived. Data are entered into the shift register through the J and K inputs of flip-flop A in a manner similar to the way that data are entered into flip-flop B from flip-flop A. Data are read out of the shift register through the QZ and $\overline{QZ}$ outputs of flip-flop Z. Therefore, in the operation of a shift register data which are entered into the shift register are remembered for as many shift pulses as there are flip-flops, and these data constitute the output of the last flip-flop.

Shift Register Memories: A shift register can be used as a drum type memory device when the shift register is connected in a recirculating loop. This recirculation is accomplished by connecting the last flip-flop's outputs, QZ and $\overline{QZ}$, to the J and K inputs of the A flip-flop. When connected in this manner the data, which have gone through the entire memory and are now at QZ and $\overline{QZ}$, reenter at the beginning of the memory. The data then recirculate through the memory.

The primary difficulty with a memory of this type is the entry and retrieval of the data stored within the memory. This difficulty is overcome by inserting in the feedback loop of the shift register a device to read out of or write into the shift register. This device allows the data to be entered into, changed within, and read from the memory.

This type of memory does not allow the random access of any address, as would be possible with a random access memory. The shift register memory must in general be cycled whenever an address is to be accessed. In large shift register memories the inherent delays become a real problem. The means to circumvent this problem are explained in the section entitled Memory Address Selector.

General Purpose Shift Register Memory Card:

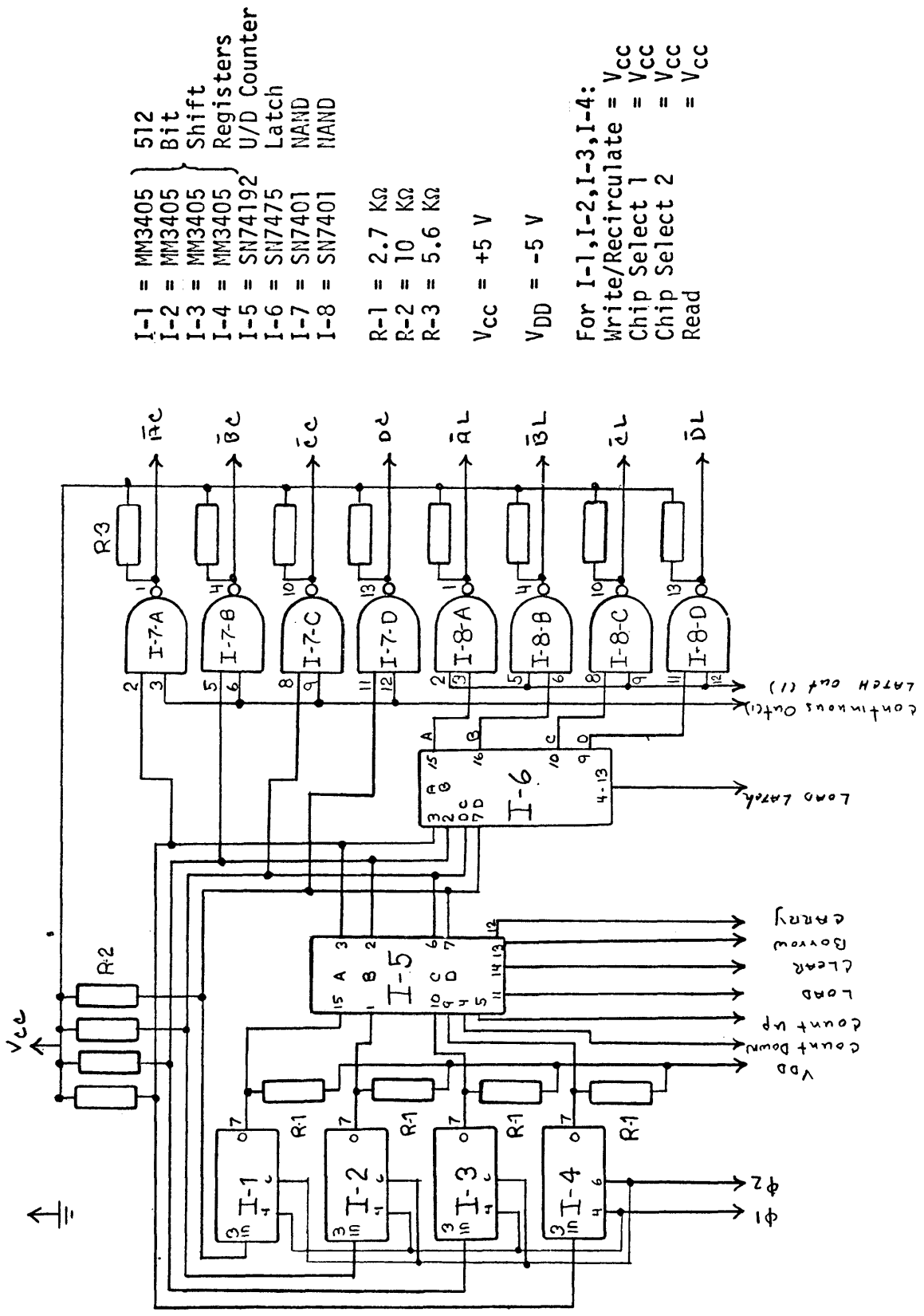
Description of the Memory Card: The shift register memory card is illustrated in Figure 2. The design of the memory is based on a binary coded decimal (BCD) format. The memory uses four 512-bit shift registers and one up-down presetable counter as the computation device. At some location in one shift register one of the four necessary BCD bits which constitute a decimal number is stored. The four shift registers then store one complete decimal digit in BCD.

The shift registers require a two-phase clock input. The two-phase clock shifts the register and also enables the read and the write operation. The output clock is $\Phi 1$; data are read out from the shift register on a low-to-high transition of the $\Phi 1$ clock. The input clock is $\Phi 2$; data are read into the shift register on a low-to-high transition of the $\Phi 2$ clock. External to the memory there is a timing and synchronization circuit that generates the two-phase clock pulses. These pulses are timed according to the application that the memory must serve.

The outputs of the shift registers I-1, I-2, I-3, and I-4 are connected to the A, B, C, and D preset inputs of the counter, I-5. The A, B, C, and D outputs of the counter are fed back to the inputs of the shift registers, I-1, I-2, I-3, and I-4 respectively.

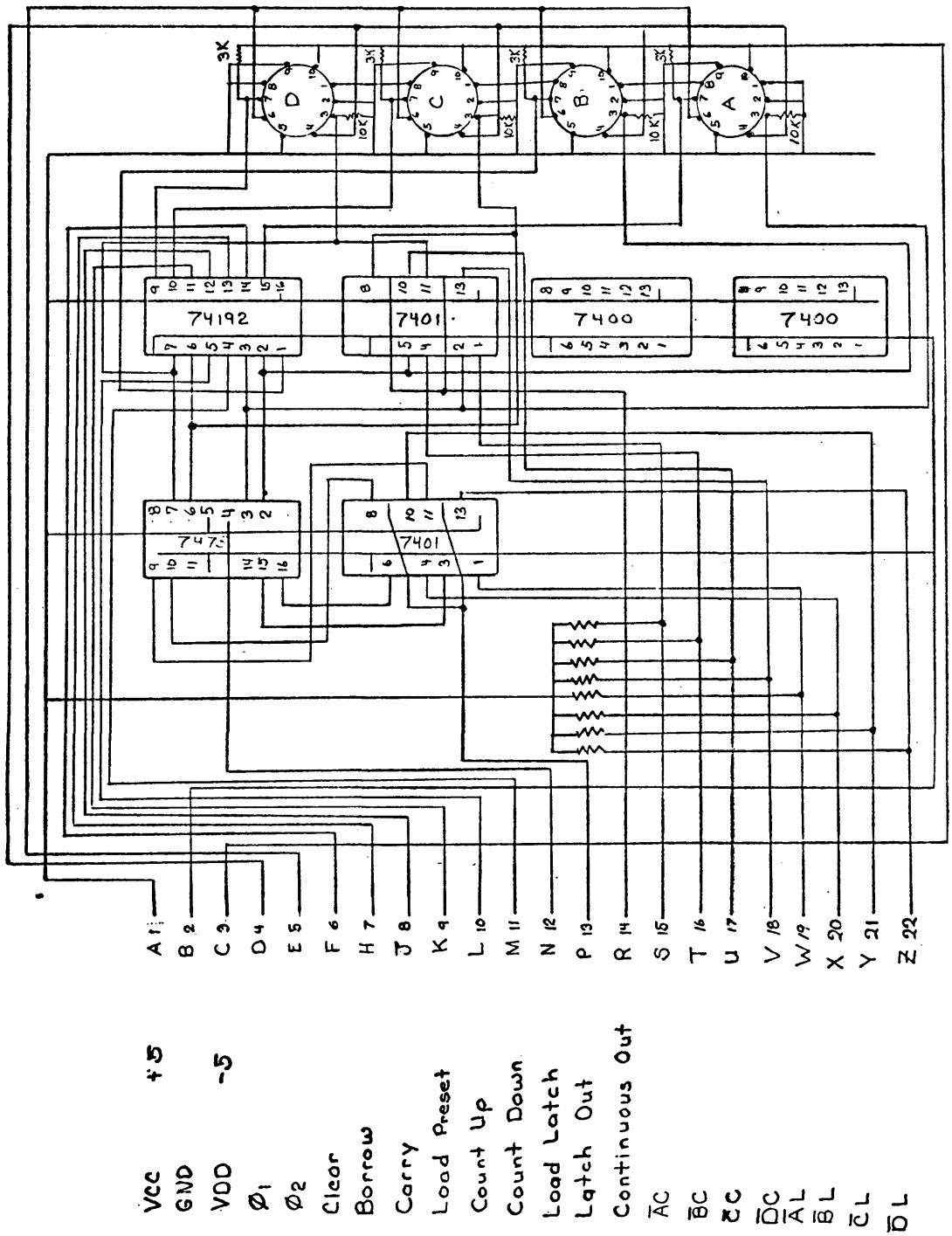
By placing the counter in the feedback loop for the recirculating shift register, data can be entered into, cleared from, changed within, and read out of the shift register.

Data are entered into and changed within the shift register in the following sequence. A low-to-high transition of the output clock $\Phi 1$ causes the values of the n-th bits from I-1, I-2, I-3, and I-4 to appear



Shift Register Memory Card Logic Diagram

Figure 2



Memory Card Layout

Figure 2-A

at the outputs. These four outputs, which constitute one decimal digit, are used to load the preset counter. The counter will now either count up (add counts) or count down (subtract counts) according to a predetermined command from an external switch. After a predetermined time the input clock Φ2 then loads into I-1, I-2, I-3, and I-4, the four BCD outputs of the counter. The shift register then shifts to location n+1 and the sequence begins again.

To clear memory requires only that the clear be enabled in the counter. Then, as the register shifts, only zeros can be entered because the clear holds the output of the counter at zero. Consequently, only zeros are written into the shift register.

If there is no count pulse (command) present the preset counter's output will assume the value of the preset input. The counter will not change value, and the shift registers will behave as a recirculating memory. This mode is ideal for storage of information, as well as for reading out of the memory. The read-out process is non-destructive and allows for the sampling of data while the memory is cycling.

Included on the memory card are two means for data output; there are a continuous output and a latched output. When enabled the continuous output reads out the instantaneous value of the counter in BCD. This type of output would typically be used for a cathode ray tube (CRT) display. Here the continuously changing output from the counter will be applied to the input of a digital-to-analog converter, and the output of the digital-to-analog converter will then give a continually changing analog output of the memory. The latched output assumes the value of the counter output when the latch pulse is received, and stores this

value until the next latch pulse is received. When the latch output is enabled the value of the counter output at the time of the latch pulse is then provided. This type of readout would be used for a numerical tube or teletype output, where the output must be present for a period of time longer than is required by a CRT display.

Both the latched and the continuous output are of a bussed configuration. In unbussed memories that require many cards there are necessarily four output wires from each card. By using the output bus and strobing the output gates of the memory card there are only four output lines for the entire memory and one strobe line for each card. This reduces the backpanel wiring and simplifies the actual hand wiring. The output gates for the memory are open-collector 2-input NAND gates. One input of the NAND gate is from the counter, in the case of the continuous output, or from the latch, in the case of the latched output. The other input to the NAND gate is one of the strobe inputs for the card. When the strobe input is at logic level "1" then the output of the NAND gate is the complement of the other input to the gate. When the strobe input is at logic level "0" then the output of the NAND gate is at logic level "1" independently of the other input. The open collector gates can have their outputs paralleled to give the wire AND-function. This feature allows implementation of the BCD output bus and reduces the output-line requirement. The output is the complement of the BCD code.

IC Shift Register: The shift register chosen for the memory application is a Monolithic Memories, Inc. MM3405. It is a 512 bit recirculating dynamic shift register. This integrated circuit features

a wide operating frequency range of 30 Hz to 4 MHz. The slow shift frequency in many applications is quite advantageous. The MM3405 is a silicon gate metal oxide semiconductor device; however, it is easily interfaced with the standard TTL logic by use of some external resistors. The write/recirculate and read controls and chip select gates were not used in the present application. An important characteristic of the shift register in designing interface circuits to TTL logic is the large clock capacitance of 80 pf This affects the level translators because they must be capable of driving capacitive loads.

Conditions of Test

Input rise and fall times: 10 nsec
Output load is 1 TTL gate

Timing Diagram

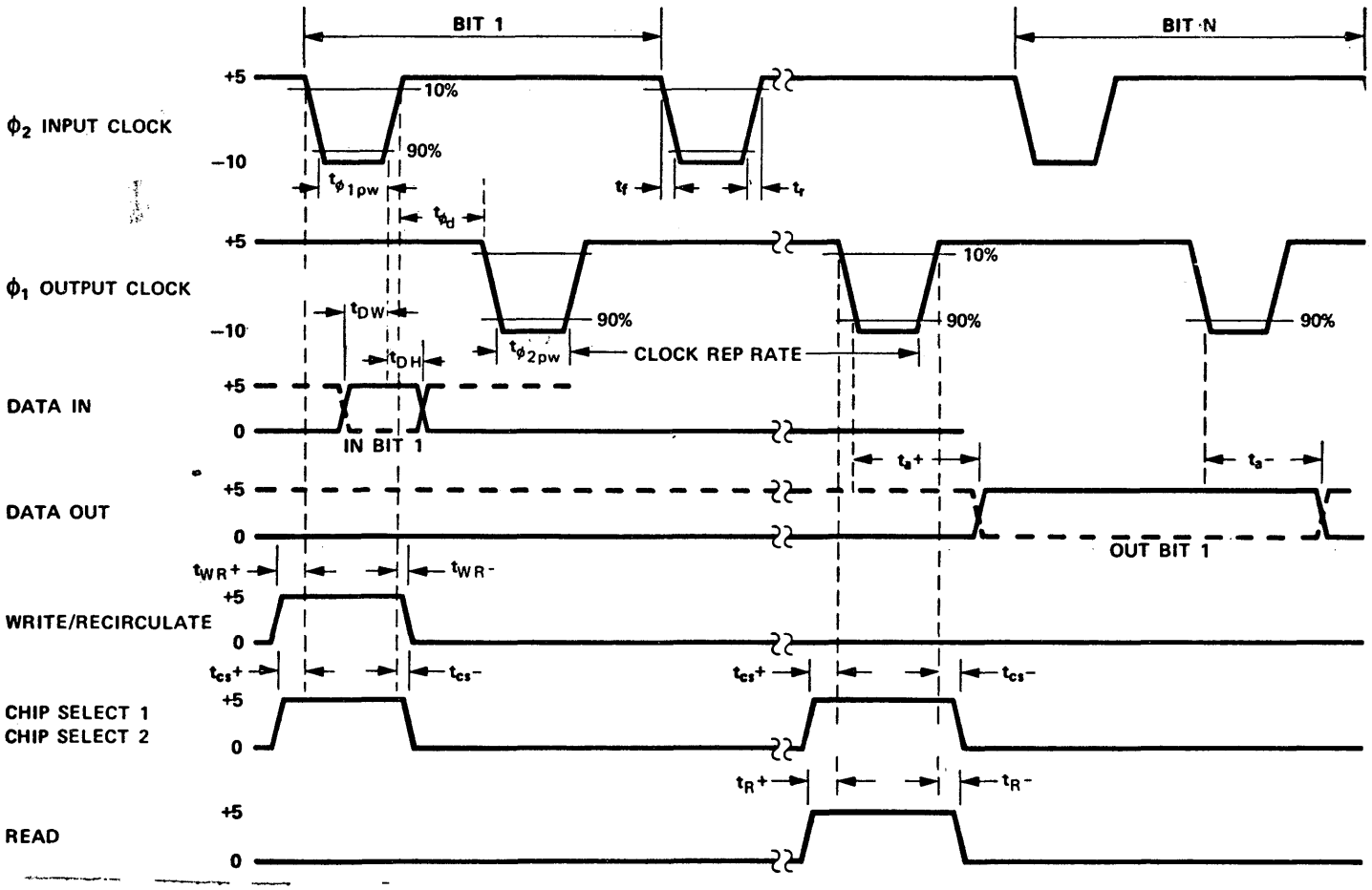


Figure 3

The Timing Diagram for the shift register is given in Figure 3(1) Clock pulses shown here are produced by the Level Translator.

Additional AC characteristics for the shift registers are given in Table 1(2)

A.C. Characteristics

$T_{Case} = -55°C$ to $+85°C$; $V_{CC} = +5V \pm 5\%$; $V_{DD} = -5V \pm 5\%$; $V_{ILC} = (V_{CC} - 14)$ to $(V_{CC} - 17)$; $R_L = 3K$; $C_L = 20pf$; 1 TTL Load; 36% Duty Cycle unless otherwise noted.

SYMBOL	TEST	MIN.	MAX.	UNIT	CONDITIONS
FREQUENCY	CLOCK & DATA REP RATE	200 Hz @25°C Note 1	2	MHz	
$t_{\phi pw}$	CLOCK PULSE WIDTH	0.180	10	μsec	
$t_{\phi d}$	CLOCK PULSE DELAY	30		nsec	
t_r; t_f	CLOCK PULSE TRANSITION		1	μsec	
t_{DW}	DATA WRITE (SET-UP) TIME	100		nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	20		nsec	
t_{a+}; t_{a-}	CLOCK TO DATA OUT DELAY		250	nsec	
t_{R-}; t_{CS-} t_{WR-}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		nsec	
t_{R+}; t_{CS+} t_{WR+}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		nsec	
C_{in}	INPUT CAPACITANCE		5	pF	@ 1 MHz; $V=V_{CC}$; v=250mV p-p
C_{out}	OUTPUT CAPACITANCE		5	pF	@ 1 MHz; $V=V_{CC}$; v=250mV p-p
$C\phi$	CLOCK CAPACITANCE		80	pF	@ 1 MHz; $V=V_{CC}$; v=250mV p-p

Table 1

• One additional factor contributing to the selection of these shift registers is the cost per bit. The cost of one cent per bit makes the shift register memory very attractive, and the fact that the memory does not permit random access can be tolerated.

IC Counter: The counter used in the feedback loop of the shift register is a Texas Instruments SN74192, which is a synchronous 4-bit up/down counter. The SN74192 is a preset counter, required in the memory

application in which the shift register must load the counter. The counter is also an up/down counter, which gives the memory the capability of both adding counts into and subtracting counts from the memory. This is particularly useful in a pulse-height analyzer because it provides a convenient method for subtracting background counts, subtracting spectra, etc.

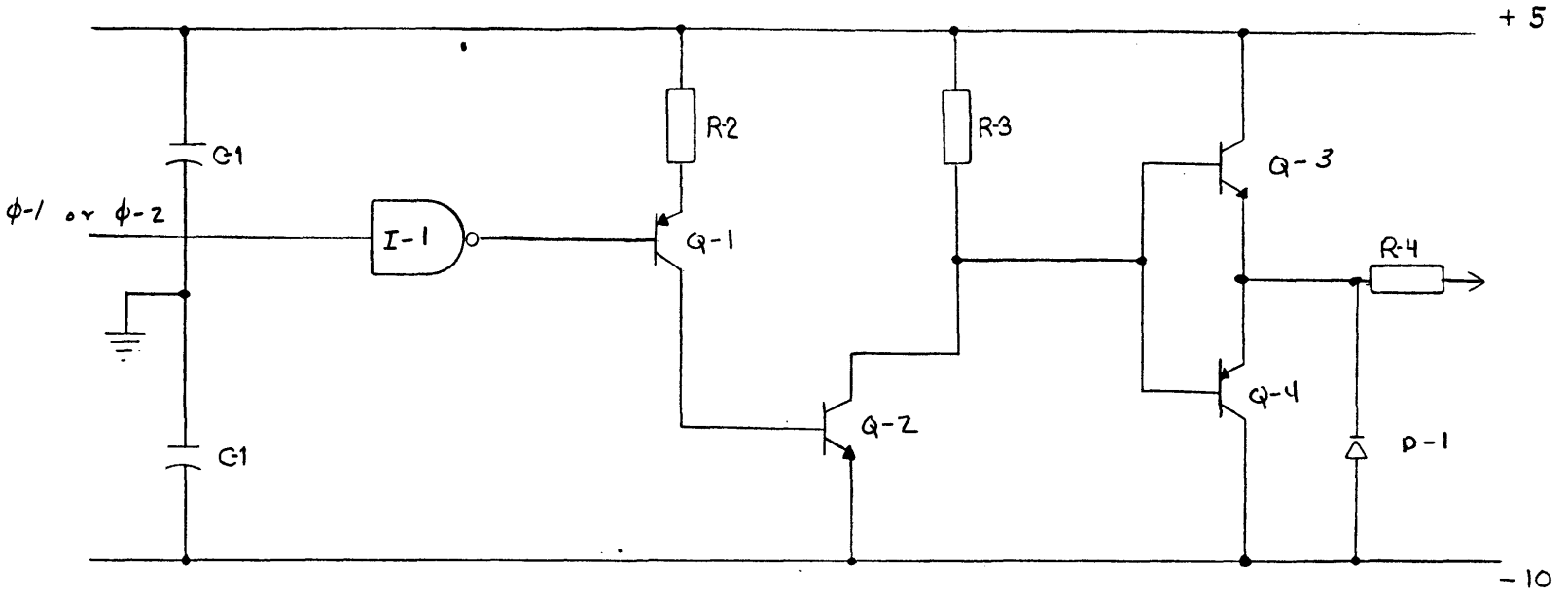
The high clear input forces all outputs to be low, independently of the count and preset inputs. The counter has both borrow and carry outputs for easily cascading the stages. There are two count inputs provided. The direction of counting is determined by which count input is pulsed. The SN74192 greatly increases the flexibility of the memory for the nominal cost of $1.92.

Level Translator:

Introduction: The shift registers require a two-phase clock input for shifting, data input, and data output. The logic determining the timing and synchronization of the two-phase clock depends upon the application of the shift register. The use of the transistor-transistor logic (TTL) for the two-phase clock would limit the output voltage of this circuit to standard TTL levels, approximately 0 volts and +5 volts. The MM3405 shift registers require a two-phase clock voltage swing of -10 volts to +5 volts. This necessitates the use of a level translator which will translate the TTL levels of 0 and +5 volts to -10 and +5 volts respectively. The clock input for an MM3405 has a predominently reactive input whose capacitance is 80 pf.

Description of Operation: The level translator is shown in Figure 4. I-1 represents a standard TTL gate. The actual input of the level translator is Q-1; the operation is more easily followed, however, by including the gate in the discussion. When the input of I-1 is at logic level "1" the output of I-1 is at logic level "0" Logic level "0" is approximately 0 volts. With 0 volts applied to its base Q-1 conducts. Transistor Q-1 is the source of sufficient current to saturate transistor Q-2. When transistor Q-2 saturates, it applies -9.5 volts to the base of the complementary emitter follower consisting of Q-3 and Q-4. The output voltage is approximately -10 volts under these conditions.

If the input of I-1 is at logic level "0" the output of I-1 is at logic level "1" Logic level "1" is approximately equal to +5 volts, and +5 volts applied to the base of transistor Q-1 will turn off Q-1



I-1 = SN7400 (Typical TTL Gate)

Q-1 = SM7557H	R-2 = 470Ω	C-1 = .1 mfd	D-1 = General Purpose Silicon Diode
Q-2 = MPS 3446	R-3 = 150Ω		
Q-3 = MPS U02	R-4 = 100Ω		
Q-4 = MPS U52			

Level Translator

Figure 4

With transistor Q-1 off there is no base current for Q-2; Q-2 is consequently turned off The collector of Q-2 is now at +5 volts. The +5 volts is applied to the base of the complementary emitter follower, giving an output voltage of the level translator of approximately +5 volts.

The complementary PNP-NPN emitter follower allows the level translator to actively pull the output to either +5 volts or -10 volts.

Design Considerations: Resistor R-2 is 470 ohms and has a potential difference of 4.5 volts across it when transistor Q-1 is conducting. The collector current of Q-1 is approximately 10 mA.

Q-2 is an NPN, high speed, saturated switching transistor. Q-2 is a type number MPS3646, which has switching times of 25 ns for time to turn on and 35 ns for time to turn off The forward current gain h_{fe} has a minimum value of 30.

For transistor Q-2 with a base current of 10 mA and an h_{fe} of 30, saturation results for

$$50\Omega < \text{R-3}.$$

Another constraint on transistor Q-2 is the maximum collector current. This current is 300 mA; R-3 has to be large enough that this current limit is not exceeded. The value of R-3 in the actual circuit is 150 ohms, which satisfies both of the above constraints.

The capacitors C-1 are used to bypass the power supply lines. These provide transient operating current to the translator which could not be provided by the power supply because of inductive leads They also reduce feedback between stages and reduce the tendency to

oscillate. Without diode D-1, the output of the level translator has some ringing following a pulse transition. Diode D-1 is inserted between the output of the level translator and the -10 volt supply and decreases the amount of ringing. If the output of the level translator falls below -10 volts in potential the diode D-1 is forward biased and conducts. The ringing, which would go below -10 volts, forward biases diode D-1; the diode consequently quickly drains the energy out of the stray capacitance and inductance which are causing the ringing.

Resistor R-4 is suggested by the manufacturer of the shift registers as an interfacing stage between the level translators and the shift registers' clock inputs.

The complementary emitter follower Q-3 and Q-4 will have to charge the clock capacitance of the shift registers through resistor R-4. The R-C charging time will determine the number of shift registers that may be driven by the level translator. From Figure 3 and Table 1 the maximum allowable clock pulse transition time is 1 μs for a transition of the clock of 90% of the final voltage. A 90% transition corresponds to approximately three R-C time constants. Therefore

$$3\{R\text{-}4\}\{C_{clock}\}\{n\} < 1\ \mu s,$$

where C_{clock} = 80 pf/shift register, n = the number of shift registers, and R-4 = 100 Ω. Consequently, n is approximately equal to 40, and the level translator should be able to drive about 40 shift registers.

Applications of the General Purpose Memory:

Serial Memory: In a serial BCD memory data may be stored in a horizontal stack. The A bit of each coded decimal digit is stored in shift register I-1; similarly, the B bit is in I-2, C is in I-3, and D is in I-4.

To store a five decimal digit number in the serial memory the 10^0 decimal digit is stored in bits 1 of shift registers I-1, I-2, I-3, and I-4; similarly, the 10^1 digit is in bits 2, the 10^2 digit is in bits 3, the 10^3 digit is in bits 4, and the 10^4 digit is in bits 5 of the shift registers I-1, I-2, I-3, and I-4. The address number 0 consists of bit numbers 1 through 5 of the four shift registers. Bit numbers 6 through 10 constitute address number 1, etc.

A memory of 100 addresses capable of storing a five digit number in each address requires one memory card. The size of the memory is determined by the size of the shift registers used on the card. For 512-bit shift registers the above memory has 12 extra bits which can be used to store additional data.

Table 2 better illustrates the serial memory configuration. In actual operation if a count is to be added in address 1, then when shift register bit #6 is reached and the output clock has loaded the preset counter, a pulse is applied to the input of the counter, increasing decimal bit 10^0 by 1 The input clock then loads the new bit #6 into the shift registers. The carry output of the counter then is sensed as to whether a count should be added to the bit #7, the 10^1, of address #1. If so, the above process is followed; if not, there is no pulse to the counter, and the value of bit #7 does not change.

TABLE 2

Serial Memory Organization

Shift Register Bit #	I-1 BCD-A	I-2 BCD-B	I-3 BCD-C	I-4 BCD-D	
1				10^0	Address #0
2				10^1	
3				10^2	
4				10^3	
5				10^4	
6				10^0	Address #1
7				10^1	
8				10^2	
9				10^3	
10				10^4	
.				.	
.				.	
.					
496				10^0	Address #99
497				10^1	
498				10^2	
499				10^3	
500				10^4	

A similar procedure is followed to subtract counts; however, the borrow is now sensed rather than the carry.

The timing and generation of the pulse is carried out by the timing and synchronization circuit.

Parallel Memory: In a parallel BCD memory the data are stored in a vertical stack. This memory configuration requires more than one memory card. It requires one memory card per decimal digit of the number to be stored. Therefore, if a number of order five is to be stored, then five memory cards are needed.

Each card in the memory stores one complete digit. I-1 stores the A bit, I-2 the B, I-3 the C, and I-4 the D. The 10^0 are stored in card 1, the 10^1 in card 2, the 10^2 in card 3, 10^3 in card 4, and 10^4 in card 5. Address #0 comprises bits #1 on all cards, address #1 comprises bits #2 on all cards, etc.

The cards are chained together to form the vertical stack. The size of the number to be stored is determined by the number of cards; the number of addresses is determined by the size of the shift register.

This memory configuration presents the various digits of a number stored in a given address simultaneously. The count pulses are applied to the input of the unit's decade memory card. The ten's decade memory card receives its input from either the borrow output of the unit's card if the counts are to be subtracted or the carry output of the unit's card if the counts are to be added. This scheme is continued for as many decades as necessary in the memory.

The strobe output feature is particularly useful for this memory configuration. The number of cards needed to store a large number dictates the necessity for a bussed output.

This memory configuration allows for easily expanding the memory capability, that is, the magnitude of a number that can be stored. This expansion is accomplished by simply adding more cards to the memory. The expansion of the address capability of the memory requires the addition of more shift registers to each card. This is the same type expansion difficulty as would be found in a serial application of the general purpose memory.

The parallel memory configuration is useful for large memories because the time needed to load the memory is on the order of 50 ns for a five digit number. This time is determined by the response time of the SN74192 decade counters. The time needed to load a similar number in a serial memory is 2.5 μs. This time is determined by the maximum shift rate of the MM3405 shift registers.

CHAPTER 3

TIMING AND SYNCHRONIZATION CIRCUIT

Introduction:

As indicated in the section entitled Shift Registers, the two-phase clock determines the reading into and writing out of memory. The most accurate and reliable means for generating the two-phase clock signals is digitally. This method, as opposed to a method which relies upon an R-C timing network to generate the timing and synchronization necessary for the shift registers, is more precise and allows for definite time synchronization.

The input to the timing and synchronization circuit is a master clock. This clock provides the pulses that the timing and synchronization circuit counts in order to generate the correct pulse train for the shift registers. Any error introduced by the master clock may change the read-in time, or write-out time, etc. This error will not change the synchronization given by the pulse train.

Pulse Height Analyzer:

Circuit Requirements: Figure 5 shows a timing and synchronization circuit appropriate for application in a pulse height analyzer. The function of this circuit is to generate the proper pulse train for the two-phase clock, preset load command, count enable command and the add/subtract 1 count to memory command. A characteristic of the pulse height analyzer is that only one count per address may be added per cycle of memory. The timing and synchronization circuit must provide for this feature.

The pulse train sequence is depicted in Figure 6. The required sequence is one in which the low-to-high transition of the Φ1 clock, the output clock of the shift register, occurs within the command to load the preset counter. The count enable and the add 1 count occur after the preset counter has been loaded. The count input and the preset load are disabled when the Φ2 clock, the input clock of the shift register, makes its low-to-high transition.

Circuit Operation: The input to the circuit is the square wave generated by the master clock. This square wave is a 10 MHz signal that is applied to the input of I-1-B, J-K flip-flop. The J and K inputs of the flip-flop are connected to the $+V_{cc}$ This connection makes the flip-flop change states on each clock pulse. The B output of I-1-B is the clock input for another J-K flip-flop, I-1-A, also connected to toggle. I-1-B divides the master clock by two, and I-1-A divides the output of B by two; the output of the master clock is, therefore, divided by four.

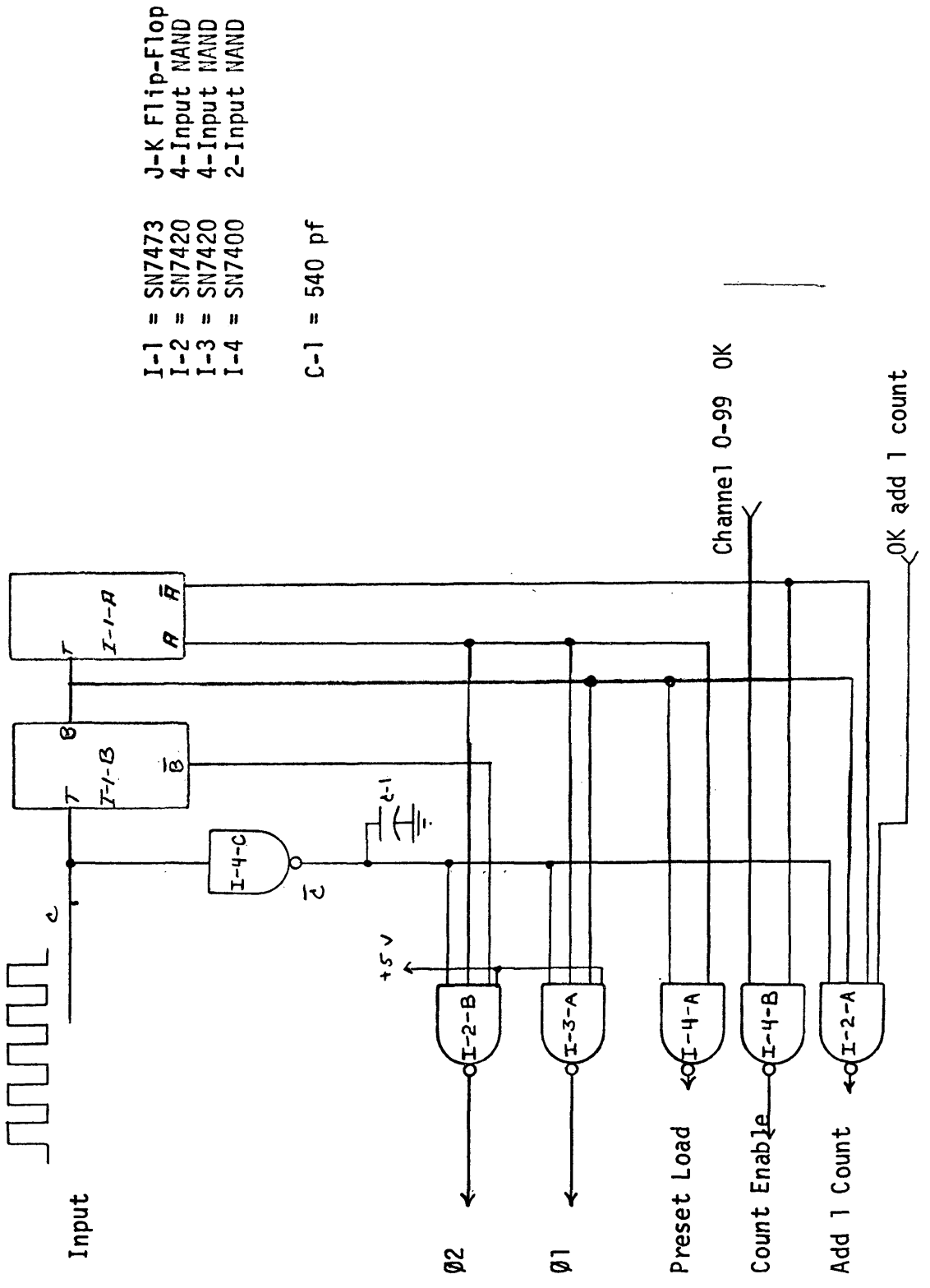


Figure 5

Timing and Synchronization Circuit (Pulse Height Analyzer) - Logic Diagram

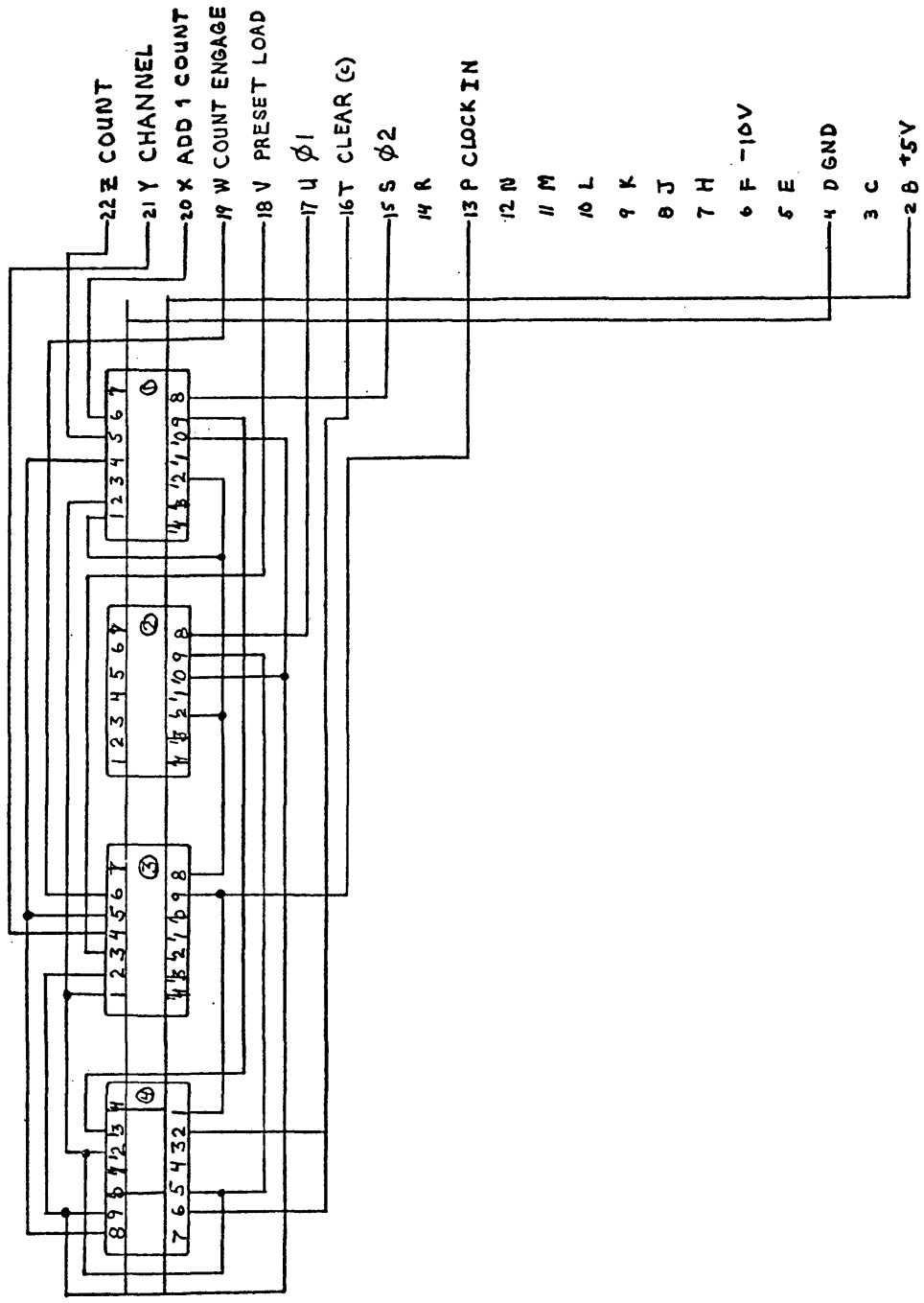
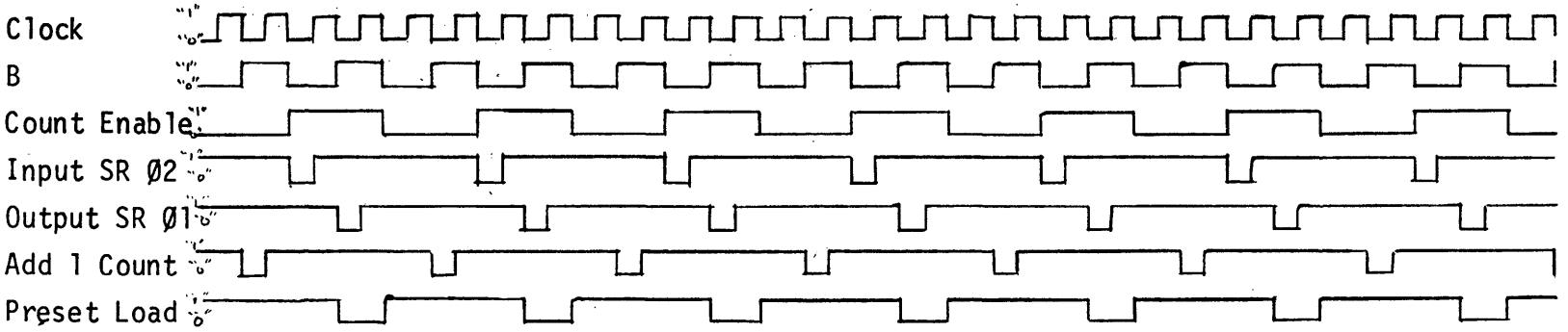


Figure 5-A

Timing and Synchronization Circuit (Pulse Height Analyzer) - Layout



Pulse Train Sequence For Pulse Height Analyzer

Figure 6

I-4-C is a NAND gate used as an inverter; it inverts the signal from the master clock. The output signal from the master clock is hereafter referred to as C.

The preset load command must have enabled the counter's preset load when the $\Phi 1$ clock makes a low-to-high transition. It is therefore advantageous for the preset load to be enabled slightly before the low-to-high transition of the $\Phi 1$ clock and remain for a period of time after this transition. The counter input must also be disabled throughout this time. The Boolean expression for the $\Phi 1$ clock can be seen from Figure 5 to be

$$\Phi 1 = \overline{\overline{C} \cdot B \cdot A}.$$

The preset load command is, in Boolean form,

$$\text{Preset Load} = \overline{B \cdot A}.$$

The count enable has an external input which comes from an external counter. This input is named "Channel 0-99 OK." This input is from a counter which determines whether the memory is in the first 100 addresses or not. The logic has been expressly designed for a 100 channel analyzer. The Boolean expression for the count enable is

$$\text{Count Enable} = \overline{\overline{A} \cdot D},$$

where D represents "Channel 0-99 OK." When D is "1", the count enable is A; when D is "0", the count enable is "1"

The count to be added into the memory must occur after the preset is loaded and the counter is enabled. This condition must be present regardless of whether the count is a new count entering memory or the carry or borrow output for the other digits.

The pulse which adds 1 count is the output of I-2-A, a 4-input NAND gate. The external input to this gate is labeled "OK add 1 count." This input represents either a new count to be added to the units or a carry to or borrow from other digits. The logical expression for add 1 count is, if "OK add 1 count" is labeled E,

$$\text{Add 1 count} = \overline{\overline{C} \cdot B \cdot \overline{A} \cdot E}.$$

When E = "1" the Add 1 count = $\overline{\overline{C} \cdot \overline{A} \cdot B}$, and when E = "0" the Add 1 count = "1"

The $\Phi 2$ clock, the input clock for the shift register, must occur after the Add 1 count pulse. This sequence allows the new value of the counter to be loaded into the shift register. After the $\Phi 2$ pulse the shift register shifts to the next bit; the $\Phi 1$ clock pulse, consequently, should follow the $\Phi 2$ clock pulse closely in time. The $\Phi 2$ clock pulse in Boolean form is as follows:

$$\Phi 2 = \overline{\overline{C} \cdot A \cdot \overline{B}}.$$

The total clock sequence for the timing and synchronization circuit is depicted in Figure 6.

The actual circuit has a 540 pf capacitor to ground at the output of I-4-C. This capacitor is used to compensate for the delays through the J-K flip-flops. The typical propagation delay for an SN7473 J-K flip-flop is 25 ns. For example if $\overline{B}$ = "1", A = "1", and $\overline{C}$ = "0", then $\Phi 2 = \overline{\overline{C} \cdot A \cdot \overline{B}}$ = "1" On the "0" to "1" transition of the master clock $\overline{C}$ changes to "1", typically 10 ns after the master clock transition if no capacitor C-1 is present. Therefore, at time t = 10 ns $\overline{C}$ = "1", A = "1" and $\overline{B}$ = "1", and $\Phi 2$ = "0" The $\Phi 2$ clock makes the transition from "1" to

"0" at t = 10 ns. At t = 25 ns the $\overline{B}$ output of I-1-B makes its transition from "1" to "0" Therefore, at t = 25 ns $\overline{C}$ = "1", A = "1", $\overline{B}$ = "0" and $\Phi 2$ = "1" The $\Phi 2$ clock therefore makes an unallowable transition and is in the wrong state from t = 10 ns to t = 25 ns with no capacitor C-1 present.

The 540 pf capacitor C-1 holds the output of I-4-C at "0" or "1" until the J-K flip-flops have changed their outputs. This capacitor compensates for the propagation delays through the flip-flops and eliminates the possibility of false outputs because of the propagation delays through the various integrated circuits.

Mössbauer Data Analyzer:

Circuit Requirements: Figure 7 shows the timing and synchronization circuit appropriate to a Mössbauer Data Analyzer. The circuit must provide essentially the same timing and synchronization that is necessary in a pulse height analyzer. A Mössbauer analyzer remains at one address and counts for a period of time, however; then the memory indexes, and the system counts at a new address. The timing and synchronization circuit for a Mössbauer analyzer is, therefore, not restricted to 1 count per address per cycle of memory, as is true for a pulse height analyzer

Figure 8 gives the time sequence for the pulse train used to synchronize the memory of a Mössbauer analyzer.

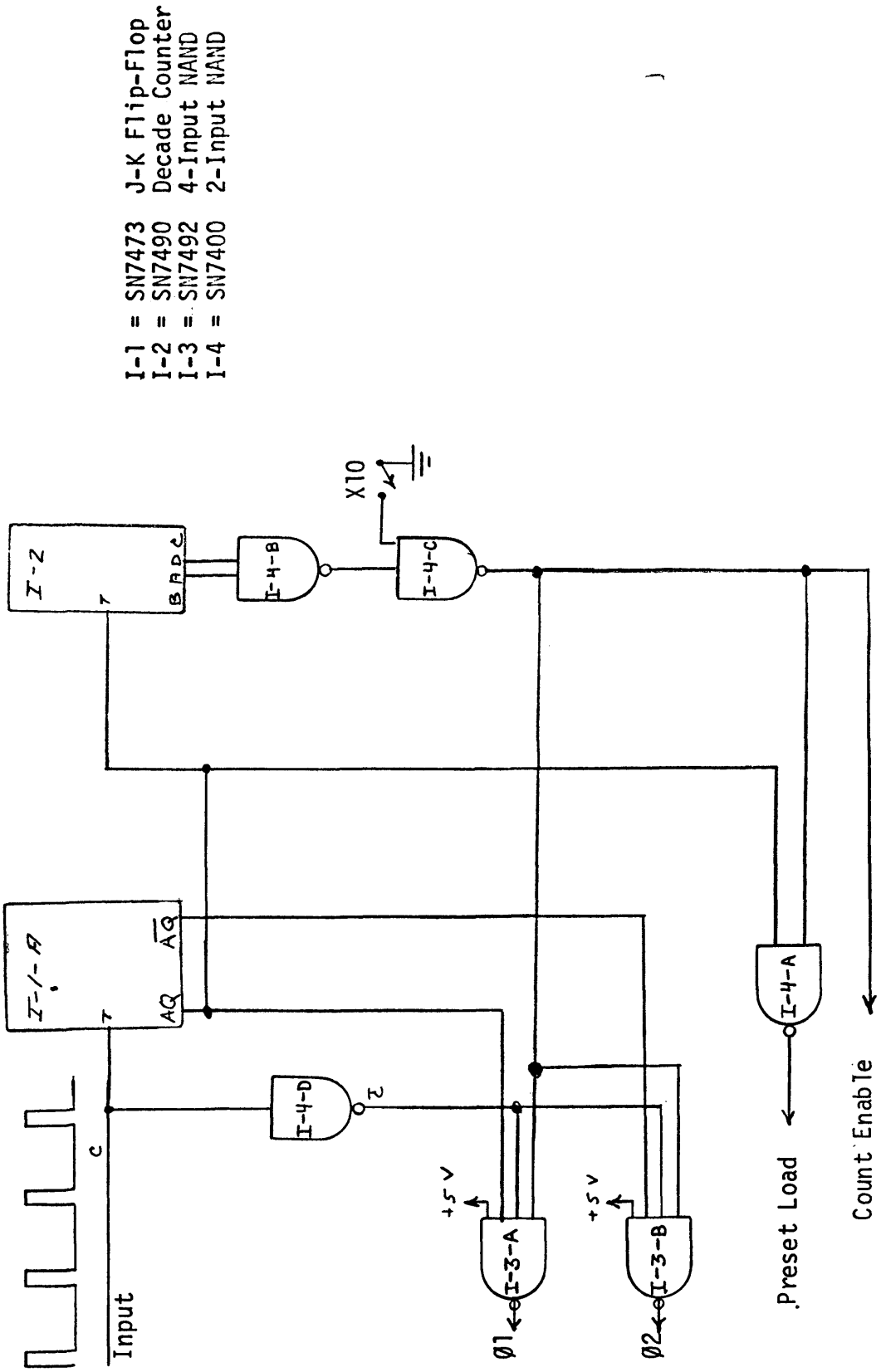
Circuit Operation: Pulses from the master clock are applied to the input of I-1-A which is a J-K flip-flop. The QA output of the flip-flop provides the count pulses for I-2, a decade counter

The A and D outputs of I-2 are applied to the input of I-4-B, a 2-input NAND gate. The output from I-4-B is one of the inputs to I-4-C, the other input is a "X10" input. The "X10" input increases the shift frequency by a factor of 10 and completely disables the memory input. This input is used in conjunction with the memory address selector to decrease the cycle time through memory.

The combination of I-2 and I-1-A provides the long count time at one address. The count time is 18 pulses out of 20 master clock pulses.

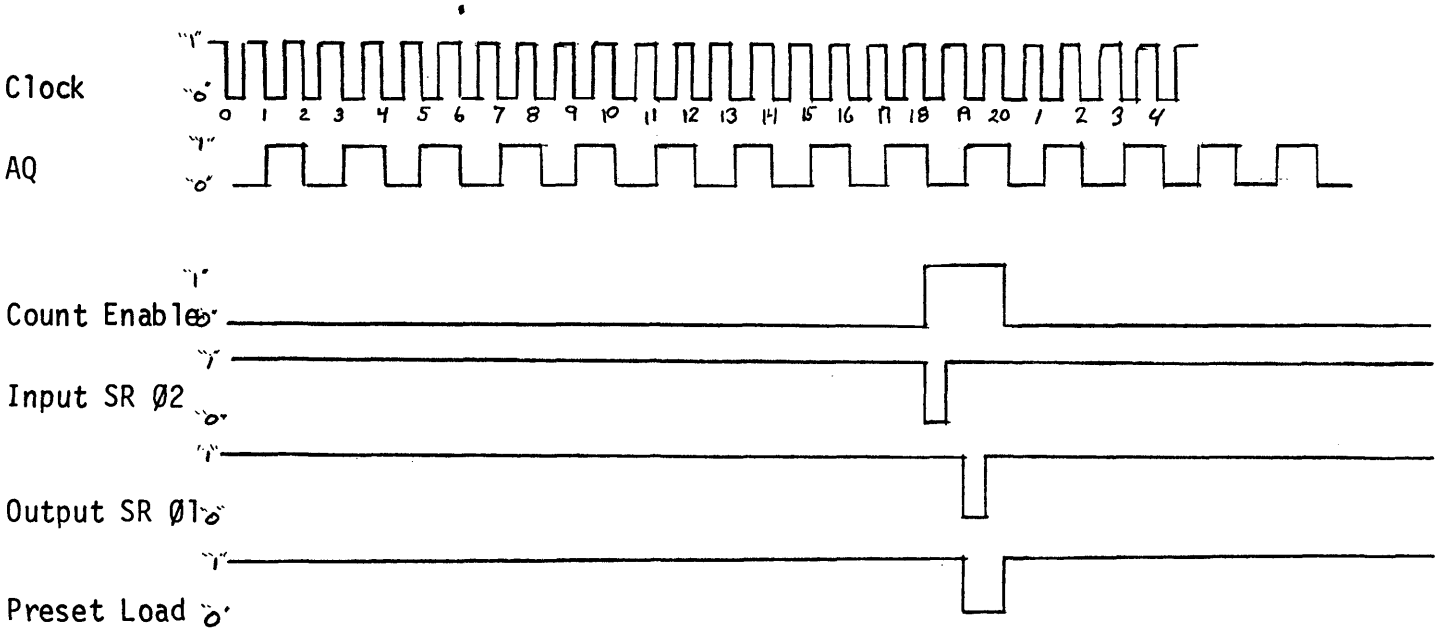
The count enable is high when the counter is disabled. The Boolean expression for the count enable is

$$\text{Count Enable} = \overline{\overline{A \cdot D} \cdot [X10]}.$$



Timing and Synchronization Circuit (Mössbauer Data Analyzer) - Logic Diagram

Figure 7



Pulse Train Sequence For Mössbauer Data Analyzer

Figure 8

The condition $A \cdot D = 1$ occurs only when the counter is at the BCD representation for the number 9. The counter counts alternate clock pulses. It counts on a high-to-low transition of its input pulse. I-1-A changes state on each clock pulse because its J and K inputs are connected to logic level "1" Since I-1-A has a high-to-low transition for every other clock pulse, the decade counter remains in each state for two master clock pulses. Therefore for pulses number 18 and 19 from the master clock A = D = "1", and for other pulses in the group of 20, $A \cdot D$ = "0"

For pulses number 18 and 19 in each group of 20, $\overline{A \quad D}$ = "0", the count enable is equal to "1", and the counter is disabled. If input "X10" is "0" then regardless of the other input for I-4-C the count enable is equal to "1", and the counter is disabled. If "X10" is "1" then during pulses 18 and 19 the count enable is equal to "1", and the counter is disabled; during the other 18 pulses in the group $\overline{A \cdot D} = 1$, count enable is equal to "0", and the counter is enabled. Consequently, the counter is enabled for 18 out of every 20 pulses of the master clock, and it is disabled for the remaining 2 pulses in 20.

The output shift register clock $\Phi 1$ and the input shift register clock $\Phi 2$ must occur during the time when the counter is disabled. Furthermore, the $\Phi 2$ must precede the $\Phi 1$ clock within the time span of the disable counter pulse. The preset load pulse has to occur throughout the time span of the $\Phi 1$ clock pulse, but not any longer than the disable pulse for the counter.

The Boolean expression for $\Phi 1$, the output shift register clock, is

$$\Phi 1 = \overline{\overline{C} \cdot [AQ] \cdot [\text{Count Enable}] \cdot 1}$$

I-3-A and I-3-B are four-input NAND gates; the fourth input is connected to "1" This connection effectively makes the gates three-input gates. If the count enable is equal to "1", as could be externally set by making the "X10" = "0", then the $\Phi 1$ clock is simply equal to $\overline{\overline{C}\ [AQ]}$. With $\Phi 1$ equal to $\overline{\overline{C} \cdot [AQ]}$ the shift register will shift ten times faster because the decade counter I-2 no longer has to count to 9 for the count enable to equal "1"

The preset load is given by the expression

$$\text{Preset Load} = \overline{[AQ] \cdot [\text{Count Enable}]}.$$

This expression ensures that the "0" to "1" transition of the $\Phi 1$ clock pulse occurs entirely within the preset load command.

The input shift register clock $\Phi 2$ has the following Boolean expression:

$$\Phi 2 = \overline{\overline{C} \cdot \overline{[AQ]} \cdot [\text{Count Enable}] \cdot 1}$$

The only difference between the $\Phi 1$ clock and the $\Phi 2$ clock lies in the interchange of AQ and $\overline{AQ}$ in the logic expression. This factor ensures that the pulses will occur closely in time and also that the $\Phi 2$ clock will precede the $\Phi 1$ clock in time.

CHAPTER 4

ANALOG PULSE STRETCHER

Introduction:

An analog pulse stretcher is a circuit which stretches in time a short duration input pulse while maintaining the height, i.e. voltage, of the input pulse. This circuit is required in a pulse height analyzer Design input pulse duration is approximately 0.5 μs. Design range for input pulse height is 0 to +10 V.

In the 100 channel pulse height analyzer the pulse stretcher is needed because the stretched pulse must be compared to a linear ramp. The linear ramp is generated from the same clock that is driving the memory. The linear ramp generator must be synchronous with the memory. A circuit that generates such a ramp with automatic compensation to ensure linearity is outlined by D. M. Brockman[3] in "Electronics" Vol 46, No. 2. When the stretched pulse voltage and the linear ramp voltage are equal, one count is added to the then current address in memory. The location in memory is determined by the height of the ramp and hence by the height of the input pulse.

The 100 channel pulse height analyzer has a memory cycle time of 0.2048 ms; this is calculated on the basis of a shift frequency of

2.5 MHz and register capacity of 512 bits.

The voltage range of the input pulse is 0 to +10 volts, and the pulse height analyzer has 100 channels; therefore, the width of each channel is 0.1 volt.

The requirements of the pulse stretcher are that it must accept an input pulse of voltage 0 to +10 and width of 0.5 μs; the output pulse must not decay by 0.1 volt in 0.2048 ms; the output voltage must bear a linear relationship to the input pulse voltage.

Basic Pulse Stretcher Circuit:

Pulse Stretcher Theory: A simple circuit that could be used for an analog pulse stretcher is a capacitor and diode, as depicted in Figure 9.

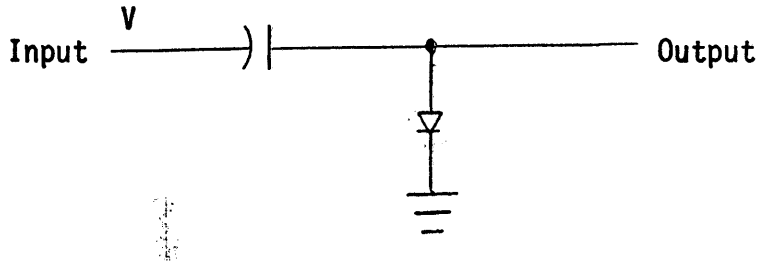


Figure 9

A positive pulse of height V is applied to the input. Because the capacitor cannot instantaneously change its charge, the right plate of the capacitor initially rises to the same potential as the left. As the potential of the right plate increases, the diode becomes forward biased and conducts. This action then brings the right plate of the capacitor to ground potential, charging the capacitor to the voltage V of the pulse.

When the input pulse returns to ground, the capacitor again cannot instantaneously change its charge; consequently, the right plate is now at a potential of -V. The diode is reverse biased and the output voltage of the pulse stretcher is -V. A time sequence at the input and output of this circuit is depicted in Figure 10.

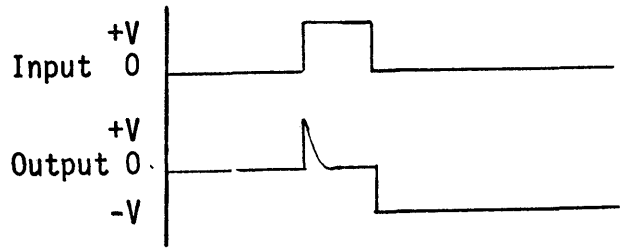


Figure 10

A disadvantage of this circuit arises from the characteristics of a semiconductor junction diode. The current through the diode is an exponential function of the voltage across the diode,(4)

$$I \simeq I_0[e^{qV/kT} - 1].$$

For small forward-biased voltages the current through the diode is small and as a result it takes a long time for the diode to bring the right plate of the capacitor to ground potential.

The basic pulse stretcher circuit utilizes the simple capacitor-diode pulse stretching circuit; however, it divorces itself of the dependence upon the diode's exponential behavior.

Super Diode Circuit: A super diode circuit uses an operational amplifier and a diode to simulate a diode with an extremely low turn-on voltage and high switching speed. Figure 11 shows such a circuit.

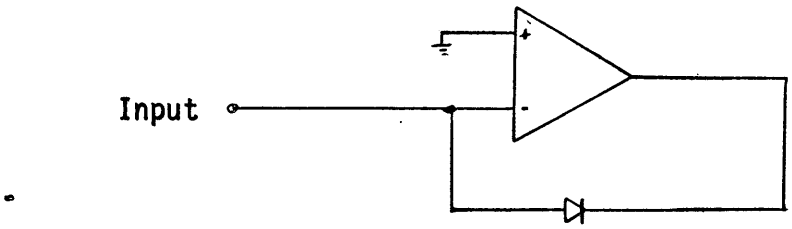


Figure 11

The operational amplifier has an open-loop voltage gain G, which is typically 10^4. The non-inverting input of the operational amplifier is grounded. Characteristic of negative feedback is a small potential difference or error voltage between the non-inverting and inverting inputs. If a positive pulse voltage δv is applied to the inverting input, the circuit ideally will apply δv to the anode of the diode and $-G[\delta v]$ to

the cathode of the diode. In practice G[δv] may be much greater than the saturation output voltage of the operational amplifier; if so, the output voltage of the operational amplifier will be limited to its saturation value. Having a potential of (1 + G)δv across it, the diode is forward biased. The turn-on voltage for a silicon diode is approximately 0.6 volt. Therefore the minimum δv that will strongly turn on the diode is

$$\delta v = \frac{0.6}{1+G} = \frac{0.6}{10^4} = 6 \times 10^{-5} \text{ volt.}$$

The diode in this circuit is strongly turned on at 6×10^{-5} volt rather than 0.6 volt as would be true for a diode alone.

If the voltage applied to the inverting input is -δv then the anode of the diode is at potential -δv and the cathode at potential G[δv]. The diode is reverse biased by a voltage of (G + 1)δv; consequently, only a small reverse leakage current is allowed in the diode for a small reverse voltage δv being applied to the input of the circuit.

Description of the Basic Pulse Stretcher Circuit: The basic pulse stretcher circuit is shown in Figure 12.

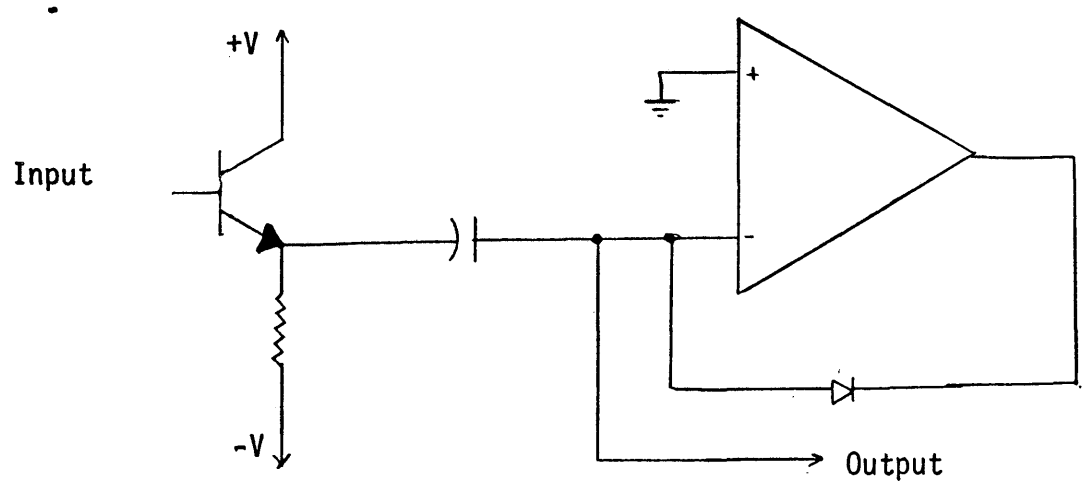


Figure 12

The transistor is connected as an emitter follower. Pulses to be stretched are applied to the base of this transistor. The emitter follower is a buffer stage which provides enough current to charge the capacitor quickly. The DC offset characteristic of the base emitter junction will not affect the operation of the pulse stretcher because the stretching capacitor AC couples the input buffer to the rest of the circuit.

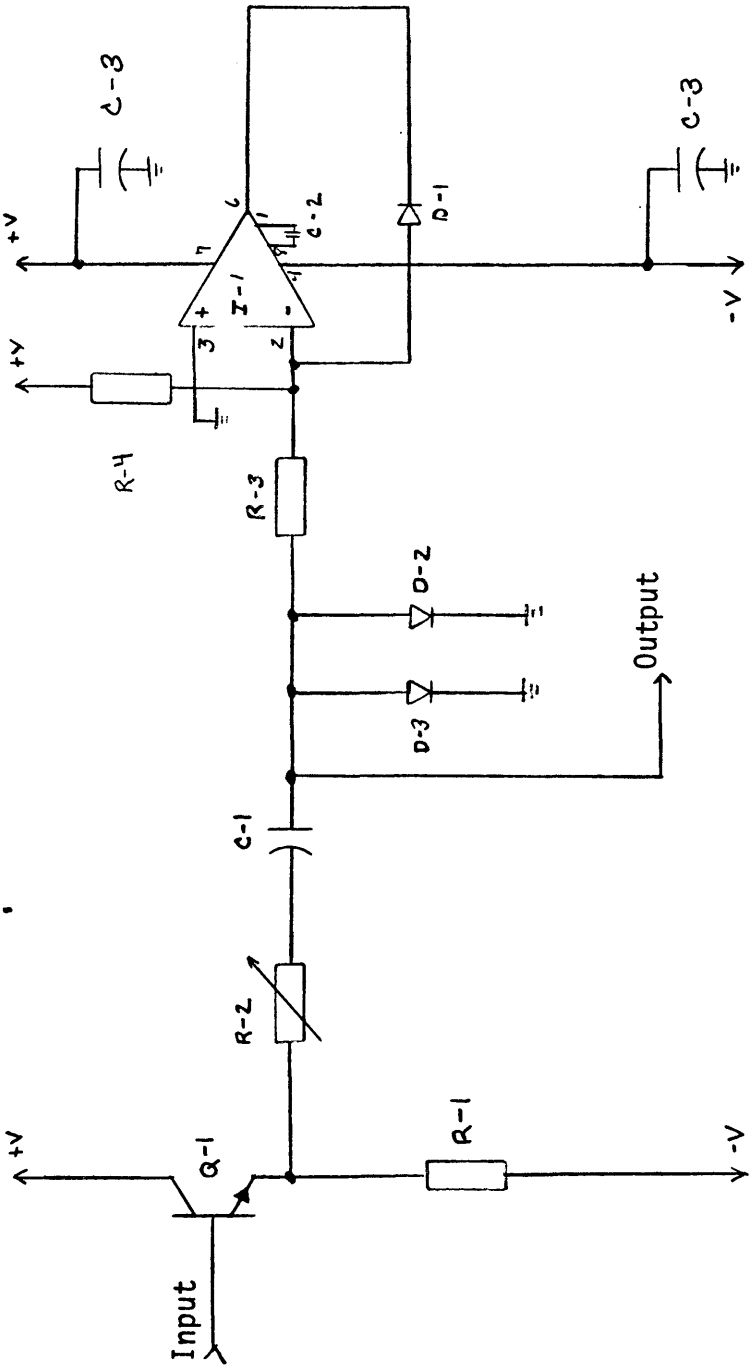
The operational amplifier and diode form a super diode. This is the charging diode through which the capacitor is charged.

The operation of this circuit resembles that of a simple capacitor-diode pulse stretcher, except that the super diode has an extremely small turn-on voltage.

Practical Pulse Stretcher Operational Design: Figure 13 shows the pulse stretcher. Added components are necessary to reduce non-ideal effects that detract from overall circuit operation.

The inverting input bias current for the operational amplifier is supplied by resistor R-4, which is necessary because this input is capacitively coupled. Resistor R-4 is slightly smaller than required for proper bias, so that in the absence of an input pulse the feedback diode is conducting. Because the feedback diode is turned on, negative feedback keeps the error signal at approximately 0 volts. This feature ensures that the right plate of capacitor C-1 is quiescently at ground potential.

Capacitor C-2 is a frequency compensation capacitor. The use of a non-frequency compensated operational amplifier allows the designer to



Q-1 = TIP 31 A

R-1 = 1 KΩ
R-2 = 1 KΩ
R-3 = 560 Ω
R-4 = 44 MΩ

C-1 = 180 pf
C-2 = 20 pf
C-3 = .01 mfd

D-1 = 5082-2800
D-2 = 5082-1002
D-3 = 5082-2800

I-1 = SN72770 OPAMP

+V = 12 Volts

-V = -12 Volts

First Stage

Figure 13

increase the slew rate by choosing the smallest compensation capacitor that gives stable operation.

Capacitors C-3 are ceramic disk capacitors. These capacitors are used to bypass the power supplies, eliminating stray feedback paths which may cause the operational amplifier to oscillate. The ceramic capacitors are used because they have better response at the high frequencies. These capacitors are mounted physically as close to the power supply input pins on the integrated circuit as possible.

The feedback diode D-1 is a Schottky diode, HP-5082-2800. This diode exhibits a forward voltage drop of less than 0.41 volts at a forward current of 1 ma. The diode also has a switching time of 100 ps. The fast switching time reduces the degradation of the stretched pulse because the diode can quickly turn off.

Diodes D-2 and D-3, which are connected from the right plate of the stretching capacitor to ground, are both HP diodes. Diode D-3 is a Schottky diode, HP-5082-2800. This diode exhibits a low turn-on voltage. Diode D-2 is a HP high conductance diode, HP-5082-1002. This diode exhibits a forward current of 800 ma at 1.4 volts. The parallel combination of these two diodes gives an equivalent diode which has a low turn-on voltage and a high conductance. The diodes D-3 and D-2 are used as the diode constituent of a simple capacitor-diode pulse stretcher. The diodes actually do most of the work in bringing the right plate of the stretching capacitor to ground potential. The actual operation is as follows: first, the feed-through pulse through the stretching capacitor raises the potential of the right plate of the stretching capacitor; second, diode D-3, having a lower turn-on voltage, turns on and tries to bring the

potential of the right plate back to ground; third, diode D-2, having not only a higher turn-on voltage but also a higher conductance, turns on and brings the potential of the right plate down into the region where the operation of diode D-3 predominates; fourth, diode D-3 brings the potential of the right plate of the stretching capacitor to within a few tenths of a volt above ground; fifth, the operational amplifier-diode combination finally brings the potential of the right plate of the capacitor very nearly to ground potential. By using the two parallel diodes the requirements of the operational amplifier are reduced because the operational amplifier does not have to work with voltages on the order of 1 to 10 volts. The operational amplifier has to bring the right plate of the capacitor from only approximately 0.4 volts to ground potential. The operational amplifier can have a smaller slew rate and longer response time than would be allowable if only the super diode were used.

Fast rise-time pulses have been found to shock components of this circuit. The effect of a fast rise-time pulse may be to charge some stray capacitance in the operational amplifier, thereby paralyzing the operational amplifier until the capacitance has discharged. Paralysis manifests itself in overcharging of the capacitor. This effect arises from the paralysis-caused delay in the feedback. Fast rise-time pulses also affect the parallel diodes, D-2 and D-3. The effect on the diodes is what appears to be a short-lived forward conduction current when the diode is reverse biased. Resistors R-2 and R-3 were added to improve operation with fast pulses. Resistor R-2 increases the rise time of the pulse somewhat; while R-3 limits the current which can flow into the

amplifier input before negative feedback has had time to take place. Resistor R-2 is a variable resistor and is adjusted for a compromise between shock oscillations and pulse rise time.

The process of charging a capacitor rapidly and yet not having appreciable decay is quite difficult. The requirement of charging a capacitor to a voltage V in a minimal amount of time dictates either a large charging current or a small capacitor. The charging current is limited due to non-ideal shock-exciting characteristics of some of the components as has been previously explained. Therefore, a small capacitor is required in the pulse stretcher. The difficulty of having a small stretching capacitor is the decay time of the stretched pulse is governed by either the R-C discharge time or by the constant current discharging the capacitor. Either of these effects is directly proportional to the size of the capacitor. Therefore, to be able to stretch a fast pulse, i.e. charge a capacitor, the capacitor must be small; this results in a quickly decaying stretched pulse. By using a two stage pulse stretcher these difficulties are easily overcome. The first stage of the pulse stretcher must charge the stretching capacitor rapidly, but it only has to provide a relatively short output pulse; the difficulties of using a small capacitor, consequently, are overcome. The second stage requirement is that it must provide a relatively long output pulse width. The stretching capacitor used here is large; therefore, the discharging time of the capacitor is large. The input pulse for this stage is provided by the first stage. This pulse has already been stretched a small amount by the first stage; the time available to charge this larger capacitor is, therefore; also larger. The two

stage pulse stretcher can therefore stretch a fast pulse for a long time.

Two Stage Pulse Stretcher Circuit:

First Stage: The first stage of the two stage system is the practical pulse stretcher already discussed and shown in Figure 13. A requirement for the first stage is that it must be able to accept a pulse with short rise time and minimum pulse width of 0.5 μs. The first stage has to stretch the pulse with essentially no decay (less than 0.05 volts) for only 5 μs. The high speed requirements of this stage dictate that the stretching capacitor be small

To satisfy the high speed and small decay requirements an operational amplifier with small bias current and large slew rate is required. The operational amplifier selected is an SN72770. This operational amplifier has a bias current of typically 8 nA and a slew rate of 2.5 volts per μs, with a compensation capacitor of 30 pf The compensation capacitor C-2 used is 20 pf This 20 pf capacitor gives a larger slew rate.

The bias current resistor R-4 is a 44 MΩ resistor. This is considerably smaller than required for bias current alone and holds the feedback diode in the conducing state, as noted before.

In order for the circuit to handle short-lived pulses the capacitor C-1 has to be small. The smaller the capacitor, the more easily it may be fully charged in the 0.5 μs width of the incoming pulse. The largest practical value for capacitor C-1 has been experimentally determined to be 180 pf

A value of 560 Ω for the anti-shock resistor at the operational amplifier input has been determined to be appropriate.

The rise-time-increasing resistor R-2 for the system is a 1 KΩ trimpot that is adjusted for minimum pulse overshoot. An order of magnitude calculation for R-2, based upon a rise time of 200 ns with C-1 = 200 pf, gives R-2 = 1 KΩ.

The emitter-follower transistor Q-1 is a TIP-31A. This element is an NPN power transistor used to charge the stretching capacitor C-1 Resistor R-1 fixes a standing current I_s in the transistor of 12 mA with the input quiescently at ground potential

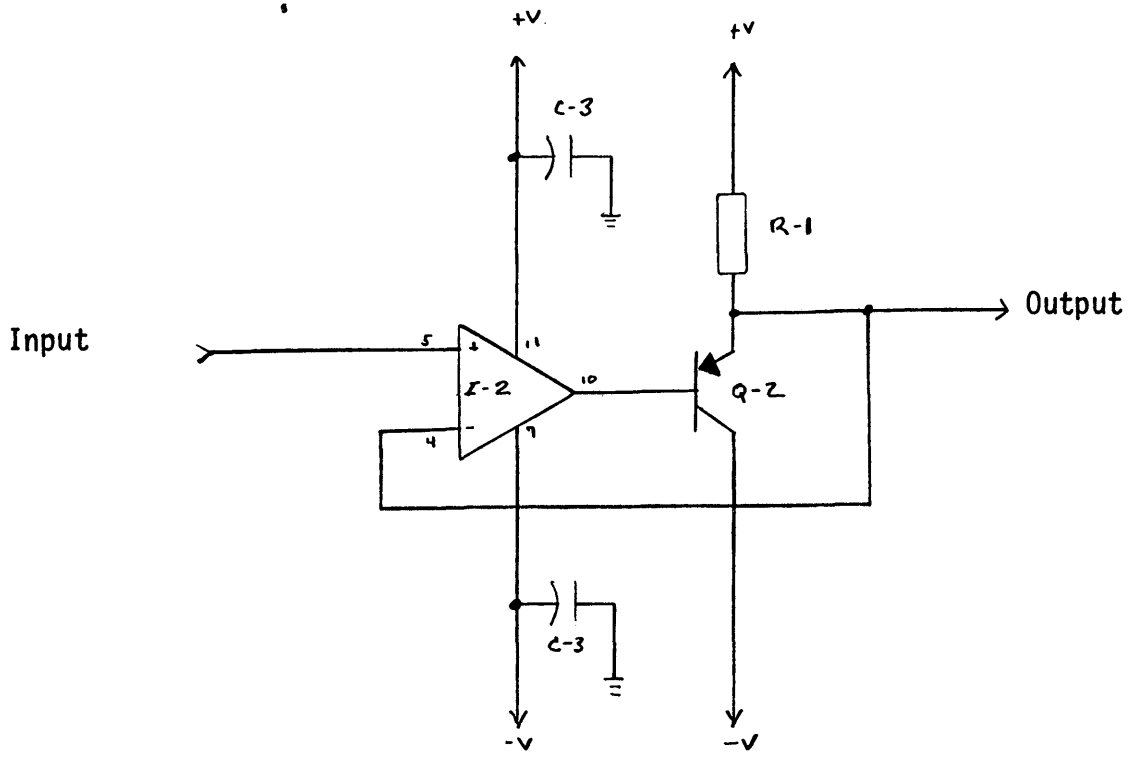
$$R\text{-}1 = \frac{V_E}{I_s} = \frac{12\ V}{12 \times 10^{-3} A} = 1000\ \Omega = 1\ K\Omega$$

The 12 mA standing current decreases the transistor's response time.

First Stage Output Buffer: The output buffer for the first stage is depicted in Figure 14. The output of the first stage comes from the right plate of the stretching capacitor. Any current taken from this output degrades the stretched pulse; that is, it causes the capacitor to discharge. The output buffer decreases the current drawn from the capacitor.

- This buffer has to have a moderate slew rate, unity gain, low input current requirement, and sufficient output-current capability.

The circuit configuration for this buffer consists of an operational amplifier and power transistor connected to operate as a power voltage follower. The transistor Q-2 is a TIP-32A, a PNP power transistor. The transistor is connected as an emitter follower whose input is connected to the output of the operational amplifier. The output of this stage occurs at the emitter of Q-2 and is applied to the inverting input of



Q-2 = TIP 32 A R-1 = 1 KΩ C-3 = .01 mfd I-2 = SN72771 OPAMP

+V = +12 volts -V = -12 volts

First Stage Output Buffer

Figure 14

I-2, an SN72771, providing 100% negative feedback. With the transistor within the feedback loop the characteristics of the individual transistor will not affect the operation of the circuit.

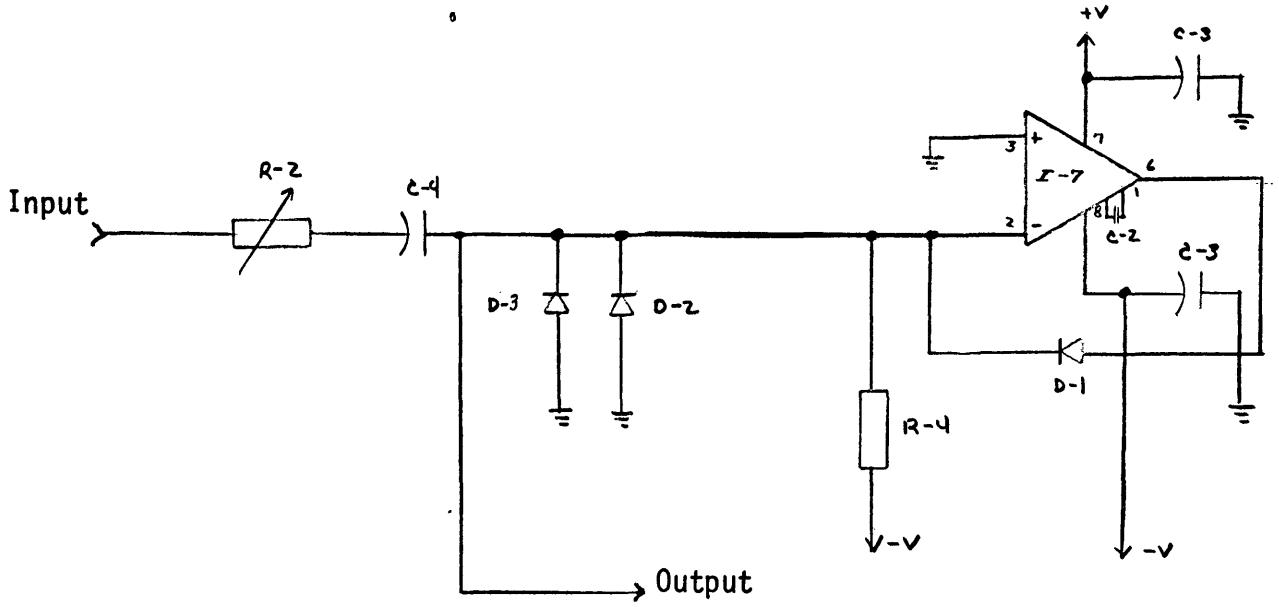
The operational amplifier I-2 is identical to the operational amplifier used in the first stage except the frequency compensation capacitor is internal on I-2. This operational amplifier has a small loading effect on the first stage in that it typically requires 8 nA input current. The power transistor can provide a great deal of current, typically 3 A.

The emitter resistor R-1 of transistor Q-2 is a 1 KΩ resistor. This resistor fixes a quiescent current of 15 mA in the transistor. The standing current improves the response of the transistor Q-2 by decreasing both response time and output impedance of this stage.

The capacitors C-3 bypass the power supply leads and prevent oscillation.

Second Stage: The second stage is schematically diagrammed in Figure 15. The second stage accepts the negative pulses from the output-buffer and stretches these pulses for the final time. This stage does not have the strict speed requirements of the first stage because the input pulse for stage two is the stretched output from stage one. Because this stage can work at a slower speed the stretching capacitor can be much larger, thereby generating a longer stretched pulse. The stretching capacitor C-4 for stage two is 0.01 mfd.

The circuit configuration is changed from that of stage one because stage two stretches negative input pulses. Therefore, all diodes in



R-2 = 1 KΩ
R-4 = 44 MΩ

C-2 = 20 pf
C-3 = .01 mfd
C-4 = .01 mfd

D-1 = 5082-2800
D-2 = 5082-1002
D-3 = 5082-2800

I-7 = SN72748 OPAMP

+V = 12 Volts

-V = -12 Volts

Second Stage

Figure 15

stage two are reversed from those of stage one. The bias resistor R-4 is connected to the negative power supply rather than the positive so it will keep the operational amplifier I-7 and feedback diode D-1 conducting.

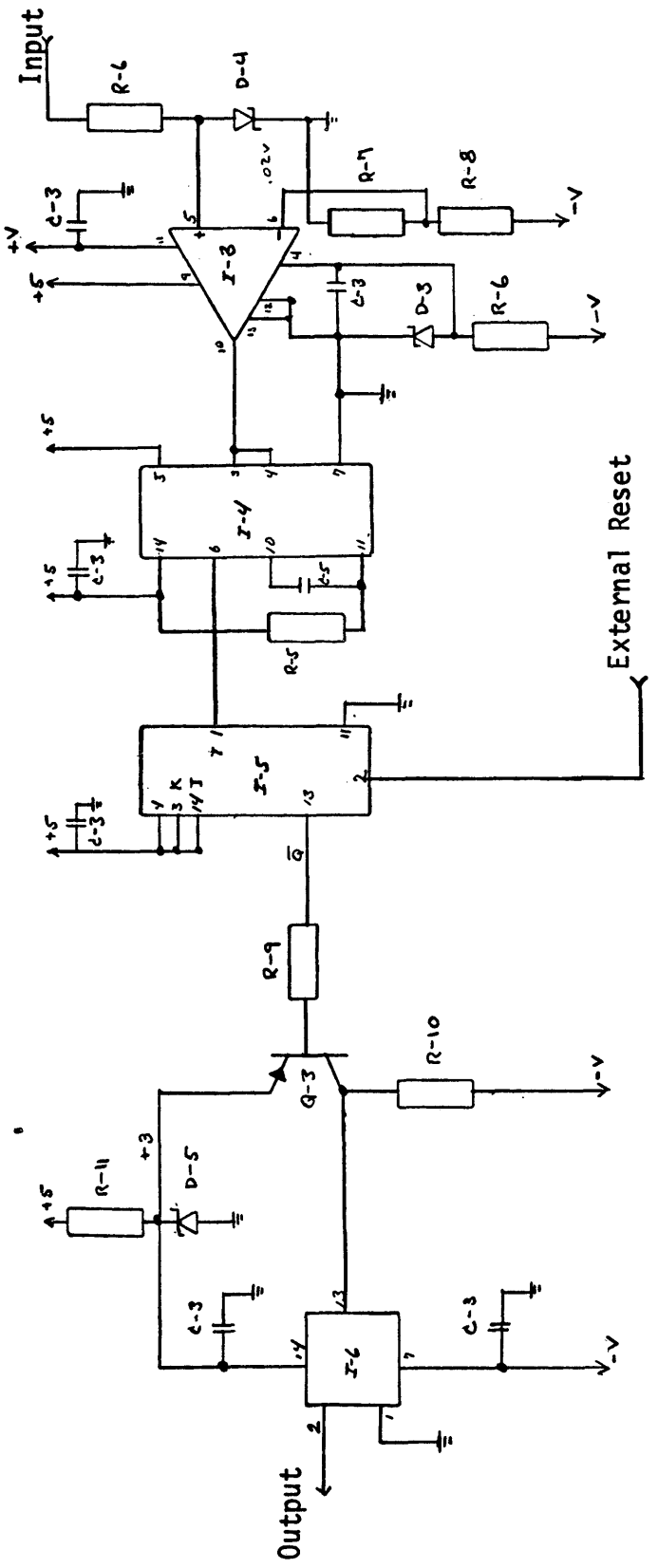
The operational amplifier I-7 is an SN72748. This operational amplifier has a smaller slew rate and frequency response than the one chosen for the first stage. Since speed is not required for this stage, the added stability from a slower amplifier may be exploited.

Amplifier I-7 must be externally frequency compensated, and capacitor C-3, 20 pf, has been found to provide the highest slew rate consistent with stable operation.

The capacitors C-3 are power supply lead bypass capacitors which provide added stability to the circuit.

Resistor R-2 is a 1 KΩ trimpot used to adjust the rise time of the input pulse for this stage.

First Stage Clear and Reset Circuit: The clear and reset circuit for the first stage is diagrammed in Figure 16. In the basic pulse stretcher circuit used here the stretched output pulse does not appear until the input pulse voltage has returned to zero. Hence, the stretched pulse from the first stage must be gone before the second stage can produce the final stretched pulse. The trailing edge transition to ground is the time at which the output pulse from the second stage will be generated. The pulse from the first stage has a large width, characteristic of the pulse stretcher circuit. Therefore, a clear and reset circuit is needed, which after a predetermined time clears the stretched



R-5 = 8.2 KΩ
R-6 = 470 Ω
R-7 = 15 Ω
R-8 = 10 KΩ
R-9 = 5.6 KΩ
R-10 = 6.8 KΩ
R-11 = 1 KΩ

C-3 = .01 mfd
C-5 = 1000 pf

Q-3 = 2N2635

D-3 = 1N821 6.3 volts
D-4 = 1N750A 4.7 volts
D-5 = 1N4372 3 volts

I-3 = SN72711 Voltage Comparator
I-4 = SN74121 Monostable Multivibrator
I-5 = SN7473 J-K Flip-Flop
I-6 = CD4016AE Analog Switch

+V = 12 volts

-V = -12 volts

First Stage Clear and Reset Circuit

Figure 16

pulse in the first stage.

A voltage comparator I-3 is connected to the output buffer of the first stage. This comparator is designed to produce a logic level "1" to "0" transition when the potential at the inverting input of the comparator becomes greater than the potential at the non-inverting input, or vice versa. The inverting terminal of I-3 is at a potential $V_- = -0.02$ volt determined by the resistive voltage divider R-7, R-8. Therefore, if the non-inverting input is at ground potential then $|V_-| > |V_+|$ and the output of I-3 is "0" When a stretched pulse from the first stage output buffer is applied to the non-inverting input of I-3 then $|V_+| > |V_-|$, and the output of I-3 is "1" Therefore, as a pulse appears at the output of the first stage output buffer, the output voltage of I-3 makes a "0" to "1" transition.

The output from the first stage output buffer is applied through a Zener diode voltage limiter to the non-inverting input of I-3. The absolute maximum input voltage for either input of I-3 is ±7 volts, and since the maximum output voltage from the first stage is -10 volts, a limiter must be provided. The Zener diode D-4 is a 1N750A and has a Zener voltage of 4.7 volts, so that the voltage at the inverting input is limited to the range 0 to 4.7 volts.

The voltage comparator operates between power supplies of +12 volts and -6 volts. The +12 volts is a standard power supply voltage for the system; however, the -6 volts is not. The -6 volts is generated from the standard -12 volt power supply using Zener diode D-3 and resistor R-6.

Capacitors C-3 are used to bypass power supply leads of the voltage comparator. These capacitors provide added stability to the operation of I-3.

I-3 is an SN72711, which is a dual voltage comparator with strobed outputs. The strobe input, when held at "0", inhibits the associated channel. In this application only one comparator is required, and it was chosen to be the number two comparator. Therefore, "0" is applied to the strobe input for comparator number one, and "1" is applied to the strobe input for comparator number two.

The output of the voltage comparator makes a "0" to "1" transition when a pulse appears at the second stage input. This output is connected to the positive input of I-4, a monostable multivibrator, type SN74121 This "0" to "1" transition triggers the monostable multivibrator, which generates an output pulse, "0" to "1" to "0" The width of the pulse is determined by the external R-C timing network consisting of resistor R-5 and capacitor C-5. Values C-5 = 1000 pf and R-5 = 8.2 KΩ yield a pulse width of approximately 5 μs. For the monostable multivibrator to trigger on "0" and "1", negative input pin number 5 must have "1" applied to it, and the output of the voltage comparator must be applied to the input pin number 3 or number 4 or both.

Capacitor C-3 bypasses the power supply leads for the monostable multivibrator. This capacitor decreases the possibility of false triggering of the monostable multivibrator because of line transients.

The Q output of I-4 is applied to the clock input of a J-K flip-flop I-5. The J and K inputs have "1" applied to them, and consequently

the flip-flop will change states on each clock pulse. On the "1" to "0" transition of the Q output of I-4 the $\overline{Q}$ output of the flip-flop I-5 makes a transition from "1" to "0" This output remains at logic level "0" until the flip-flop is reset.

The output of I-5 is applied to the base of transistor Q-3, which is used as a saturated switch. For the transistor to operate in the saturated mode,

$$\frac{R\text{-}10}{R\text{-}9} > \frac{5}{h_{fe}}$$

Transistor Q-3 is a 2N2635, with h_{fe} = 30, and maximum ratings I_c = 10 mA, V_{ce} = 30 volts. Hence

$$6[R\text{-}10] > R\text{-}9.$$

Another consideration is the maximum collector current, I_c = 10 mA, which limits R-10 to more than 1.5 KΩ.

The operating values used in the circuit for R-9 and R-10 were chosen to be 5.6 KΩ and 6.8 KΩ respectively.

I-6 is an analog switch and is the device that is actually used to discharge the stretching capacitor for the first stage. The analog switch is a device whose resistance can be changed over a wide range by applying a control voltage. This device is essentially a field effect transistor. I-6 is a CD4016AE; the "on" resistance is approximately 200 Ω and the "off" resistance, 10^{12} Ω. One side of the switch is connected to the right plate of the first stage capacitor, and the other side is connected to ground. When the switch is on, the output of the first stage is grounded. The stretching capacitor discharges. When the switch is off, the output of the first stage is isolated from ground.

The feedthrough pulse, that part of the pulse that appears on the right plate of the first stage capacitor before the diodes and operational amplifier can react and bring the plate to ground potential, is transmitted through the entire circuit. This pulse is approximately 1 volt in magnitude. The largest negative pulse is -10 V. These two voltages fix the operating range of the analog switch. The analog switch must be powered so that the voltage on the switch never lies outside the range of the power supply voltages. Also the control voltage for the analog switch must be approximately equal to the supply voltage. The transistor switch Q-3 translates the logic level "0" and "1" voltages to +3 volts and -12 volts, respectively, for the control line of the analog switch. The transistor switch inverts its signal so that "0" corresponds to +3 volts and "1" corresponds to -12 volts. Zener diode D-5 and resistor R-11 constitute a Zener diode power supply for the analog switch. The Zener diode D-5 is a type number 1N4372, which regulates at 3 volts This scheme insures that the control voltages are within the supply voltages of the switch. Also, by powering the switch between +3 and -12 volts the switching voltages of +1 volt and -10 volts are well within the supply voltages of the switch.

Output Buffer: The output buffer is shown in Figure 17 The output buffer is simply an operational amplifier connected as a voltage follower. The voltage follower has a high input impedance and a low output impedance. High slew rate is not necessary in this stage; therefore, an SN72741 operational amplifier is used.

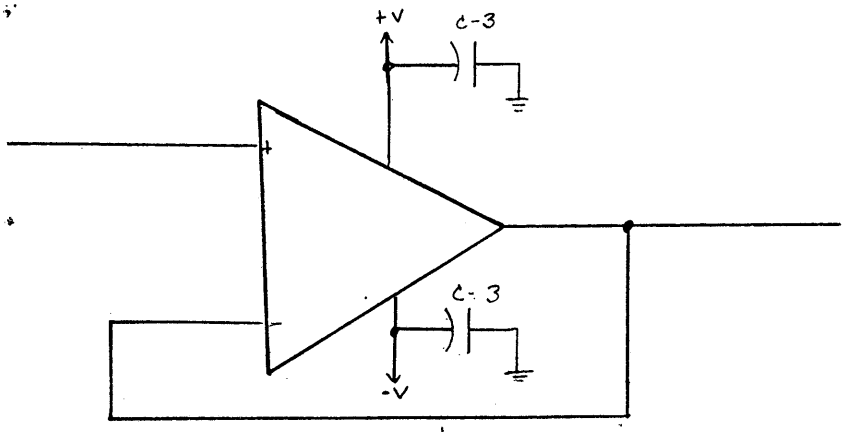


Figure 17

Summary: Figure 18 is a block diagram of the complete pulse stretcher. Positive pulses of height 0 to +10 volts and width 0.5 μs are applied to the input of an emitter follower in the first stage. The first stage further inverts and stretches the incoming pulse. The stretched pulse is generated from the first stage as the input pulse returns to ground. The presence of the pulse at the first stage output buffer triggers a timing circuit which, after a predetermined time of 5 μs, discharges the first stage stretching capacitor.

The negative voltage output pulse from the first stage output buffer is applied to the input of the second stage. As the first stage output returns to ground after the 5 μs delay, the final stretched pulse is provided at the output buffer.

The output pulse height is a linear function of the input pulse height. The output pulse decays by less than 0.1 volt in the 0.2048 ms required to cycle through 512 bits in the memory.

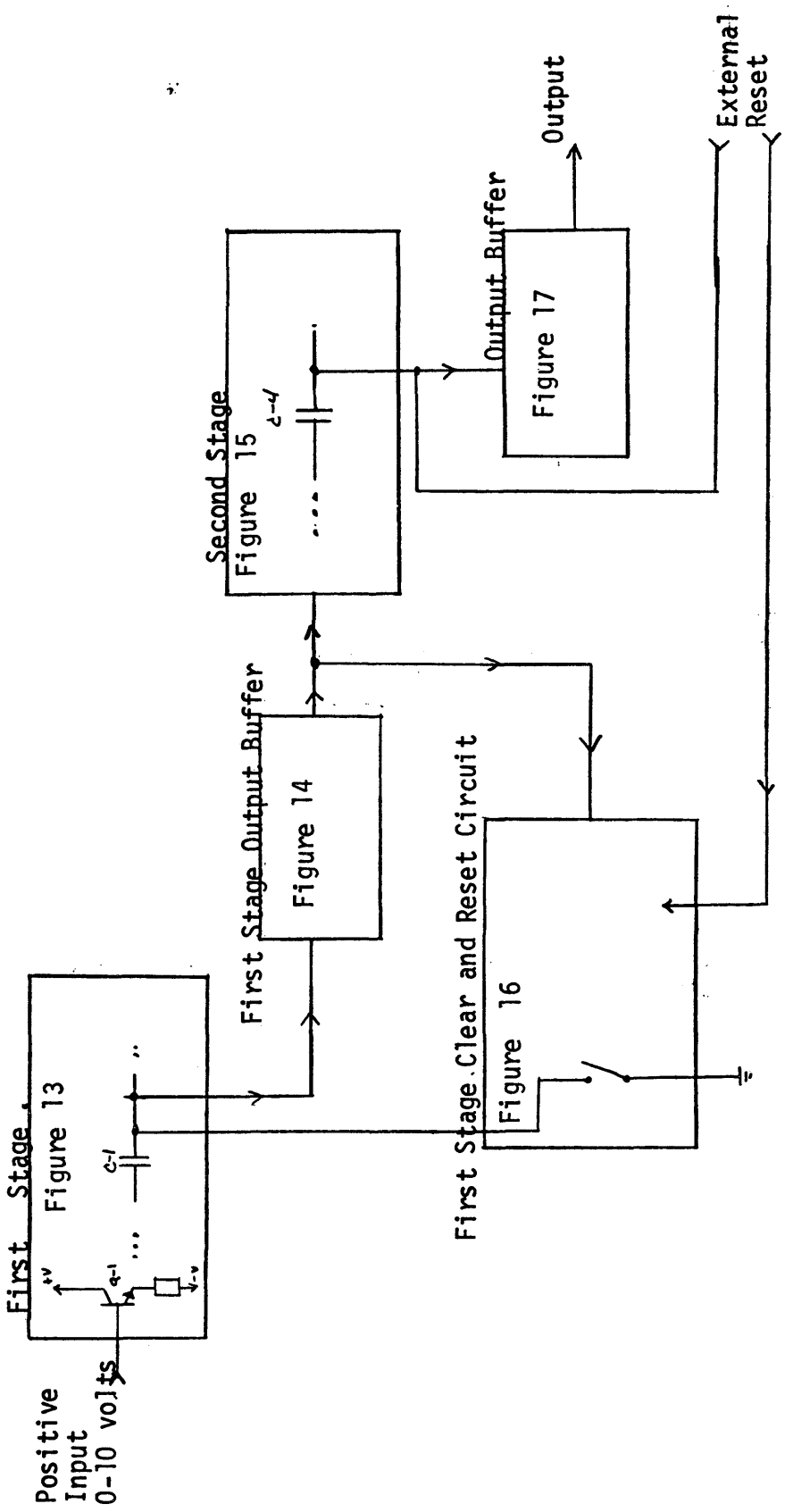


Figure 18

Block Diagram of Complete Pulse Stretcher

Testing the Pulse Stretcher:

Determination of the Minimum Input Pulse Width: The minimum input pulse width is determined by the first stage. For input pulses greater in width than the minimum, the output pulse height will be independent of input pulse width. In this case the stretcher will perform reliably.

The minimum pulse width is determined by the time required for the right plate of the stretching capacitor to be brought to ground potential by the diodes and operational amplifier. The plots of Figure 19 show the potential of the right plate of the stretching capacitor, time-correlated with the input pulse.

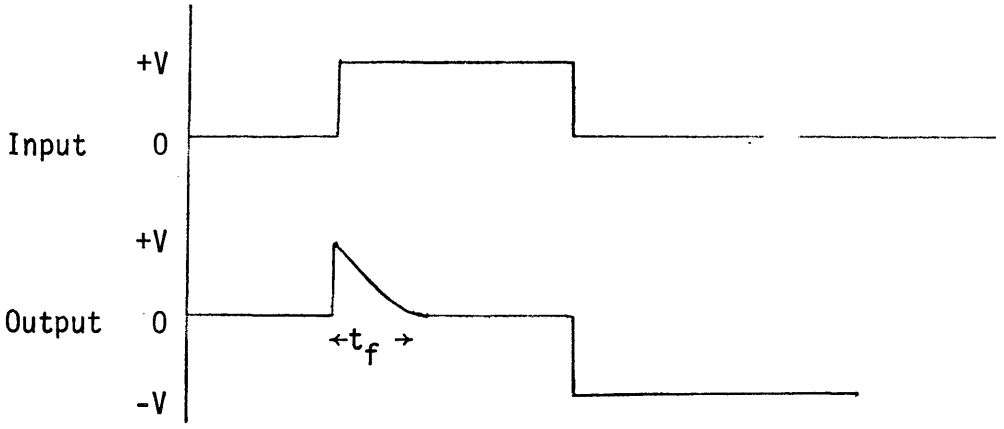


Figure 19

Time t_f is the minimum pulse width for which the pulse stretcher will perform reliably. Any smaller pulse width will not allow the diodes or operational amplifier to bring the potential of the right plate of the capacitor to ground potential before the input pulse returns to zero. If the right plate of the capacitor is not at ground potential when the input pulse returns to ground the output stretched pulse will be smaller in voltage than the voltage of the input pulse.

The minimum pulse width was measured on an oscilloscope to be 0.4 μs. Design minimum input pulse width is 0.5 μs; consequently, the pulse stretcher circuit will react fast enough to meet design requirements in this respect.

Determination of the Decay Time for the Stretched Pulse: The decay of the stretched pulse was found not to be an exponential R-C decay. It was found that the discharge of the capacitor was a linear function of time. The voltage across a capacitor is given by the relation

$$\frac{dv}{dt} = \frac{i}{C}.$$

Since voltage across the capacitor is a linear function of time it appears that the capacitor is being discharged by a constant current source.

The constant current source is the bias current that is required for the operation of the operational amplifier. This current, determined by R-4, discharges the capacitor.

The effect of this type of discharge is independent of the voltage of the pulse. That is, a pulse decays from 10 volts to 9.9 volts in the same time interval as it does from 0.2 volts to 0.1 volts.

The decay rate was measured on an oscilloscope. The time measured was for the stretched pulse to decay 0.1 volts. The pulse height was 0.5 volts; however, as explained above the time to decay a tenth of a volt is independent of the height of the pulse. The time to decay a tenth of a volt was measured to be 2 ms. Therefore, in the 0.2 ms required to cycle the memory the pulse decays only 0.01 volts. This is well within the required 0.1 volts decay in 0.2 ms.

Determination of Linearity: The height of the stretched output pulse is not equal to the height of the input pulse. This feature is not prohibitive in the use of the pulse stretcher. The only required relationship between input and output pulse heights is that the output must be a linear function of the input.

The fact that the output pulse height is less than the input pulse height suggests that there may be an AC voltage divider within the pulse stretcher circuit. The attenuation was found to exist only in the first stage of the pulse stretcher. An analysis of the effect of the capacitance of the two parallel diodes D-1 and D-2 on the overall circuit operation is given below. An equivalent circuit of a capacitor C-1, which corresponds to the stretching capacitor, and C-D, which corresponds to the total capacitance of the two diodes in parallel, and the output impedance of the emitter follower represented as Z, is given in Figure 20.

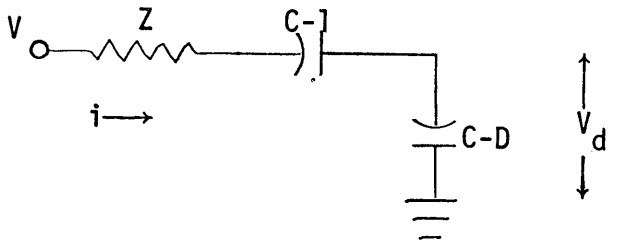


Figure 20

Step voltage V from the emitter follower is divided between C-1 and C-D. The value of capacitor C-1, the stretching capacitor, is 180 pf The capacitance of the diodes D-1 and D-2 is approximately 3 pf for each diode. The value of capacitor C-D is therefore 6 pf With these values the output voltage is related to the input voltage by the following expression:

$$V_D = \frac{V(180)}{180 + 6} = 0.967 \text{ V}$$

The slope of the graph of output versus input should be on the order of 0.967 This value is remarkably close to the actual measured slope, as will be shown later in this section.

The output voltage of the stretched pulse and the voltage of the input pulse were both measured on a pulse height analyzer The pulse height analyzer used for these measurements is a Victoreen SCIPP 400 channel analyzer. By plotting the address of the output pulse as a function of the input pulse address, the linearity of the pulse stretcher is determined.

An emitter-follower output buffer was used for these measurements instead of the voltage follower output because the maximum pulse width the SCIPP can accept is 3 μs. The slew rate limit of the output voltage follower is 0.5 volts per μs; therefore, a 10 volt stretched pulse will have a rise time of 20 μs. The 20 μs rise time of the output stretched pulse prohibits the use of this buffer. The emitter follower has a much faster slew rate, but suffers the disadvantage of a 0.6 volt offset. The SCIPP is capacitively coupled, however, so that the DC offset will not affect the measurements. The DC offset is objectionable in the ultimate application of the stretcher, nevertheless, and the voltage-follower output buffer is required.

The procedure for measuring the input and output pulse height is first to set the input pulse height by adjusting the pulse generator voltage. Second the input pulses are applied to the input of the pulse height analyzer, and the analyzer is allowed to accumulate counts from the pulse generator in a certain address. This address is recorded.

Next the output of the pulse stretcher is applied to the input of the analyzer and counts are accumulated in another address, and the address is recorded. This procedure is followed for pulse voltages covering the full range of the pulse stretcher.

Two sets of data were taken. One set of data was with fast rise time pulses, and the other set was taken with exponential rise and fall time pulses. If counts were accumulated in more than one address in the SCIPP, then a weighted average was taken to determine the channel The weighting factor for this average is the number of counts accumulated in the corresponding channel The SCIPP analyzer was set for 400 channels and ten volts full scale. Therefore, each channel of the analyzer corresponds to 0.025 volt.

Data set number 1 had input pulses generated by a Data Pulse pulse generator, Model Number 101 The input pulses had a rise time of 5 ns The input pulse width was 0.4 μs. Two separate calibration trials were made with this generator. The trials were separated by 7.5 hours Between these trials the pulse stretcher accumulated counts in only one channel The 7.5 hours' separation allowed for a stability measurement to be made on the pulse stretcher.

Data set 1-A was taken at 9:30 A.M. on June 27, 1973. Data set 1-A is given in Table 3. Data set 1-B was taken at 5:00 P.M. on June 27, 1973. Data set 1-B is given in Table 4. The results of these two data sets are graphed in Figure 21

The results of data sets 1-A and 1-B show the output of the pulse stretcher to be linear with respect to the input pulse by approximately 1.5 divisions. Each division corresponds to 0.025 volt; the output is

TABLE 3

Data Set 1-A
(Fast Rise Time Pulse Linearity Data)

Input Address	Average Input Address	Output Address	Average Output Address
393(22),394(68)	393.8	363	363
379	379	350	350
356	356	330	330
336	336	311	311
317	317	294	294
298	298	276	276
279	279	259	259
269(33),270(57)	269.6	249(5),250(69)	249.9
255	255	236	236
235	235	218(40),217(8)	217.8
206	206	192	192
193	193	180	180
170	170	160	160
147	147	139	139
117(65),118(25)	117.3	112	112
102	102	98	98
82(18),83(84)	82.8	80	80
64	64	61	61
46	46	44	44
42	42	40	40
37	37	36	36

The numbers in parentheses are the numbers of counts accumulated in the corresponding addresses.

TABLE 4

Data Set 1-B
(Fast Rise Time Pulse Linearity Data)

Input Address	Average Input Address	Output Address	Average Output Address
391	391	362	362
372	372	344	344
348	348	323	323
331(68),332(22)	331.2	307	307
309	309	286(16),287(29)	286.6
287	287	267	267
272	272	252(13),253(32)	252.7
250	250	232	232
229	229	213(36),212(9)	212.8
202(15),203(82)	202.8	189	189
180	180	169	169
162	162	152	152
147(72),146(18)	146.8	139	139
130	130	124	124
118	118	112	112
100	100	96	96
76(79),75(11)	75.9	73	73
56	56	54	54
39	39	38	38
34	34	33	33
26	26	25	25

The numbers in parentheses are the numbers of counts accumulated in the corresponding addresses.

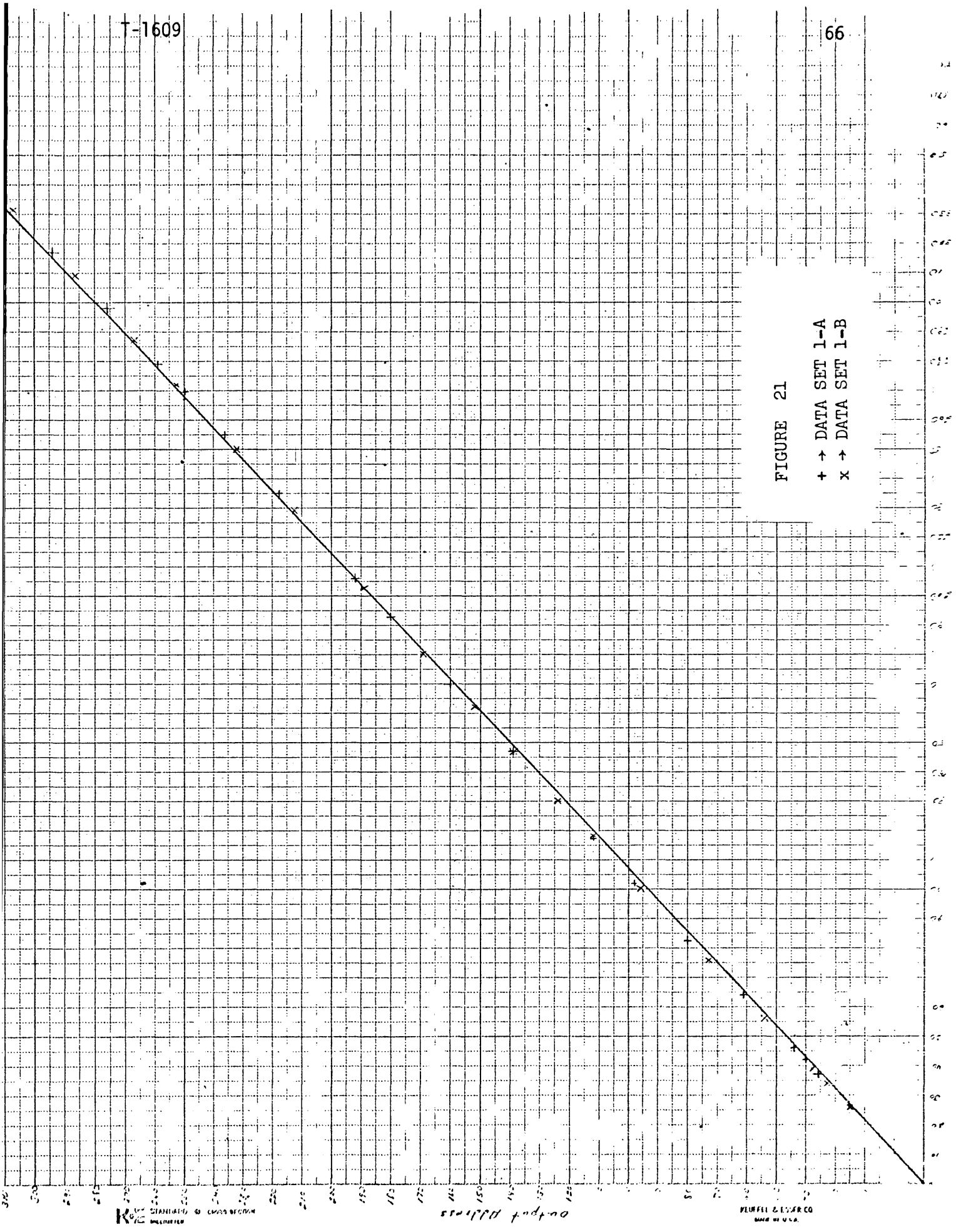


FIGURE 21

+ → DATA SET 1-A

x → DATA SET 1-B

linear, therefore, to approximately 0.037 volt. Another factor to be considered regarding these results is that the measurements were made by a digital device. All measurements were necessarily quantized and grouped into 0.025 volt intervals. A pulse on the edge of a channel could be in error by 1 channel which is 0.025 volt. With this fact taken into consideration the results of data sets 1-A and 1-B appear to be very good and certainly meet the requirements of a 100 channel analyzer. The fact that the fit to data set 1-B is the same line as for data set 1-A indicates that the pulse stretcher shows no drift nor instability over a 7.5 hour continuous run.

During the time interval between data set 1-A and data set 1-B the pulse stretcher had pulses of a single height applied to its input. The input pulse accumulated 22,071 counts in address 209. The output of the pulse stretcher accumulated 60,420 counts in channel 195 and no counts in any other channel Therefore it can be safely stated that the pulse stretcher output will drift by less than one half channel in 7.5 hours. This tolerance is approximately 0.013 volt in 7.5 hours. The actual drift may be considerably less than the above figure; however, the results above were taken at the resolution limits of the analyzer.

The second set of data used an RIDL precision exponential pulse generator, Model Number 47-2, to generate the input pulses. The input pulse had a 200 ns rise time and 4 μs decay time to ∿0 volts. The output of the pulse generator had to be buffered by an emitter follower. This buffer was necessary because the SCIPP loaded the output of the RIDL pulse generator. The results of this calibration run are tabulated in Table 5. Figure 22 is a graph of the data in Table 5 and further

TABLE 5

Data Set 2
(Exponential Rise Time Pulse Linearity Data)

Input Address	Average Input Address	Output Address	Average Output Address
313	313	296(21),297(160)	296.8
282(39),283(349)	282.9	266	266
252(212),253(151)	252.4	237	237
222	222	208	208
191	191	179(19),180(176)	179.9
160	160	151	151
129(321),130(86)	129.2	123(87),122(94)	122.5
98(196),99(198)	98.5	94	94
68	68	64(88),63(94)	63.5
38	38	35(16),36(89)	35.8

The numbers in parentheses are the numbers of counts accumulated in the corresponding addresses.

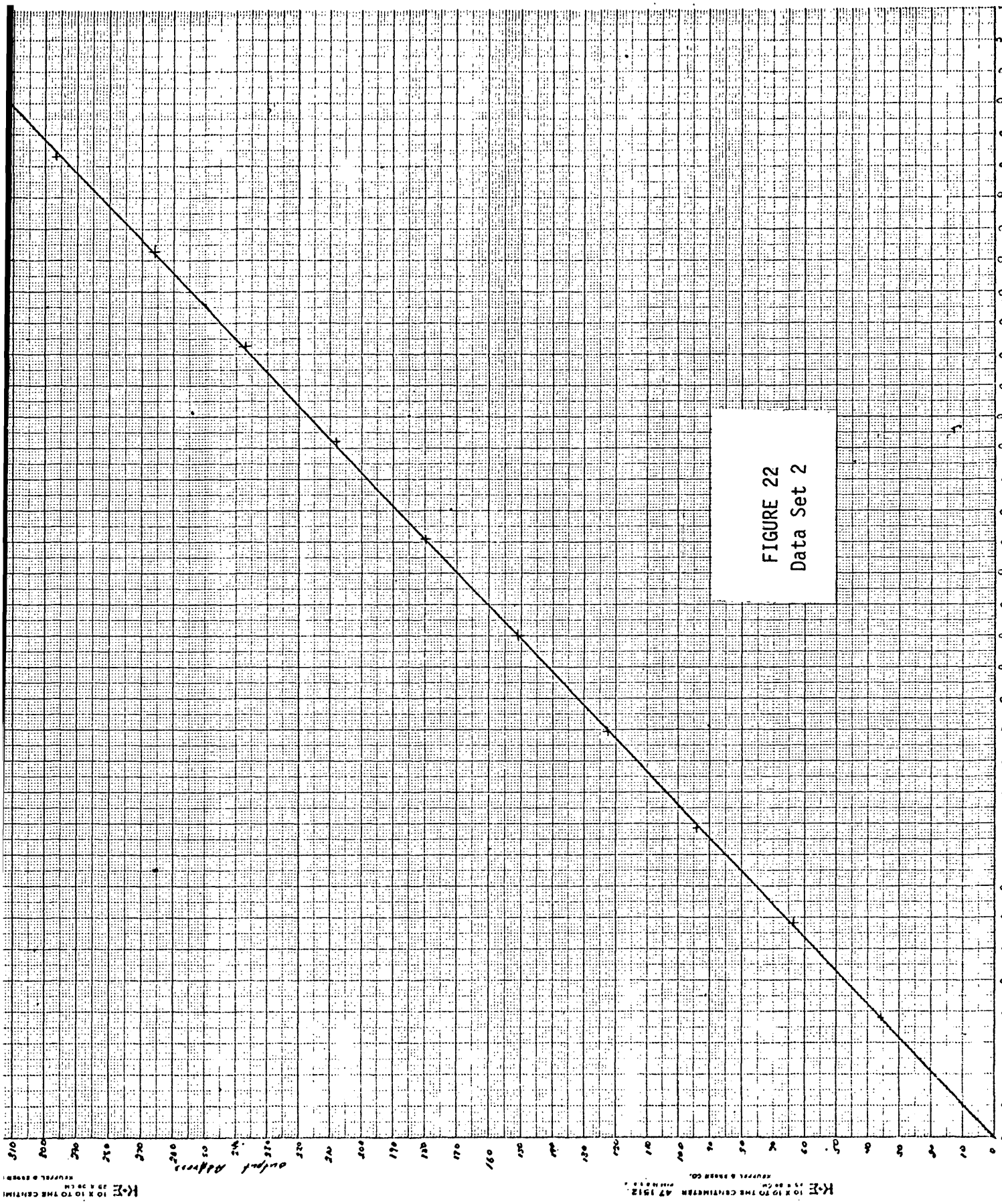


FIGURE 22
Data Set 2

shows the linear relationship between the input voltage and the output voltage. This graph shows a maximum deviation from linearity of 1 channel, which is the highest resolution of the SCIPP. Therefore the pulse stretcher circuit is satisfactory for use in a 100 channel analyzer with exponential pulses applied to the input of the stretcher.

The slope of the graph for the fast rise-time pulse is 250/267 = 0.936, and the slope of the graph for the exponential pulses is 250/266 = 0.940. The intercept of the graph has to be at the origin. Consequently, for a 10-volt fast rise time pulse the stretched output voltage is 9.36 volts, and for a 10-volt exponential pulse the stretched output voltage is 9.4 volts. The difference between these two values is four tenths of one channel

The theoretical value of the slope of the line from the discussion at the beginning of this section is 0.967 This value agrees remarkably well with theory because the capacitances of the diodes D-1 and D-2 are only approximate values.

Summary: The testing verifies that the pulse stretcher circuit meets and exceeds all requirements necessary for use in a 100 channel analyzer. The pulse stretcher will accept a 0 to 10 volt pulse of width 0.4 μs and stretch it for 0.2 ms with a decay of 0.01 volt. The input bears a linear relationship to the output within the accuracy of the measuring equipment and techniques.

CHAPTER 5

MEMORY ADDRESS SELECTOR

Introduction:

In a shift register memory the entire memory must be cycled to access all locations in the memory. For small memories and certain applications this feature proves to be an advantage rather than a disadvantage; with large memories, however, the time to cycle through the memory becomes prohibitive. In many applications the shift register is normally shifted at a rate much less than the maximum shift frequency. The memory address selector exploits this fact by allowing the selection of a certain block of memory to be used at the slow shift frequency and the remaining unused bits of memory to be shifted at the maximum shift frequency. This feature involves the use of two sets of four decade thumbwheel switches labeled Start Location and Stop Location.

The memory address selector card was designed for use with a shift register memory of 1024 bits; however, with minor modifications the memory address selector's capabilities can be easily extended to handle a larger memory.

Integral to the use of the memory address selector is a gated divider circuit. This circuit divides the maximum rated shift frequency for

the shift registers into a working frequency appropriate for the application.

Operating Sequence:

The operating sequence for the memory address selector is a four step one. The operator initially sets the address selector; Start Location is set for memory location "A" and Stop Location is set for memory location "B" The address selector cycles through the next four steps:

1 The memory address selector disables the divide circuit and the memory input until location "A" is reached.

2. The memory address selector enables the divide circuit and the memory input for memory addresses between locations "A" and "B"

3. The memory address selector disables the divide circuit and the memory input for memory addresses greater than "B"

4. The memory address selector resets all counters and flip-flops and returns to step 1 to begin the cycle again.

- This sequence causes rapid-shifting through the memory up to location "A", slow-shifting from location "A" to location "B", enabling either read or write functions, and then rapid-shifting from location "B" to 1024. At location 1024 the address selector signals, indicating end of memory, and returns to the beginning to initiate the cycle again.

Circuit Operation:

The decimal thumbwheel switches in this application actually perform some of the logical decisions in determining whether the start or stop location has been reached. This is in contrast to the use of BCD thumbwheel switches where the output of the thumbwheel switch is compared with the value from the counters to determine whether the start or stop location has been reached.

Figure 23 gives the logic diagram for the Memory Address Selector Positive pulses are applied to I-10-C, which is a NAND gate; this inverting gate is required because the decade counters and flip-flops make their transitions on a "1" to "0" transitions of the clock or toggle pulse. It allows the counters and flip-flops to make the change at the beginning of the pulse.

The negative pulse output of I-10-C is then applied to I-1, which is a decade counter. The D output of I-1 is connected to the input of I-2, the D output of I-2 is connected to the input of I-3, and the D output of I-3 is connected to the clock input of I-7-A, which is a J-K flip-flop. The D output of the decade counter makes the "1" to "0" transition only on a decimal 9 to 0 count; therefore, the D output may be used as the count input for the next counter without any external logic. The manner in which I-1, I-2, I-3, and I-7-A are connected constitutes a chained counter. As I-1, the 10^0 stage, recycles from 9 to 0 its D output goes from "1" to "0"; this then is a legitimate transition for I-2, the 10^1 stage, to count one pulse. Similarly I-3 counts once for every ten counts of I-2. I-7-A is a flip-flop connected so that it will change states on every clock pulse; it makes its transition

I-1 = SN7490 Decade Counter
I-2 = SN7490 Decade Counter
I-3 = SN7490 Decade Counter
I-4 = SN7442 BCD to Decimal Decoder
I-5 = SN7442 BCD to Decimal Decoder
I-6 = SN7442 BCD to Decimal Decoder
I-7 = SN7473 Dual J-K Flip-Flop
I-8 = SN7402 Quad 2-Input NOR
I-9 = SN7400 Quad 2-Input NAND
I-10 = SN7402 Quad 2-Input NOR
I-11 = SN7400 Quad 2-Input NAND
I-12 = SN74121 Monostable Multivibrator

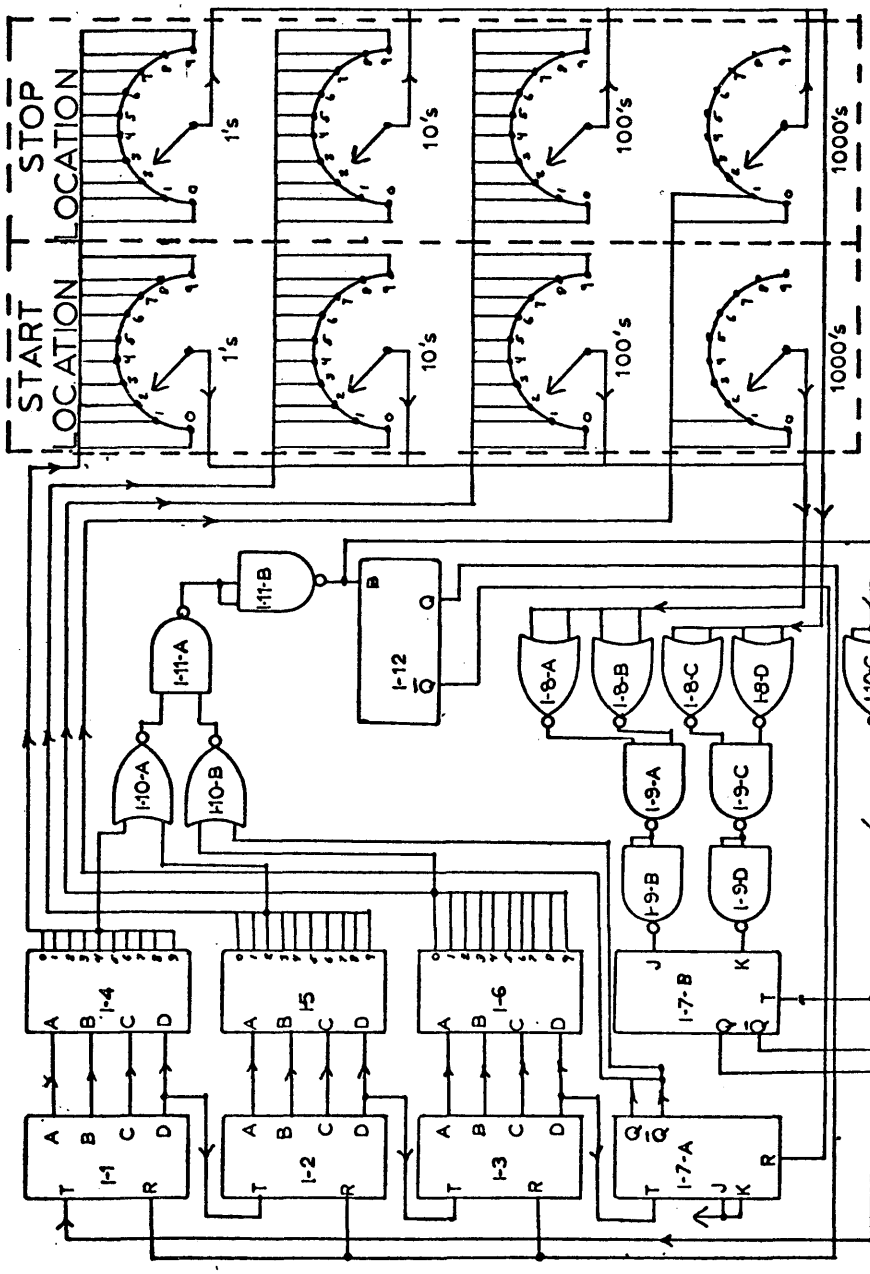


Figure 23

Memory Address Selector Logic Diagram

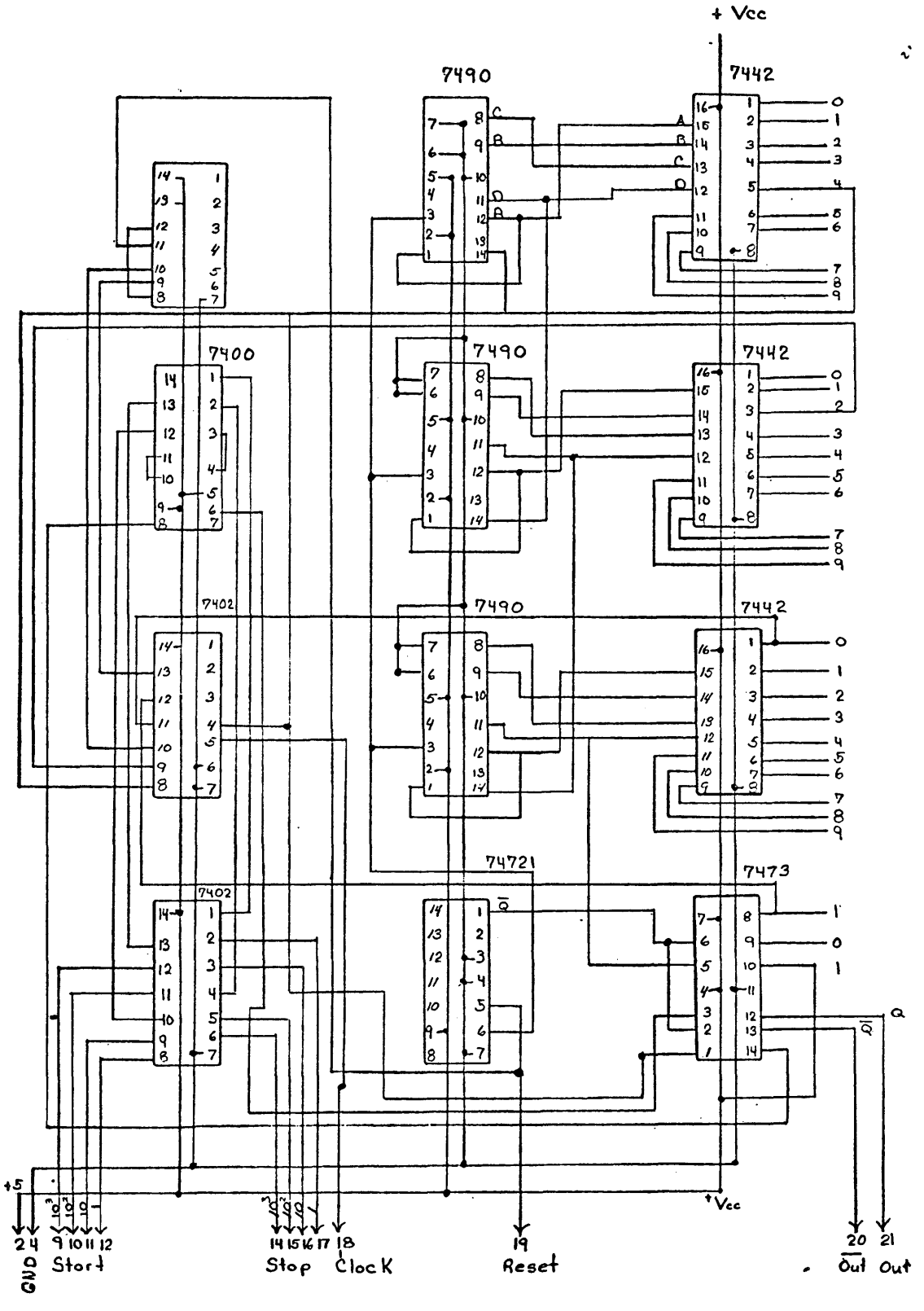


Figure 23-A Memory Address Selector Layout

Pin # 7 open

from 0 to 1 when I-3 counts from 9 to 0. These circuits make up a count to 1999 counter with I-1 being the units, I-2 being the tens, I-3 being the hundreds, and I-7-A being the thousands.

The A, B, C, and D outputs of the I-1, I-2, and I-3 are connected to the A, B, C, and D inputs of I-4, I-5, and I-6, respectively, which are BCD to Decimal Decoders. The decoders take the BCD input and generate a 10 line output of which one of the ten lines is at logic level "0", corresponding to the input BCD code, and the other nine outputs of the decoder are at logic level "1" These ten line outputs are then connected to the ten inputs of the thumbwheel switches. The wiper of the thumbwheel switch will then go from "1" to "0" when the terminal on which it is set goes from "1" to "0" Therefore if I-1 is at count 4 and if the units thumbwheel is at location 5, the output from the thumbwheel wiper will be at "1"; with the next pulse I-1 will go from 4 to 5 and the units thumbwheel wiper voltage will now go from "1" to "0", thereby indicating that I-1 is now at the location set into the units thumbwheel The tens and hundreds function in the same manner The thousands, since it only has two states, zero-thousand and one-thousand, does not need a decoder, and it is connected directly to the thousands thumbwheel switch.

The wiper outputs of the thumbwheel switches are connected as shown to the inputs of I-8-A & B which are two-input NOR gates. The outputs of these two gates, corresponding to the start location thumbwheel switches, are connected to the input of I-9-A, which is a NAND gate. The output of the NAND gate is then inverted by another NAND gate I-9-B. A Boolean expression for the logical operation performed above can be

written in terms of E which corresponds to the wiper for the units thumbwheel, F which corresponds to the wiper for the tens, G which corresponds to the wiper for the hundreds, and H which corresponds to the wiper for the thousands. The output of I-9-B has the expression

$$\overline{\overline{E+F} \cdot \overline{G+H}} = \overline{E+F+G+H}$$

The above operation corresponds to a single 4-input NOR gate. The characteristic of the NOR operation is that the output is "1" when all inputs are "0", and the output is "0" if any input is "1" Therefore the output of I-9-B will be at "1" when and only when the counters are at the location set into the start location thumbwheel switches

One of the inherent problems with chained decade counters is "ripple-through." The count on I-2 cannot change until the output of I-1 has changed and the typical delay through an SN7490 decade counter is 60 ns. The problem compounds itself as more decades are chained. A typical example of a ripple-through problem is displayed in Table 6.

Example of Ripple-Through

Time	0	60ns	120ns	180ns
I-1 state	9	0	0	0
I-2 state	9	9	0	0
I-3 state	7	7	7	8
I-4 state	0	0	0	0

Table 6

At 60 ns there is a false output of 790; at 120 ns there is a false output of 700; not until 180 ns is the correct value of the count 800 achieved. The two false counts of 790 and 700 could easily trigger a logic gate and give a false memory location.

To eliminate the ripple-through problem I-7-B, an SN7473 J-K flip-flop, is used so that the ripple-through is complete before the output of the memory address selector can possibly change. Its clock input pulses are derived from the inverted shift frequency for the shift registers.

The truth table for the SN7473 is given in Table 7[5]

Truth Table (each flip-flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Table 7

t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse

The SN7473 consists of two J-K master-slave flip-flops. The inputs to the master are governed by the clock pulse. The clock pulse also determines the state of the coupling between the master and slave. The operating sequence is

1. Isolate the slave from the master;
2. Enter information from J and K inputs into the master;
3. Disable J and K inputs;
4. Transfer the information from the master into the slave.

The above numbers refer to the clock wave form depicted in Figure 24.

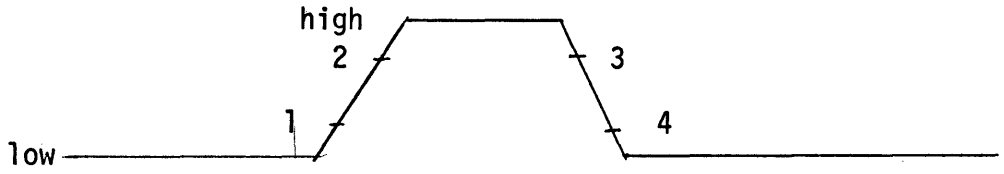


Figure 24

If the start location gate I-9-B is at "1" and the stop I-9-D is at "0" so that J = "1" and K = "0" on I-7-B, then on the t_{n+1} pulse Q assumes the value "1" The clock input is the inverted shift frequency as depicted in Figure 25.

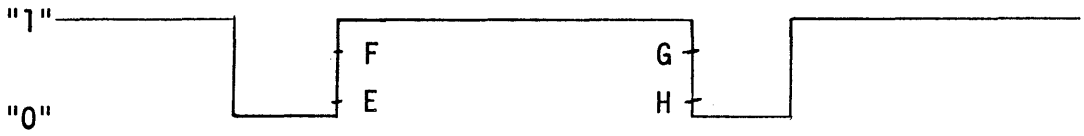


Figure 25

If J = "1" and K = "0" at point E then the slave is isolated from the master, and at F the values of J = "1" and K = "0" are entered into the master. At the beginning of the next clock pulse, point G, the J and K inputs are disabled and the value of J = "1" and K = "0" are transferred into the slave from the master, and Q changes from "0" to "1" at H. This method of using the J-K flip-flop eliminates the ripple-through problem that is inherent in the delays through the counters.

The Q output of I-7-B is now "1" and after the next count pulse J = "0" and K = "0"; therefore, Q of I-7-B will remain at "1"

The logic for the stop location circuit is identical to that of the start location. When the stop location is reached J = "0" and K = "1" At the proper time Q becomes "0" and remains at "0" until the next cycle starts the process over again.

Hard-wired into the memory address selector is a circuit that resets all counters when they reach 1024. The logic for the reset is the same as the logic for the start and stop location, except that the 1024 is hard-wired from the decoders rather than going through the thumbwheel switches. Therefore as the counters reach 1024 the output of I-11-B goes from "0" to "1", and this transition is applied to the "B" input of I-12, a monostable multivibrator, which generates a pulse of 30 ns width, determined by an internal R-C timing circuit. The Q pulse is used to reset the decade counters, and the $\overline{Q}$ is used to reset the J-K flip-flop I-7-A. No ripple-through problem is present in the reset circuits.

CHAPTER 6

HIGH-FREQUENCY VOLTAGE FOLLOWER

Introduction:

As a consequence of the development of the pulse stretcher a high-frequency voltage follower was designed. Advantages of the voltage follower are that output voltage is equal to input voltage, input impedance is high and output impedance low. A voltage follower is inherently unstable because of the large amount of feedback. Any delays or phase shifts are possible sources of instability. These instabilities are revealed in oscillation of the operational amplifier circuit.

To achieve the necessary high frequency response a high-frequency operational amplifier is needed. The SN 72702 operational amplifier was selected for this reason. This amplifier must be externally frequency compensated. To achieve maximum bandwidth the operational amplifier was frequency compensated in two ways: Lag compensation was used to add stability, and lead compensation was used to extend the bandwidth of the amplifier.

Frequency Compensation of the SN 72702 Operational Amplifier:

Lag Compensation: Oscillation of an operational amplifier circuit is determined by two factors: loop gain and phase shift. Phase shift is frequency dependent. If the phase shift is 180° or greater at frequencies for which the loop gain is greater than 1, negative feedback becomes positive. An operational amplifier with positive feedback will oscillate.

Lag compensation decreases the bandwidth of the operational amplifier. The effect of the lag compensation circuit on the operational amplifier can be analyzed by referring to Figure 26.

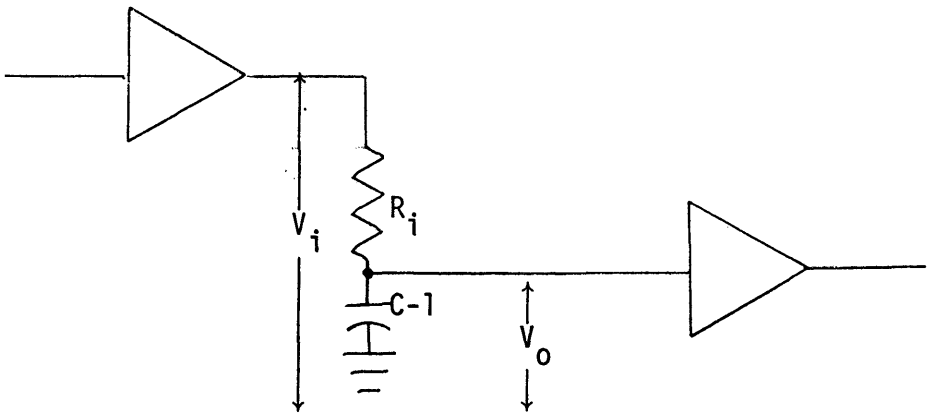


Figure 26

A lag compensation capacitor is inserted between two amplifier stages. The effect of lag compensation on the operational amplifier is given by the expression

$$V_0 = \frac{1}{1 + j\omega(C\text{-}1)R_i} V_i$$

The phase angle δ of output with respect to input is then

$$\delta = \text{Tan}^{-1}[-\omega R_i(C\text{-}1)]$$

so that δ is zero at low frequencies and becomes $-\pi/2$ at high frequencies.

The total phase shift in the negative feedback loop is the sum of the phase shift δ due to compensation and that of the operational amplifier, $\phi(\omega)$. A typical response curve for phase shift $\phi(\omega)$ as a function of frequency for the SN 72702 operational amplifier is given in Figure 27[6]

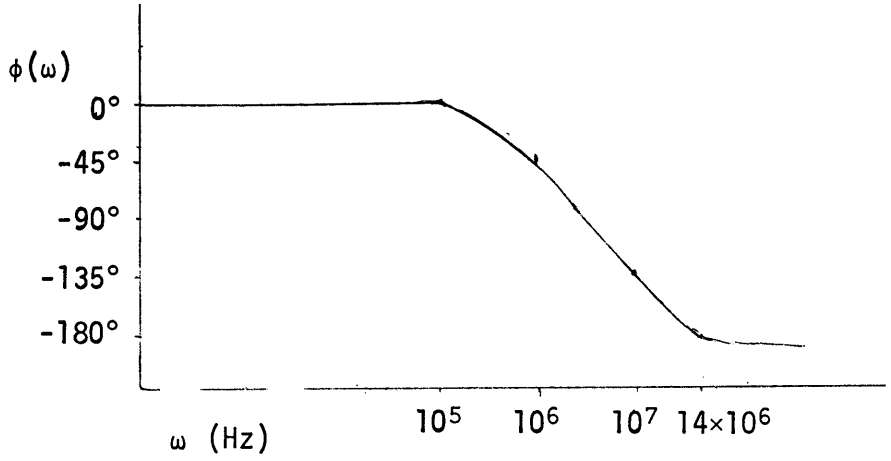


Figure 27

The operational amplifier circuit will be stable if the loop gain G is less than one when $|\phi(\omega) + \delta|$ is 180° Consequently at frequencies for which $|\phi(\omega) + \delta| \geq 180°$ α must be less than 1/G. If G is large at these frequencies this restriction on α is stringent. Since the gain G is frequency dependent, one can use the natural rolloff of the gain along with that of the compensation capacitor in frequency compensation. This simple lag compensation is normally employed when the operational amplifier is used in low-frequency applications.

To increase the bandwidth of the circuit the lag compensation network of Figure 28 is employed.

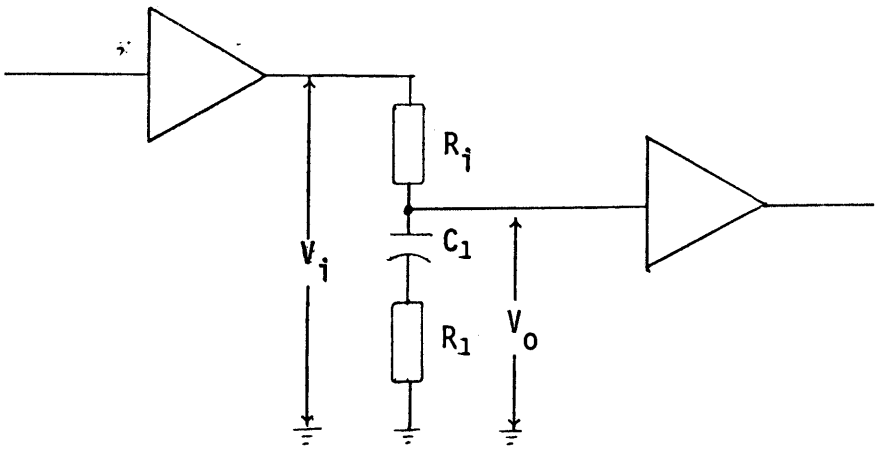


Figure 28

The R_1C_1 network is inserted before the output stage of the operational amplifier.

At $\omega = 0$ the capacitor is an infinite impedance and $V_i = V_o$.

As $\omega \to \infty$ the capacitor appears to be a short circuit and

$$V_o = \frac{R_1}{R_1 + R_i} V_i$$

This compensation network inserts a step in the loop gain of the circuit, as shown in Figure 29, rather than decreasing the loop gain monotonically as is characteristic of the simple capacitor lag compensation circuit.

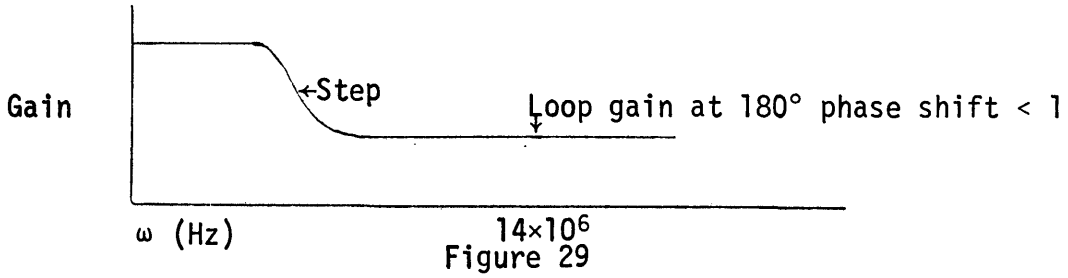
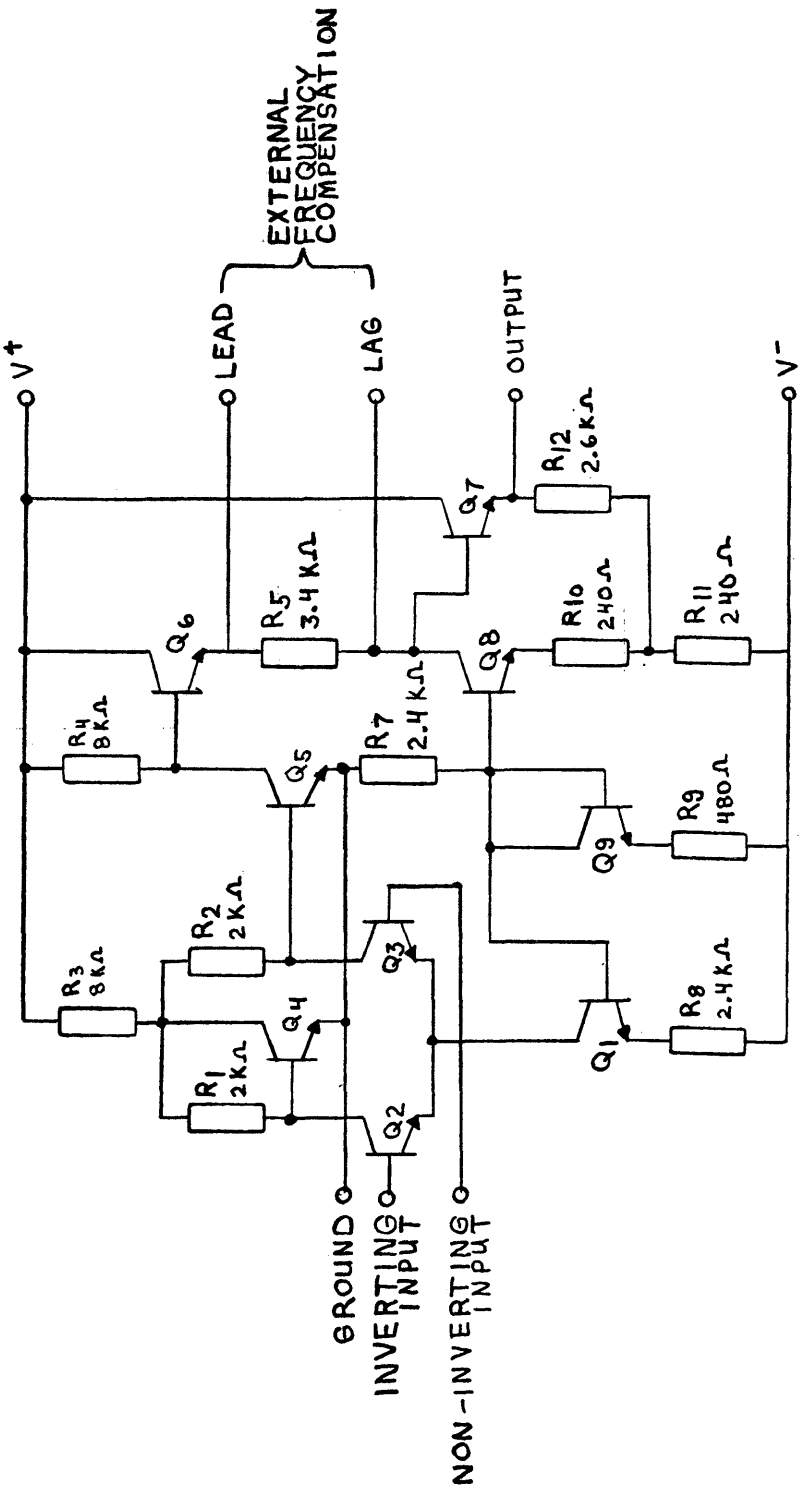


Figure 29

The size of the step must be such that the loop gain is less than 1 at the 180° phase shift point of the circuit..



Schematic Diagram - SN72702 Operational Amplifier[7]

Figure 30

The compensation circuit will affect the slew rate limit of the circuit least by being placed at the input to the operational amplifier. When the compensation circuit is placed between stages near the output of the amplifier, one stage of the amplifier must provide the current to charge the capacitor. The current required is large because the signal is large here. The constant current charging of the capacitor by the current-limited amplifier gives the linear change in output voltage characteristic of slew rate limiting. However, if the lag compensation network is placed across the input terminals of the operational amplifier where the signal voltage is small, the current required is small, and slew-rate limiting is reduced.

Lead Compensation: Figure 30 shows the circuit of the SN 72702 operational amplifier. Lead compensation increases the bandwidth of the operational amplifier by placing a capacitor in parallel with R_i in the stage preceding the output stage. The equivalent circuit for this compensation is shown below in Figure 31

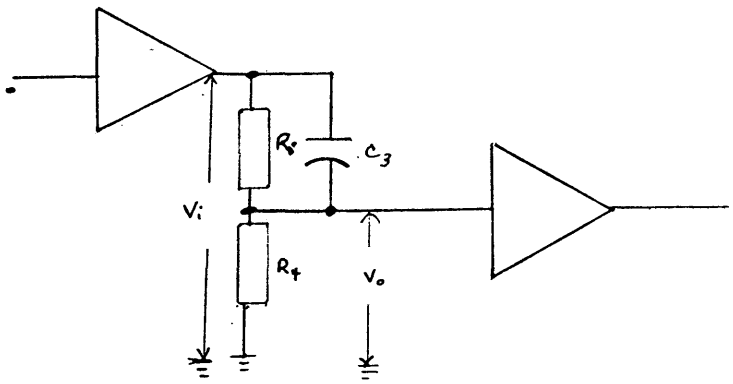


Figure 31

R_4 is the input impedance of the emitter follower, which is very large. The AC analysis of the circuit operation is as follows:

$$V_o = \frac{R_4}{R_4 + \dfrac{R_i/j\omega C_3}{R_i + 1/j\omega C_3}} V_i$$

After appropriate simplification the ratio of output voltage to input voltage is given by

$$\frac{V_o}{V_i} = \frac{[R_4(R_4 + R_i) + \omega^2 C_3^2 R_4^2 R_i^2] + j[\omega C_3 (R_4 R_i)(R_4 + R_i) - \omega C_3 R_4^2 R_i]}{(R_4 + R_i)^2 + R_4^2 R_i^2 \omega^2 C_3^2};$$

and the phase angle δ is given by

$$\delta = \text{Tan}^{-1}\left\{\frac{\omega C_3 R_4 R_i^2}{R_4(R_4 + R_i) + \omega^2 C_3^2 R_4^2 R_i^2}\right\}.$$

The resistor R_4 is much greater than R_i consequently

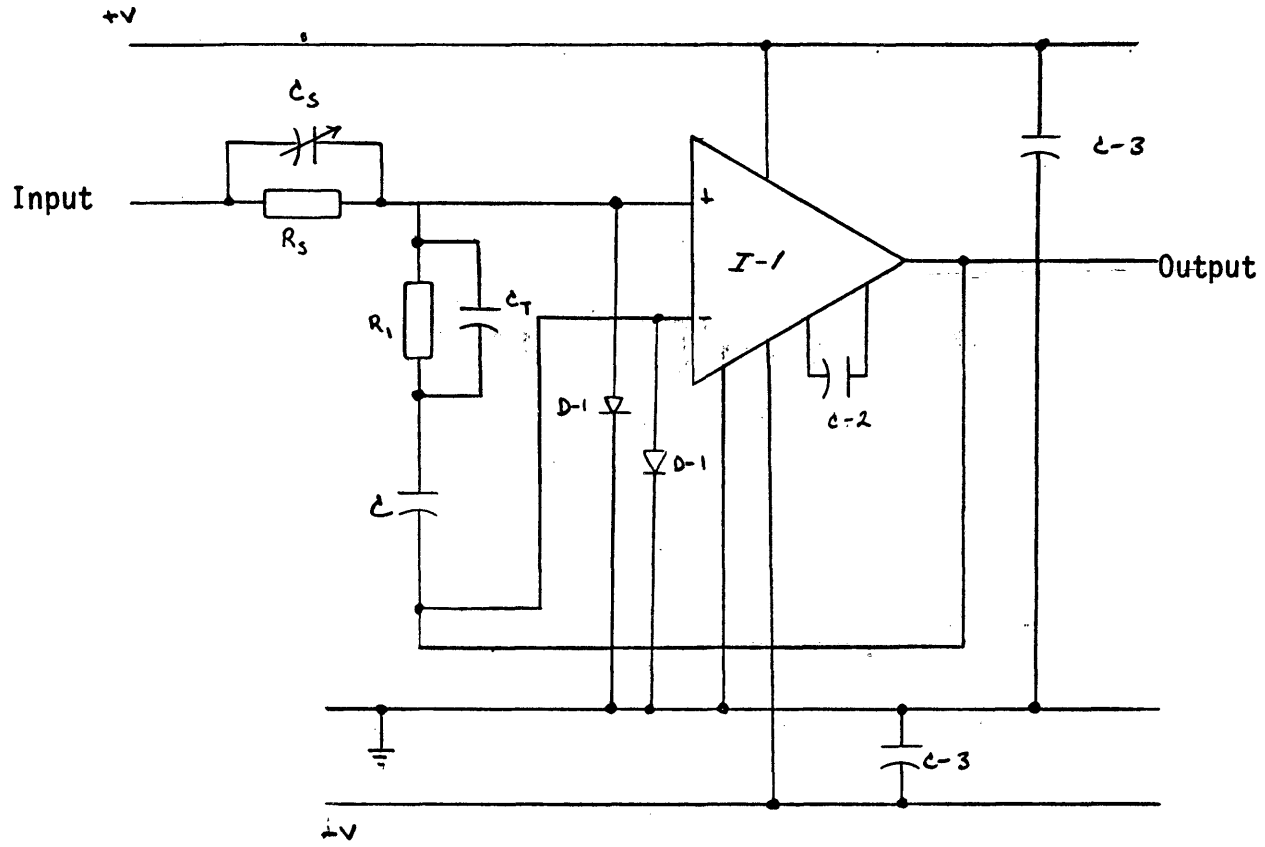
$$\delta = \text{Tan}^{-1}\left\{\frac{\omega C_3 R_i^2}{R_4(1 + \omega^2 C_3^2 R_i^2)}\right\}.$$

There is no phase shift for $\omega = 0$ or $\omega \to \infty$. The phase shift δ is greater than zero for values of ω between 0 and ∞; consequently,

$$\text{total phase shift} = \phi(\omega) + \delta.$$

There is a decrease in the amount of total phase shift because δ is positive and $\phi(\omega)$ is negative (see Figure 27).

The lead capacitor allows the amplifier to be used at higher frequencies because it moves the 180° phase shift point to higher frequencies. This compensation effectively increases the bandwidth of the operational amplifier; it still may be necessary, however, to reduce the gain at the 180° phase shift point to make the circuit stable.



C_s = 26 pf R_s = 10 K D-1 = DR 352 I-1 = SN72702 OPAMP

C_t = .005 mfd R_1 = 50

C = .005 mfd

C-2 = 50 pf -V = -6 volts +V = +12 volts

C-3 = 1 mfd

High Frequency Voltage Follower

Figure 32

Voltage Follower Circuit:

Description: Figure 32 shows a high frequency voltage follower circuit using both lead and lag compensation. The SN72702 operational amplifier is used in this circuit because the bandwidth of the operational amplifier may be extended to 15 MHz by using lead compensation.

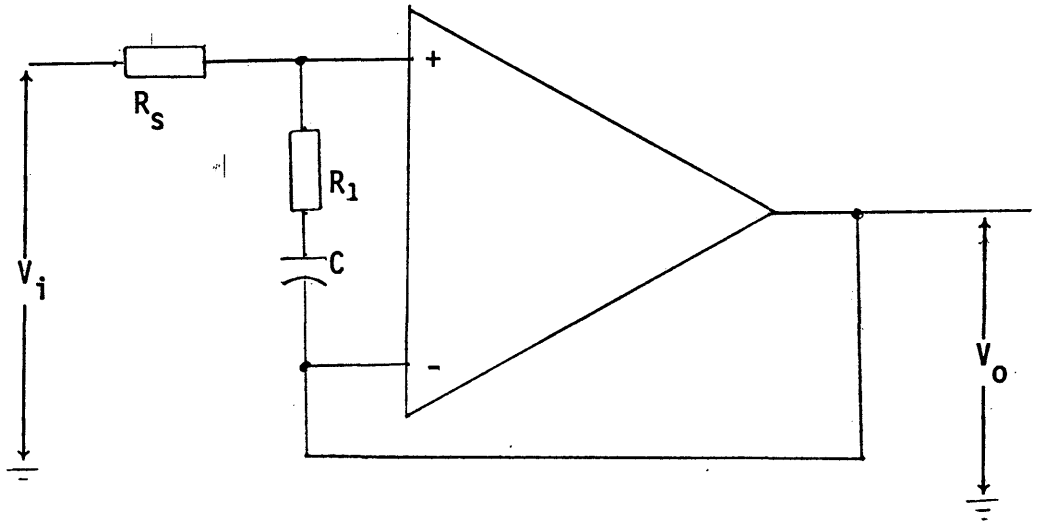


Figure 33

The circuit of Figure 33 is the basic voltage follower. The capacitor C and the resistors R_1 and R_s constitute the lag compensation network.

At DC the capacitor C is an infinite impedance, and the circuit is a conventional voltage follower.

The analysis of the AC response of the circuit follows. Let the voltage at the non-inverting input be V_+ and the voltage at the inverting input be V_-. The output voltage V_o of the circuit is $G[V_+ - V_-]$. The negative feedback makes $V_- = V_o$. Using the principle of superposition the value of V_+ is given by

$$V_+ = \frac{R_1 + 1/j\omega C}{R_1 + R_s + 1/j\omega C} V_i + \frac{R_s}{R_1 + R_s + 1/j\omega C} V_o.$$

Let

$$\alpha = \frac{R_1 + 1/j\omega C}{R_1 + R_s + 1/j\omega C},$$

then

$$V_o = \frac{\alpha G}{1 + \alpha G} V_i \qquad (5\text{-}1)$$

For large values of the gain G of the operational amplifier, the output voltage is equal to the input voltage.

As $\omega \to \infty$ the value of α is equal to $R_1/(R_s + R_1)$, supplying the necessary step in the loop gain for stable operation of the operational amplifier. This step in the loop gain must occur before the 180° phase shift point of the operational amplifier. From the specification sheets for the SN72702 operational amplifier the value of the open-loop gain G with lead compensation at 11 MHz, the 135° phase shift frequency is approximately equal to 100. The 135° phase shift point is selected to give a 45° phase margin for added security. The loop gain of the circuit with the lag compensation network is αG. Therefore, αG must be less than or equal to 1/100 at 11 MHz.

This circuit was highly unstable because of the effects of stray capacitance across the resistor R_s. Figure 32 shows the components that were added to compensate for the non-ideal effects of some of the components.

In Equation 5-1, the value of α changes because of the stray capacitance C_s across R_s, as follows:

$$\alpha = \frac{R_1 + \dfrac{1}{j\omega C}}{R_1 + \dfrac{1}{j\omega C} + \dfrac{R_s}{1 + j\omega C_s R_s}}.$$

Simplification of this expression yields:

$$\alpha = \frac{(1 - \omega^2 R_1 C R_s C_s) + j(\omega R_1 C + \omega R_s C_s)}{(1 - \omega^2 R_1 C R_s C_s) + j(\omega R_1 C + \omega R_s C_s + \omega R_s C)}.$$

The effect of the stray capacitance C_s is to make the value of α equal to 1 at high frequencies. The value of α must be 1/100 at the 45° phase margin point. Because the value of α is 1 rather than 1/100 the circuit is unstable and oscillates.

To compensate for the effect of the stray capacitance C_s, capacitor C_t was added in parallel with resistor R_1 The addition of capacitor C_t changes the value of α in the following way:

$$\alpha = \frac{\dfrac{1}{j\omega C} + \dfrac{R_1/j\omega C_t}{R_1 + 1/j\omega C_t}}{\dfrac{R_1/j\omega C_t}{R_1 + 1/j\omega C_t} + \dfrac{1}{j\omega C} + \dfrac{R_s/j\omega C_s}{R_s + 1/j\omega C_s}};$$

which can be shown to be equal to

$$\frac{(1 - \omega^2 C_t R_1 C_s R_s - \omega^2 C C_s R_1 R_s) + j(\omega C_t R_1 + \omega C R_1 + \omega C_s R_s)}{(1 - \omega^2 C C_s R_s R_1 - \omega^2 C_s R_s C_t R_1 - \omega^2 C_t C R_1 R_s) + j(\omega C R_1 + \omega C_t R_1 + \omega C_s R_s + \omega C R_s)},$$

after appropriate simplification. By arbitrarily letting $R_s C_s = R_1 C_t$, the value of α may be further simplified to

$$\alpha = \frac{(1 - \omega^2 C_s^2 R_s^2 - \omega^2 C_s R_s C R_1) + j(\omega C_s R_s + \omega C R_1 + \omega R_s C_s)}{(1 - \omega^2 C_s R_s C R_1 - \omega^2 C_s^2 R_s^2 - \omega^2 C_s R_s^2 C) + j(\omega C R_1 + 2\omega R_s C_s + \omega C R_s)}. \quad (5\text{-}2)$$

In the limit of $\omega \to \infty$, α assumes the value

$$\alpha' = \frac{C_s R_s + C R_1}{C_s R_s + C(R_1 + R_s)}.$$

By making $R_s C_s \ll R_1 C$ the circuit becomes more independent of the stray capacitance; therefore, α is $R_1/(R_1 + R_s)$.

Under the assumptions made, the conditions for stable operation of the voltage follower circuit are

1. $R_1 C_t = R_s C_s$,
2. $R_s C_s \ll C R_1$,
3. $\dfrac{R_1}{R_1 + R_s} < \dfrac{1}{100}$.

These conditions have to be satisfied in addition to allowing values that will give a large bandwidth for the voltage follower.

The two diodes D-1 are inserted between the inputs of the operational amplifier and ground to prevent latch-up. If the input voltage on the inverting input exceeds $2V_{be}$, the input stage saturates. When this condition exists the inverting input acts as a non-inverting input, and the negative feedback becomes positive feedback. This condition saturates the operational amplifier and may cause excessive current to flow through the output transistor. The diodes prevent the inputs of the operational amplifier from assuming a potential of more than one diode-junction turn-on voltage above ground, eliminating latch-up.

Capacitor C-2 is the lead compensation capacitor used to extend the bandwidth of the operational amplifier and has been experimentally determined, for maximum bandwidth and stability, to be equal to 50 pf

The capacitors C-3 are used to bypass the power supplies at the operational amplifier. These capacitors add stability to the circuit by removing the effects of the power supply lead inductance.

The SN72702 operational amplifier is biased between -6 volts and +12 volts. The unbalanced power supply voltages are suggested operating voltages; however, the 2-to-1 ratio between the power supply voltages does not have to be strictly maintained.

Computer Modeling: A computer program, listed as Figure 34, was used to optimize the component values. The component values are initially entered into the program. Optimization involves determining the correct values for the components for stable operation and large bandwidth of the voltage follower.

From Equation 5-2 the computer program calculates the magnitude of α and δ, the phase angle of α, as a function of the angular frequency ω.

The results of the program are plotted in Figure 35 for the final values of the components (these values are listed in the program, Figure 34). The results of the computer program are listed in Figure 36.

The values of the components are

$R_1 = 50\ \Omega$

$R_s = 10\ K\Omega$

$C_t = 0.005$ mfd

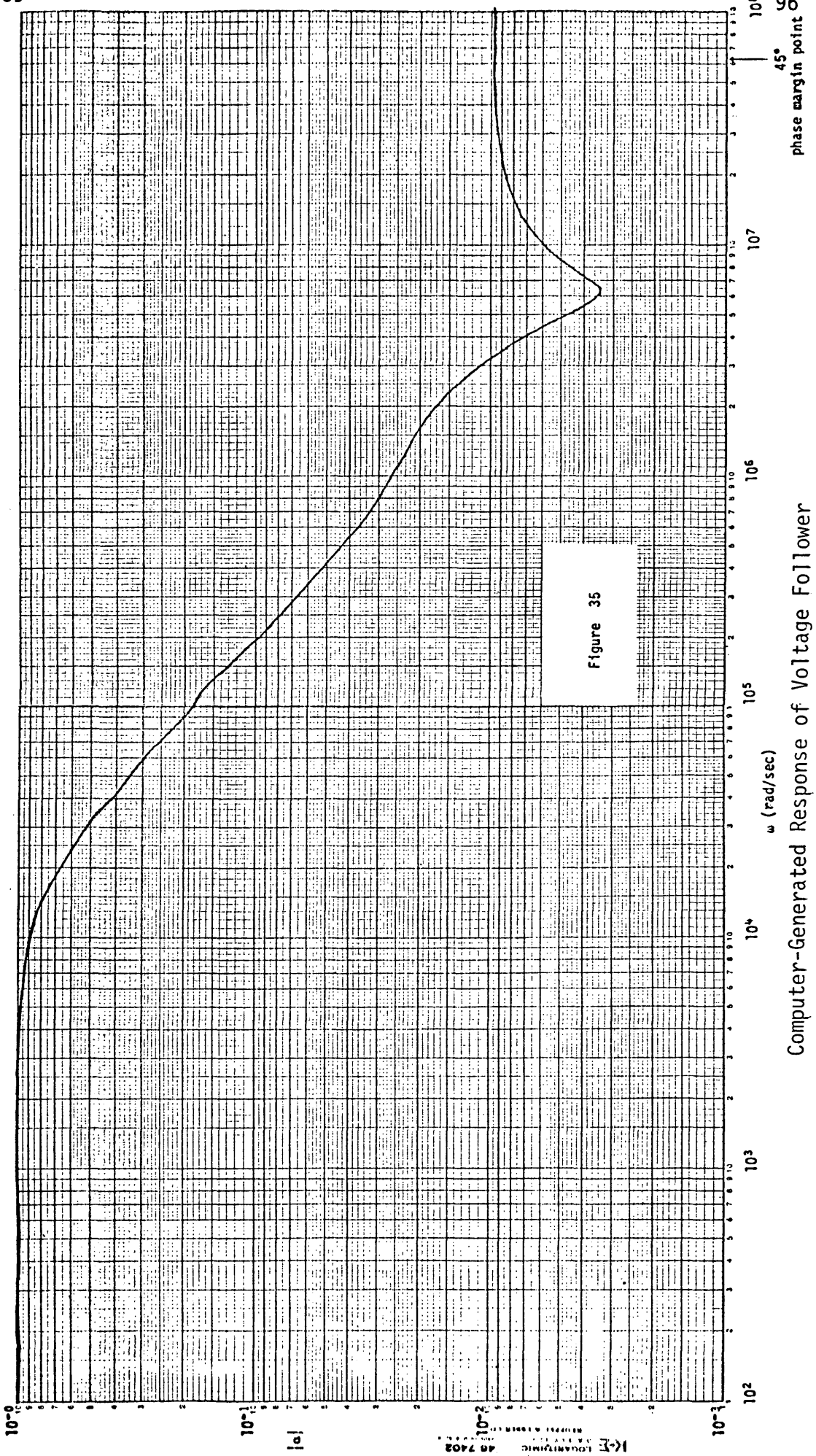
$C = 0.005$ mfd

$C_s = 26$ pf (trimmer capacitor).

```
.TYPE CØMP.F4
[15:43:15]
        DIMENSIØN ALP(100),PHI(100),W(100)
1000    FØRMAT (3E20.8)
        R1=50.
        CT=5000.*(10.**-12.)
        C=.005*(10.**-6.)
        RS= 10000.
        PI=3.1415926535
C N= STARTING W
        N=1000000
C M= ENDPØINT W
        M=9900000
C L= INCREMENT ØF W
        L=100000
        DØ 100 IN=N,M,L
        I=I+1
        AA=IN
C W(I)=AA/1000... IS AN ADDED SCALE FACTØR FØR SMALL W
        W(I)=AA/1000.
        A=(W(I)*R1*CT)**2.
        B=C*CT*((W(I)*R1)**2.)
        D=CT*R1*RS*C*W(I)*W(I)
        E=W(I)*CT*R1
        F=W(I)*C*R1
        G=W(I)*C*RS
        Ø=1.-A-B
        P=1.-B-A-D
        Q=(2.*E)+F
        R=(2.*E)+F+G
        X=(Ø*P)-(Q*R)
        Y=(Q*P)-(R*Ø)
        WRITE(2,1000)X,Y
        WRITE(2,1000)A,B,D
        WRITE(2,1000)E,F,G
        WRITE(2,1000)Ø,P,Q
        WRITE(2,1000)R
        ALP(I)=SQRT(((X*X)+(Y*Y))/(((P*P)+(R*R))**2.))
100     PHI(I)=(180./PI)*ATAN(Y/X)
        WRITE(1,1000)(W(IM),ALP(IM),PHI(IM),IM=1,I)
        END
.
```

Voltage Follower - Frequency Compensation

Figure 34



Computer-Generated Response of Voltage Follower

ω (rad/sec)	|α|	δ (deg)
0.10000000E+04	0.99865159E+00	-0.28625506E+01
0.11000000E+04	0.99836913E+00	-0.31482894E+01
0.12000000E+04	0.99806002E+00	-0.34338813E+01
0.13000000E+04	0.99772435E+00	-0.37193127E+01
0.14000000E+04	0.99736224E+00	-0.40045708E+01
0.15000000E+04	0.99697372E+00	-0.42896424E+01
0.16000000E+04	0.99655890E+00	-0.45745143E+01
0.17000000E+04	0.99611790E+00	-0.48591738E+01
0.18000000E+04	0.99565078E+00	-0.51436078E+01
0.19000000E+04	0.99515772E+00	-0.54278033E+01
0.20000000E+04	0.99463878E+00	-0.57117478E+01
0.21000000E+04	0.99409409E+00	-0.59954282E+01
0.22000000E+04	0.99352378E+00	-0.62788321E+01
0.23000000E+04	0.99292801E+00	-0.65619469E+01
0.24000000E+04	0.99230688E+00	-0.68447599E+01
0.25000000E+04	0.99166057E+00	-0.71272590E+01
0.26000000E+04	0.99098920E+00	-0.74094317E+01
0.27000000E+04	0.99029297E+00	-0.76912659E+01
0.28000000E+04	0.98957198E+00	-0.79727494E+01
0.29000000E+04	0.98882644E+00	-0.82538700E+01
0.30000000E+04	0.98805649E+00	-0.85346154E+01
0.31000000E+04	0.98726234E+00	-0.88149748E+01
0.32000000E+04	0.98644415E+00	-0.90949355E+01
0.33000000E+04	0.98560210E+00	-0.93744862E+01
0.34000000E+04	0.98473639E+00	-0.96536157E+01
0.35000000E+04	0.98384721E+00	-0.99323121E+01
0.36000000E+04	0.98293475E+00	-0.10210564E+02
0.37000000E+04	0.98199922E+00	-0.10488361E+02
0.38000000E+04	0.98104084E+00	-0.10765691E+02
0.39000000E+04	0.98005979E+00	-0.11042544E+02
0.40000000E+04	0.97905631E+00	-0.11318908E+02
0.41000000E+04	0.97803061E+00	-0.11594774E+02
0.42000000E+04	0.97698291E+00	-0.11870130E+02
0.43000000E+04	0.97591343E+00	-0.12144966E+02
0.44000000E+04	0.97482239E+00	-0.12419272E+02
0.45000000E+04	0.97371005E+00	-0.12693037E+02
0.46000000E+04	0.97257664E+00	-0.12966252E+02
0.47000000E+04	0.97142237E+00	-0.13238906E+02
0.48000000E+04	0.97024749E+00	-0.13510990E+02
0.49000000E+04	0.96905226E+00	-0.13782495E+02
0.50000000E+04	0.96783691E+00	-0.14053411E+02
0.51000000E+04	0.96660171E+00	-0.14323727E+02
0.52000000E+04	0.96534687E+00	-0.14593436E+02
0.53000000E+04	0.96407266E+00	-0.14862528E+02
0.54000000E+04	0.96277934E+00	-0.15130995E+02

Figure 36 (a)

ω (rad/sec)	|α|	δ (deg)
0.55000000E+04	0.96146718E+00	-0.15398827E+02
0.56000000E+04	0.96013643E+00	-0.15666015E+02
0.57000000E+04	0.95878733E+00	-0.15932553E+02
0.58000000E+04	0.95742017E+00	-0.16198431E+02
0.59000000E+04	0.95603518E+00	-0.16463640E+02
0.60000000E+04	0.95463266E+00	-0.16728174E+02
0.61000000E+04	0.95321285E+00	-0.16992024E+02
0.62000000E+04	0.95177604E+00	-0.17255183E+02
0.63000000E+04	0.95032247E+00	-0.17517642E+02
0.64000000E+04	0.94885242E+00	-0.17779394E+02
0.65000000E+04	0.94736618E+00	-0.18040433E+02
0.66000000E+04	0.94586399E+00	-0.18300751E+02
0.67000000E+04	0.94434612E+00	-0.18560342E+02
0.68000000E+04	0.94281287E+00	-0.18819198E+02
0.69000000E+04	0.94126449E+00	-0.19077313E+02
0.70000000E+04	0.93970124E+00	-0.19334680E+02
0.71000000E+04	0.93812342E+00	-0.19591293E+02
0.72000000E+04	0.93653128E+00	-0.19847147E+02
0.73000000E+04	0.93492510E+00	-0.20102234E+02
0.74000000E+04	0.93330515E+00	-0.20356548E+02
0.75000000E+04	0.93167169E+00	-0.20610086E+02
0.76000000E+04	0.93002502E+00	-0.20862840E+02
0.77000000E+04	0.92836537E+00	-0.21114806E+02
0.78000000E+04	0.92669304E+00	-0.21365977E+02
0.79000000E+04	0.92500828E+00	-0.21616350E+02
0.80000000E+04	0.92331135E+00	-0.21865919E+02
0.81000000E+04	0.92160255E+00	-0.22114679E+02
0.82000000E+04	0.91988213E+00	-0.22362625E+02
0.83000000E+04	0.91815034E+00	-0.22609754E+02
0.84000000E+04	0.91640747E+00	-0.22856060E+02
0.85000000E+04	0.91465375E+00	-0.23101540E+02
0.86000000E+04	0.91288947E+00	-0.23346189E+02
0.87000000E+04	0.91111487E+00	-0.23590005E+02
0.88000000E+04	0.90933023E+00	-0.23832981E+02
0.89000000E+04	0.90753578E+00	-0.24075115E+02
0.90000000E+04	0.90573179E+00	-0.24316404E+02
0.91000000E+04	0.90391852E+00	-0.24556845E+02
0.92000000E+04	0.90209622E+00	-0.24796433E+02
0.93000000E+04	0.90026512E+00	-0.25035166E+02
0.94000000E+04	0.89842550E+00	-0.25273041E+02
0.95000000E+04	0.89657757E+00	-0.25510055E+02
0.96000000E+04	0.89472160E+00	-0.25746205E+02
0.97000000E+04	0.89285784E+00	-0.25981490E+02
0.98000000E+04	0.89098652E+00	-0.26215906E+02
0.99000000E+04	0.88910787E+00	-0.26449451E+02

Figure 36 (b)

ω (rad/sec)	|α|	δ (deg)
0.10000000E+05	0.88722214E+00	-0.26682123E+02
0.11000000E+05	0.86802571E+00	-0.28960433E+02
0.12000000E+05	0.84836459E+00	-0.31149939E+02
0.13000000E+05	0.82843677E+00	-0.33250331E+02
0.14000000E+05	0.80841487E+00	-0.35262228E+02
0.15000000E+05	0.78844630E+00	-0.37187021E+02
0.16000000E+05	0.76865436E+00	-0.39026718E+02
0.17000000E+05	0.74914005E+00	-0.40783800E+02
0.18000000E+05	0.72998420E+00	-0.42461111E+02
0.19000000E+05	0.71124990E+00	-0.44061739E+02
0.20000000E+05	0.69298473E+00	-0.45588935E+02
0.21000000E+05	0.67522307E+00	-0.47046027E+02
0.22000000E+05	0.65798826E+00	-0.48436374E+02
0.23000000E+05	0.64129436E+00	-0.49763307E+02
0.24000000E+05	0.62514791E+00	-0.51030097E+02
0.25000000E+05	0.60954934E+00	-0.52239927E+02
0.26000000E+05	0.59449422E+00	-0.53395868E+02
0.27000000E+05	0.57997435E+00	-0.54500872E+02
0.28000000E+05	0.56597854E+00	-0.55557756E+02
0.29000000E+05	0.55249345E+00	-0.56569203E+02
0.30000000E+05	0.53950417E+00	-0.57537757E+02
0.31000000E+05	0.52699467E+00	-0.58465822E+02
0.32000000E+05	0.51494819E+00	-0.59355672E+02
0.33000000E+05	0.50334767E+00	-0.60209445E+02
0.34000000E+05	0.49217587E+00	-0.61029155E+02
0.35000000E+05	0.48141560E+00	-0.61816697E+02
0.36000000E+05	0.47104998E+00	-0.62573848E+02
0.37000000E+05	0.46106241E+00	-0.63302275E+02
0.38000000E+05	0.45143672E+00	-0.64003545E+02
0.39000000E+05	0.44215725E+00	-0.64679126E+02
0.40000000E+05	0.43320890E+00	-0.65330394E+02
0.41000000E+05	0.42457709E+00	-0.65958640E+02
0.42000000E+05	0.41624785E+00	-0.66565077E+02
0.43000000E+05	0.40820779E+00	-0.67150838E+02
0.44000000E+05	0.40044409E+00	-0.67716989E+02
0.45000000E+05	0.39294452E+00	-0.68264530E+02
0.46000000E+05	0.38569743E+00	-0.68794401E+02
0.47000000E+05	0.37869168E+00	-0.69307483E+02
0.48000000E+05	0.37191669E+00	-0.69804601E+02
0.49000000E+05	0.36536235E+00	-0.70286537E+02
0.50000000E+05	0.35901914E+00	-0.70754022E+02
0.51000000E+05	0.35287790E+00	-0.71207743E+02
0.52000000E+05	0.34692998E+00	-0.71648349E+02
0.53000000E+05	0.34116714E+00	-0.72076451E+02
0.54000000E+05	0.33558157E+00	-0.72492623E+02

Figure 36 (c)

ω (rad/sec)	|α|	δ (deg)
0.55000000E+05	0.33016581E+00	-0.72897408E+02
0.56000000E+05	0.32491282E+00	-0.73291318E+02
0.57000000E+05	0.31981586E+00	-0.73674834E+02
0.58000000E+05	0.31486854E+00	-0.74048414E+02
0.59000000E+05	0.31006480E+00	-0.74412488E+02
0.60000000E+05	0.30539888E+00	-0.74767464E+02
0.61000000E+05	0.30086526E+00	-0.75113725E+02
0.62000000E+05	0.29645872E+00	-0.75451638E+02
0.63000000E+05	0.29217430E+00	-0.75781548E+02
0.64000000E+05	0.28800725E+00	-0.76103783E+02
0.65000000E+05	0.28395308E+00	-0.76418651E+02
0.66000000E+05	0.28000748E+00	-0.76726448E+02
0.67000000E+05	0.27616637E+00	-0.77027452E+02
0.68000000E+05	0.27242585E+00	-0.77321932E+02
0.69000000E+05	0.26878219E+00	-0.77610136E+02
0.70000000E+05	0.26523184E+00	-0.77892304E+02
0.71000000E+05	0.26177144E+00	-0.78168667E+02
0.72000000E+05	0.25839774E+00	-0.78439440E+02
0.73000000E+05	0.25510766E+00	-0.78704827E+02
0.74000000E+05	0.25189825E+00	-0.78965029E+02
0.75000000E+05	0.24876669E+00	-0.79220230E+02
0.76000000E+05	0.24571030E+00	-0.79470612E+02
0.77000000E+05	0.24272651E+00	-0.79716342E+02
0.78000000E+05	0.23981284E+00	-0.79957584E+02
0.79000000E+05	0.23696695E+00	-0.80194494E+02
0.80000000E+05	0.23418657E+00	-0.80427221E+02
0.81000000E+05	0.23146954E+00	-0.80655906E+02
0.82000000E+05	0.22881381E+00	-0.80880683E+02
0.83000000E+05	0.22621738E+00	-0.81101683E+02
0.84000000E+05	0.22367834E+00	-0.81319031E+02
0.85000000E+05	0.22119488E+00	-0.81532844E+02
0.86000000E+05	0.21876526E+00	-0.81743237E+02
0.87000000E+05	0.21638779E+00	-0.81950318E+02
0.88000000E+05	0.21406085E+00	-0.82154194E+02
0.89000000E+05	0.21178290E+00	-0.82354961E+02
0.90000000E+05	0.20955245E+00	-0.82552719E+02
0.91000000E+05	0.20736807E+00	-0.82747558E+02
0.92000000E+05	0.20522840E+00	-0.82939567E+02
0.93000000E+05	0.20313210E+00	-0.83128832E+02
0.94000000E+05	0.20107790E+00	-0.83315433E+02
0.95000000E+05	0.19906459E+00	-0.83499449E+02
0.96000000E+05	0.19709100E+00	-0.83680956E+02
0.97000000E+05	0.19515597E+00	-0.83860026E+02
0.98000000E+05	0.19325842E+00	-0.84036730E+02
0.99000000E+05	0.19139730E+00	-0.84211134E+02

Figure 36 (d)

ω (rad/sec)	|α|	δ (deg)
0.10000000E+06	0.18957160E+00	-0.84383303E+02
0.11000000E+06	0.17306365E+00	-0.85994702E+02
0.12000000E+06	0.15921067E+00	-0.87438813E+02
0.13000000E+06	0.14742984E+00	-0.88752296E+02
0.14000000E+06	0.13729558E+00	-0.89961731E+02
0.15000000E+06	0.12849040E+00	0.88913176E+02
0.16000000E+06	0.12077284E+00	0.87857516E+02
0.17000000E+06	0.11395620E+00	0.86859828E+02
0.18000000E+06	0.10789395E+00	0.85911164E+02
0.19000000E+06	0.10246950E+00	0.85004437E+02
0.20000000E+06	0.97588971E-01	0.84133978E+02
0.21000000E+06	0.93175959E-01	0.83295192E+02
0.22000000E+06	0.89167656E-01	0.82484331E+02
0.23000000E+06	0.85511962E-01	0.81698300E+02
0.24000000E+06	0.82165307E-01	0.80934532E+02
0.25000000E+06	0.79090980E-01	0.80190878E+02
0.26000000E+06	0.76257826E-01	0.79465526E+02
0.27000000E+06	0.73639249E-01	0.78756940E+02
0.28000000E+06	0.71212393E-01	0.78063815E+02
0.29000000E+06	0.68957523E-01	0.77385029E+02
0.30000000E+06	0.66857502E-01	0.76719619E+02
0.31000000E+06	0.64897380E-01	0.76066748E+02
0.32000000E+06	0.63064055E-01	0.75425692E+02
0.33000000E+06	0.61345999E-01	0.74795815E+02
0.34000000E+06	0.59733026E-01	0.74176567E+02
0.35000000E+06	0.58216109E-01	0.73567456E+02
0.36000000E+06	0.56787209E-01	0.72968053E+02
0.37000000E+06	0.55439154E-01	0.72377973E+02
0.38000000E+06	0.54165517E-01	0.71796877E+02
0.39000000E+06	0.52960529E-01	0.71224458E+02
0.40000000E+06	0.51818989E-01	0.70660443E+02
0.41000000E+06	0.50736208E-01	0.70104587E+02
0.42000000E+06	0.49707931E-01	0.69556664E+02
0.43000000E+06	0.48730304E-01	0.69016473E+02
0.44000000E+06	0.47799820E-01	0.68483829E+02
0.45000000E+06	0.46913278E-01	0.67958561E+02
0.46000000E+06	0.46067758E-01	0.67440512E+02
0.47000000E+06	0.45260587E-01	0.66929540E+02
0.48000000E+06	0.44489312E-01	0.66425508E+02
0.49000000E+06	0.43751679E-01	0.65928293E+02
0.50000000E+06	0.43045618E-01	0.65437778E+02
0.51000000E+06	0.42369216E-01	0.64953850E+02
0.52000000E+06	0.41720708E-01	0.64476408E+02
0.53000000E+06	0.41098465E-01	0.64005352E+02
0.54000000E+06	0.40500974E-01	0.63540587E+02

Figure 36 (e)

ω (rad/sec)	|α|	δ (deg)
0.55000000E+06	0.39926833E-01	0.63082025E+02
0.56000000E+06	0.39374743E-01	0.62629580E+02
0.57000000E+06	0.38843493E-01	0.62183167E+02
0.58000000E+06	0.38331957E-01	0.61742708E+02
0.59000000E+06	0.37839086E-01	0.61308125E+02
0.60000000E+06	0.37363898E-01	0.60879343E+02
0.61000000E+06	0.36905480E-01	0.60456289E+02
0.62000000E+06	0.36462974E-01	0.60038891E+02
0.63000000E+06	0.36035580E-01	0.59627081E+02
0.64000000E+06	0.35622545E-01	0.59220789E+02
0.65000000E+06	0.35223166E-01	0.58819948E+02
0.66000000E+06	0.34836781E-01	0.58424494E+02
0.67000000E+06	0.34462767E-01	0.58034360E+02
0.68000000E+06	0.34100540E-01	0.57649485E+02
0.69000000E+06	0.33749549E-01	0.57269804E+02
0.70000000E+06	0.33409275E-01	0.56895255E+02
0.71000000E+06	0.33079228E-01	0.56525777E+02
0.72000000E+06	0.32758947E-01	0.56161312E+02
0.73000000E+06	0.32447997E-01	0.55801795E+02
0.74000000E+06	0.32145963E-01	0.55447172E+02
0.75000000E+06	0.31852456E-01	0.55097380E+02
0.76000000E+06	0.31567108E-01	0.54752364E+02
0.77000000E+06	0.31289570E-01	0.54412064E+02
0.78000000E+06	0.31019509E-01	0.54076425E+02
0.79000000E+06	0.30756611E-01	0.53745389E+02
0.80000000E+06	0.30500579E-01	0.53418901E+02
0.81000000E+06	0.30251130E-01	0.53096906E+02
0.82000000E+06	0.30007996E-01	0.52779348E+02
0.83000000E+06	0.29770920E-01	0.52466173E+02
0.84000000E+06	0.29539660E-01	0.52157326E+02
0.85000000E+06	0.29313984E-01	0.51852756E+02
0.86000000E+06	0.29093674E-01	0.51552407E+02
0.87000000E+06	0.28878519E-01	0.51256228E+02
0.88000000E+06	0.28668319E-01	0.50964168E+02
0.89000000E+06	0.28462884E-01	0.50676173E+02
0.90000000E+06	0.28262034E-01	0.50392195E+02
0.91000000E+06	0.28065593E-01	0.50112181E+02
0.92000000E+06	0.27873397E-01	0.49836082E+02
0.93000000E+06	0.27685289E-01	0.49563849E+02
0.94000000E+06	0.27501118E-01	0.49295432E+02
0.95000000E+06	0.27320738E-01	0.49030783E+02
0.96000000E+06	0.27144012E-01	0.48769854E+02
0.97000000E+06	0.26970809E-01	0.48512599E+02
0.98000000E+06	0.26801002E-01	0.48258968E+02
0.99000000E+06	0.26634469E-01	0.48008917E+02

Figure 36 (f)

ω (rad/sec)	|α|	δ (deg)
0.10000000E+07	0.26471097E-01	0.47762400E+02
0.11000000E+07	0.24988891E-01	0.45481858E+02
0.12000000E+07	0.23725234E-01	0.43508146E+02
0.13000000E+07	0.22619727E-01	0.41804069E+02
0.14000000E+07	0.21630931E-01	0.40337392E+02
0.15000000E+07	0.20729874E-01	0.39080439E+02
0.16000000E+07	0.19895998E-01	0.38009593E+02
0.17000000E+07	0.19114552E-01	0.37104809E+02
0.18000000E+07	0.18374869E-01	0.36349137E+02
0.19000000E+07	0.17669190E-01	0.35728293E+02
0.20000000E+07	0.16991862E-01	0.35230300E+02
0.21000000E+07	0.16338761E-01	0.34845154E+02
0.22000000E+07	0.15706887E-01	0.34564567E+02
0.23000000E+07	0.15094072E-01	0.34381734E+02
0.24000000E+07	0.14498756E-01	0.34291156E+02
0.25000000E+07	0.13919835E-01	0.34288478E+02
0.26000000E+07	0.13356535E-01	0.34370371E+02
0.27000000E+07	0.12808332E-01	0.34534436E+02
0.28000000E+07	0.12274877E-01	0.34779118E+02
0.29000000E+07	0.11755952E-01	0.35103653E+02
0.30000000E+07	0.11251433E-01	0.35508019E+02
0.31000000E+07	0.10761261E-01	0.35992908E+02
0.32000000E+07	0.10285424E-01	0.36559699E+02
0.33000000E+07	0.98239416E-02	0.37210456E+02
0.34000000E+07	0.93768592E-02	0.37947917E+02
0.35000000E+07	0.89442381E-02	0.38775500E+02
0.36000000E+07	0.85261551E-02	0.39697302E+02
0.37000000E+07	0.81227000E-02	0.40718110E+02
0.38000000E+07	0.77339773E-02	0.41843402E+02
0.39000000E+07	0.73601074E-02	0.43079335E+02
0.40000000E+07	0.70012291E-02	0.44432733E+02
0.41000000E+07	0.66575031E-02	0.45911040E+02
0.42000000E+07	0.63291157E-02	0.47522238E+02
0.43000000E+07	0.60162822E-02	0.49274740E+02
0.44000000E+07	0.57192491E-02	0.51177193E+02
0.45000000E+07	0.54382965E-02	0.53238227E+02
0.46000000E+07	0.51737381E-02	0.55466092E+02
0.47000000E+07	0.49259179E-02	0.57868181E+02
0.48000000E+07	0.46952058E-02	0.60450438E+02
0.49000000E+07	0.44819864E-02	0.63216610E+02
0.50000000E+07	0.42866445E-02	0.66167432E+02
0.51000000E+07	0.41095433E-02	0.69299708E+02
0.52000000E+07	0.39509989E-02	0.72605452E+02
0.53000000E+07	0.38112471E-02	0.76071145E+02
0.54000000E+07	0.36904096E-02	0.79677333E+02

Figure 36 (g)

ω (rad/sec)	|α|	δ (deg)
0.55000000E+07	0.35884584E-02	0.83398609E+02
0.56000000E+07	0.35051857E-02	0.87204237E+02
0.57000000E+07	0.34401817E-02	-0.88940694E+02
0.58000000E+07	0.33928259E-02	-0.85073556E+02
0.59000000E+07	0.33622918E-02	-0.81232130E+02
0.60000000E+07	0.33475702E-02	-0.77452530E+02
0.61000000E+07	0.33475021E-02	-0.73767308E+02
0.62000000E+07	0.33608218E-02	-0.70204059E+02
0.63000000E+07	0.33862040E-02	-0.66784566E+02
0.64000000E+07	0.34223084E-02	-0.63524571E+02
0.65000000E+07	0.34678187E-02	-0.60434035E+02
0.66000000E+07	0.35214743E-02	-0.57517754E+02
0.67000000E+07	0.35820939E-02	-0.54776193E+02
0.68000000E+07	0.36485889E-02	-0.52206368E+02
0.69000000E+07	0.37199722E-02	-0.49802733E+02
0.70000000E+07	0.37953586E-02	-0.47557942E+02
0.71000000E+07	0.38739631E-02	-0.45463508E+02
0.72000000E+07	0.39550951E-02	-0.43510312E+02
0.73000000E+07	0.40381515E-02	-0.41689015E+02
0.74000000E+07	0.41226094E-02	-0.39990342E+02
0.75000000E+07	0.42080170E-02	-0.38405285E+02
0.76000000E+07	0.42939859E-02	-0.36925249E+02
0.77000000E+07	0.43801843E-02	-0.35542122E+02
0.78000000E+07	0.44663289E-02	-0.34248317E+02
0.79000000E+07	0.45521800E-02	-0.33036800E+02
0.80000000E+07	0.46375350E-02	-0.31901076E+02
0.81000000E+07	0.47222230E-02	-0.30835166E+02
0.82000000E+07	0.48061021E-02	-0.29833589E+02
0.83000000E+07	0.48890536E-02	-0.28891331E+02
0.84000000E+07	0.49709803E-02	-0.28003804E+02
0.85000000E+07	0.50518027E-02	-0.27166823E+02
0.86000000E+07	0.51314564E-02	-0.26376569E+02
0.87000000E+07	0.52098913E-02	-0.25629548E+02
0.88000000E+07	0.52870676E-02	-0.24922577E+02
0.89000000E+07	0.53629559E-02	-0.24252748E+02
0.90000000E+07	0.54375352E-02	-0.23617402E+02
0.91000000E+07	0.55107913E-02	-0.23014108E+02
0.92000000E+07	0.55827170E-02	-0.22440639E+02
0.93000000E+07	0.56533095E-02	-0.21894961E+02
0.94000000E+07	0.57225706E-02	-0.21375203E+02
0.95000000E+07	0.57905065E-02	-0.20879650E+02
0.96000000E+07	0.58571259E-02	-0.20406726E+02
0.97000000E+07	0.59224405E-02	-0.19954981E+02
0.98000000E+07	0.59864646E-02	-0.19523082E+02
0.99000000E+07	0.60492140E-02	-0.19109794E+02

Figure 36 (h)

ω (rad/sec)	|α|	δ (deg)
0.10000000E+08	0.61107060E-02	-0.18713985E+02
0.11000000E+08	0.66609671E-02	-0.15520395E+02
0.12000000E+08	0.71089862E-02	-0.13286765E+02
0.13000000E+08	0.74753835E-02	-0.11639201E+02
0.14000000E+08	0.77772669E-02	-0.10373595E+02
0.15000000E+08	0.80280915E-02	-0.93700767E+01
0.16000000E+08	0.82382670E-02	-0.85539738E+01
0.17000000E+08	0.84158299E-02	-0.78764800E+01
0.18000000E+08	0.85670075E-02	-0.73044035E+01
0.19000000E+08	0.86966587E-02	-0.68144020E+01
0.20000000E+08	0.88086019E-02	-0.63895912E+01
0.21000000E+08	0.89058654E-02	-0.60174540E+01
0.22000000E+08	0.89908683E-02	-0.56885157E+01
0.23000000E+08	0.90655597E-02	-0.53954685E+01
0.24000000E+08	0.91315217E-02	-0.51325855E+01
0.25000000E+08	0.91900481E-02	-0.48953115E+01
0.26000000E+08	0.92422049E-02	-0.46799772E+01
0.27000000E+08	0.92888749E-02	-0.44835924E+01
0.28000000E+08	0.93307954E-02	-0.43036945E+01
0.29000000E+08	0.93685841E-02	-0.41382375E+01
0.30000000E+08	0.94027631E-02	-0.39855039E+01
0.31000000E+08	0.94337744E-02	-0.38440445E+01
0.32000000E+08	0.94619957E-02	-0.37126240E+01
0.33000000E+08	0.94877494E-02	-0.35901850E+01
0.34000000E+08	0.95113136E-02	-0.34758155E+01
0.35000000E+08	0.95329285E-02	-0.33687255E+01
0.36000000E+08	0.95528018E-02	-0.32682256E+01
0.37000000E+08	0.95711156E-02	-0.31737125E+01
0.38000000E+08	0.95880275E-02	-0.30846559E+01
0.39000000E+08	0.96036769E-02	-0.30005865E+01
0.40000000E+08	0.96181852E-02	-0.29210893E+01
0.41000000E+08	0.96316610E-02	-0.28457931E+01
0.42000000E+08	0.96441995E-02	-0.27743680E+01
0.43000000E+08	0.96558852E-02	-0.27065171E+01
0.44000000E+08	0.96667936E-02	-0.26419744E+01
0.45000000E+08	0.96769917E-02	-0.25804993E+01
0.46000000E+08	0.96865400E-02	-0.25218749E+01
0.47000000E+08	0.96954921E-02	-0.24659041E+01
0.48000000E+08	0.97038966E-02	-0.24124079E+01
0.49000000E+08	0.97117972E-02	-0.23612235E+01
0.50000000E+08	0.97192333E-02	-0.23122016E+01
0.51000000E+08	0.97262405E-02	-0.22652066E+01
0.52000000E+08	0.97328511E-02	-0.22201131E+01
0.53000000E+08	0.97390943E-02	-0.21768067E+01
0.54000000E+08	0.97449969E-02	-0.21351821E+01

Figure 36 (i)

ω (rad/sec)	|α|	δ (deg)
0.55000000E+08	0.97505831E-02	-0.20951415E+01
0.56000000E+08	0.97558751E-02	-0.20565953E+01
0.57000000E+08	0.97608932E-02	-0.20194604E+01
0.58000000E+08	0.97656560E-02	-0.19836599E+01
0.59000000E+08	0.97701801E-02	-0.19491220E+01
0.60000000E+08	0.97744816E-02	-0.19157806E+01
0.61000000E+08	0.97785747E-02	-0.18835740E+01
0.62000000E+08	0.97824730E-02	-0.18524444E+01
0.63000000E+08	0.97861879E-02	-0.18223382E+01
0.64000000E+08	0.97897312E-02	-0.17932053E+01
0.65000000E+08	0.97931132E-02	-0.17649987E+01
0.66000000E+08	0.97963436E-02	-0.17376747E+01
0.67000000E+08	0.97994312E-02	-0.17111920E+01
0.68000000E+08	0.98023842E-02	-0.16855120E+01
0.69000000E+08	0.98052106E-02	-0.16605985E+01
0.70000000E+08	0.98079172E-02	-0.16364174E+01
0.71000000E+08	0.98105108E-02	-0.16129364E+01
0.72000000E+08	0.98129975E-02	-0.15901256E+01
0.73000000E+08	0.98153835E-02	-0.15679562E+01
0.74000000E+08	0.98176737E-02	-0.15464015E+01
0.75000000E+08	0.98198735E-02	-0.15254360E+01
0.76000000E+08	0.98219869E-02	-0.15050359E+01
0.77000000E+08	0.98240195E-02	-0.14851782E+01
0.78000000E+08	0.98259745E-02	-0.14658414E+01
0.79000000E+08	0.98278557E-02	-0.14470054E+01
0.80000000E+08	0.98296673E-02	-0.14286508E+01
0.81000000E+08	0.98314126E-02	-0.14107590E+01
0.82000000E+08	0.98330944E-02	-0.13933128E+01
0.83000000E+08	0.98347161E-02	-0.13762956E+01
0.84000000E+08	0.98362806E-02	-0.13596917E+01
0.85000000E+08	0.98377904E-02	-0.13434861E+01
0.86000000E+08	0.98392479E-02	-0.13276646E+01
0.87000000E+08	0.98406555E-02	-0.13122137E+01
0.88000000E+08	0.98420158E-02	-0.12971203E+01
0.89000000E+08	0.98433304E-02	-0.12823721E+01
0.90000000E+08	0.98446016E-02	-0.12679573E+01
0.91000000E+08	0.98458313E-02	-0.12538650E+01
0.92000000E+08	0.98470214E-02	-0.12400839E+01
0.93000000E+08	0.98481731E-02	-0.12266041E+01
0.94000000E+08	0.98492887E-02	-0.12134157E+01
0.95000000E+08	0.98503691E-02	-0.12005094E+01
0.96000000E+08	0.98514162E-02	-0.11878759E+01
0.97000000E+08	0.98524310E-02	-0.11755069E+01
0.98000000E+08	0.98534150E-02	-0.11633942E+01
0.99000000E+08	0.98543696E-02	-0.11515295E+01

Figure 36 (j)

ω (rad/sec)	|α|	δ (deg)
0.10000000E+09	0.98552956E-02	-0.11399055E+01
0.11000000E+09	0.98632139E-02	-0.10354339E+01
0.12000000E+09	0.98692396E-02	-0.94855993E+00
0.13000000E+09	0.98739312E-02	-0.87517179E+00
0.14000000E+09	0.98776554E-02	-0.81234872E+00
0.15000000E+09	0.98806603E-02	-0.75795832E+00
0.16000000E+09	0.98831203E-02	-0.71040651E+00
0.17000000E+09	0.98851596E-02	-0.66847799E+00
0.18000000E+09	0.98868685E-02	-0.63122966E+00
0.19000000E+09	0.98883153E-02	-0.59791829E+00
0.20000000E+09	0.98895505E-02	-0.56795045E+00
0.21000000E+09	0.98906135E-02	-0.54084621E+00
0.22000000E+09	0.98915349E-02	-0.51621352E+00
0.23000000E+09	0.98923392E-02	-0.49372876E+00
0.24000000E+09	0.98930447E-02	-0.47312250E+00
0.25000000E+09	0.98936675E-02	-0.45416861E+00
0.26000000E+09	0.98942198E-02	-0.43667587E+00
0.27000000E+09	0.98947119E-02	-0.42048146E+00
0.28000000E+09	0.98951524E-02	-0.40544595E+00
0.29000000E+09	0.98955479E-02	-0.39144922E+00
0.30000000E+09	0.98959045E-02	-0.37838707E+00
0.31000000E+09	0.98962272E-02	-0.36616892E+00
0.32000000E+09	0.98965202E-02	-0.35471549E+00
0.33000000E+09	0.98967871E-02	-0.34395712E+00
0.34000000E+09	0.98970304E-02	-0.33383241E+00
0.35000000E+09	0.98972535E-02	-0.32428695E+00
0.36000000E+09	0.98974581E-02	-0.31527237E+00
0.37000000E+09	0.98976465E-02	-0.30674556E+00
0.38000000E+09	0.98978203E-02	-0.29866799E+00
0.39000000E+09	0.98979807E-02	-0.29100506E+00
0.40000000E+09	0.98981293E-02	-0.28372562E+00
0.41000000E+09	0.98982673E-02	-0.27680156E+00
0.42000000E+09	0.98983950E-02	-0.27020751E+00
0.43000000E+09	0.98985143E-02	-0.26392040E+00
0.44000000E+09	0.98986258E-02	-0.25791925E+00
0.45000000E+09	0.98987295E-02	-0.25218504E+00
0.46000000E+09	0.98988268E-02	-0.24670029E+00
0.47000000E+09	0.98989179E-02	-0.24144910E+00
0.48000000E+09	0.98990032E-02	-0.23641684E+00
0.49000000E+09	0.98990835E-02	-0.23159010E+00
0.50000000E+09	0.98991591E-02	-0.22695655E+00
0.51000000E+09	0.98992301E-02	-0.22250480E+00
0.52000000E+09	0.98992973E-02	-0.21822437E+00
0.53000000E+09	0.98993605E-02	-0.21410553E+00
0.54000001E+09	0.98994201E-02	-0.21013932E+00

Figure 36 (k)

ω (rad/sec)	|α|	δ (deg)
0.55000001E+09	0.98994769E-02	-0.20631741E+00
0.56000001E+09	0.98995307E-02	-0.20263205E+00
0.57000001E+09	0.98995813E-02	-0.19907607E+00
0.58000001E+09	0.98996293E-02	-0.19564277E+00
0.59000001E+09	0.98996749E-02	-0.19232588E+00
0.60000001E+09	0.98997186E-02	-0.18911962E+00
0.61000001E+09	0.98997600E-02	-0.18601850E+00
0.62000001E+09	0.98997992E-02	-0.18301747E+00
0.63000001E+09	0.98998367E-02	-0.18011174E+00
0.64000001E+09	0.98998726E-02	-0.17729684E+00
0.65000001E+09	0.98999066E-02	-0.17456859E+00
0.66000001E+09	0.98999392E-02	-0.17192303E+00
0.67000001E+09	0.98999705E-02	-0.16935648E+00
0.68000001E+09	0.99000002E-02	-0.16686543E+00
0.69000001E+09	0.99000285E-02	-0.16444662E+00
0.70000001E+09	0.99000558E-02	-0.16209693E+00
0.71000001E+09	0.99000821E-02	-0.15981344E+00
0.72000001E+09	0.99001070E-02	-0.15759341E+00
0.73000001E+09	0.99001309E-02	-0.15543421E+00
0.74000001E+09	0.99001541E-02	-0.15333338E+00
0.75000001E+09	0.99001761E-02	-0.15128861E+00
0.76000001E+09	0.99001977E-02	-0.14929763E+00
0.77000001E+09	0.99002178E-02	-0.14735840E+00
0.78000001E+09	0.99002377E-02	-0.14546889E+00
0.79000001E+09	0.99002565E-02	-0.14362724E+00
0.80000001E+09	0.99002748E-02	-0.14183163E+00
0.81000001E+09	0.99002923E-02	-0.14008038E+00
0.82000001E+09	0.99003094E-02	-0.13837183E+00
0.83000001E+09	0.99003256E-02	-0.13670447E+00
0.84000001E+09	0.99003414E-02	-0.13507682E+00
0.85000001E+09	0.99003562E-02	-0.13348748E+00
0.86000001E+09	0.99003711E-02	-0.13193510E+00
0.87000001E+09	0.99003852E-02	-0.13041842E+00
0.88000001E+09	0.99003990E-02	-0.12893621E+00
0.89000001E+09	0.99004122E-02	-0.12748731E+00
0.90000001E+09	0.99004247E-02	-0.12607062E+00
0.91000001E+09	0.99004371E-02	-0.12468508E+00
0.92000001E+09	0.99004494E-02	-0.12332964E+00
0.93000001E+09	0.99004608E-02	-0.12200338E+00
0.94000001E+09	0.99004721E-02	-0.12070533E+00
0.95000001E+09	0.99004827E-02	-0.11943462E+00
0.96000001E+09	0.99004932E-02	-0.11819038E+00
0.97000001E+09	0.99005034E-02	-0.11697180E+00
0.98000001E+09	0.99005137E-02	-0.11577809E+00
0.99000001E+09	0.99005229E-02	-0.11460851E+00

Figure 36 (1)

These values of the components move the cusp in the response curve, Figure 35, to a frequency of approximately 1 MHz. The high frequency value of $|\alpha|$, as can be seen from the graph and the tabulated data, is equal to 1/100; therefore, the circuit satisfies the constraints and is stable.

The phase shift due to the compensation network is small at high frequencies; therefore, the majority of the overall phase shift at high frequencies is due only to the amplifier. The phase shift of the compensation network is large when the phase shift due to the amplifier is small and vice versa.

Results:

A characteristic of the SN72702 operational amplifier is the input voltage range, -6 volts to +1.5 volts. The voltage follower is therefore limited principally to negative signals.

The bandwidth of the voltage follower is defined here on the basis of a decrease by a factor of e in output signal With a -2 volt input signal the output voltage was reduced by a factor of e at 5 MHz. The response of the voltage follower is within 90% of the input signal at 2.4 MHz.

An estimate of the input impedance of the voltage follower was made by discharging a capacitor through the voltage follower and observing the decay time. This procedure was followed because the voltage follower was to be used as the output buffer for a pulse stretcher circuit. The time for the capacitor to decay to 5% of its original value is three time constants. The measured value of this time was 6 ms with a capacitance of 5 nf The low-frequency input impedance Z_i of the voltage follower is therefore approximately 400 KΩ.

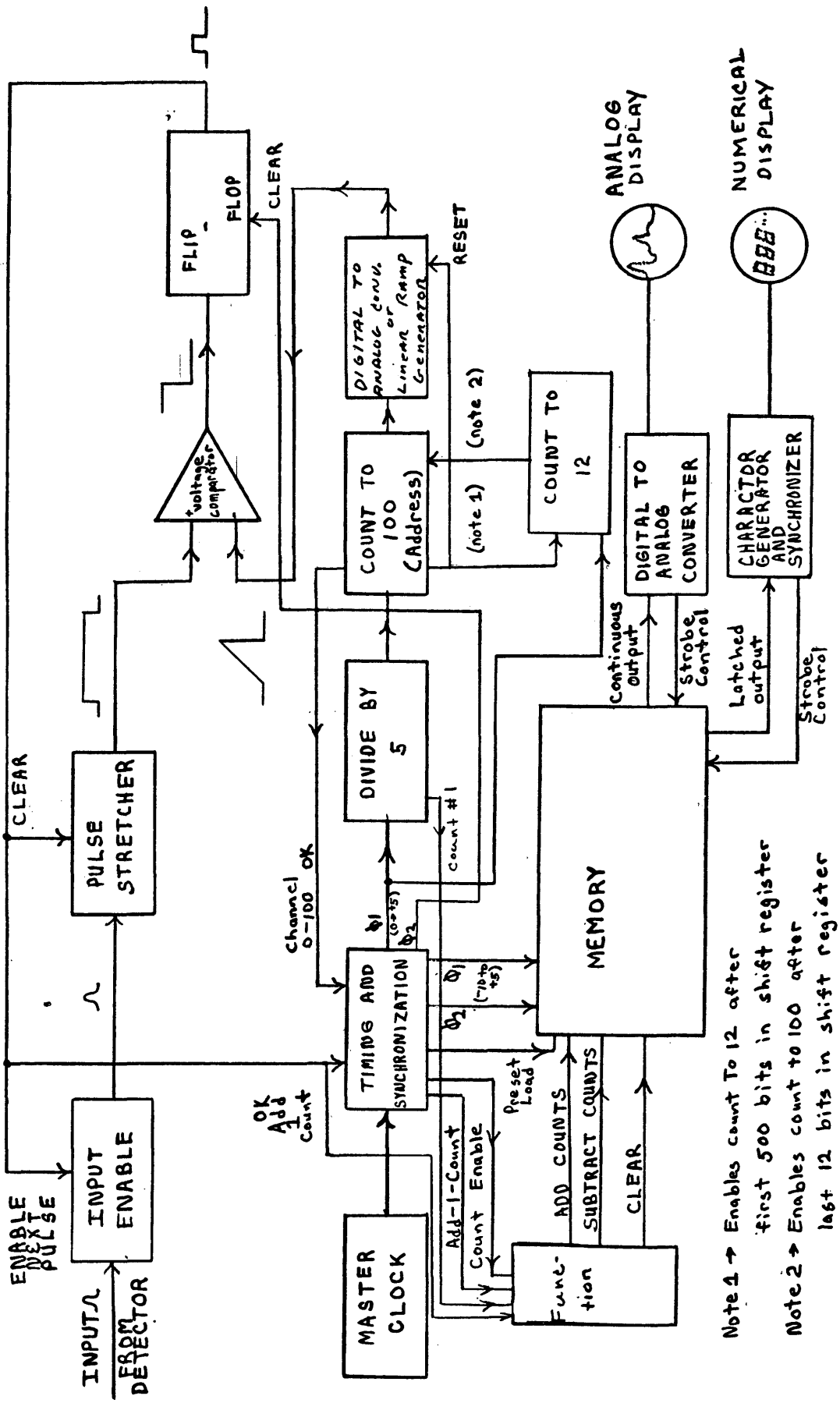
CHAPTER 7

DESCRIPTION OF A PULSE HEIGHT ANALYZER

The previously described circuits may be used in a pulse height analyzer. Figure 37 is a block flow diagram for such a device with 5 decimal digits of information in each of 100 addresses.

Pulses from a detector are applied to the input enable. This stage allows only one pulse to reach the input of the pulse stretcher. The pulse stretcher stretches in time the pulse transmitted through the input enable and applies it to one of the inputs of a voltage comparator.

The master clock's output is applied to the input of the timing and synchronization circuit. The $\Phi 1$ clock output is divided by five because there are five decimal digits corresponding to each address in the memory (four shift registers). The output of the divide by 5 is applied to the input of a count to 100 circuit. The count to 100 monitors the analyzer's address. The output of the count to 100 is applied to the input of a digital-to-analog converter or synchronized linear ramp generator, and the analog output voltage of the converter or generator is a staircase or linear ramp which is synchronized with the memory. This staircase or ramp is applied to the other input of the voltage comparator.



Block Flow Diagram - Pulse Height Analyzer

Figure 37

When the voltage of the stretched pulse is equal to the voltage of the staircase or ramp, the voltage comparator changes states and triggers the flip-flop. The flip-flop is reset on the next Φ2 clock pulse; therefore, the flip-flop generates a pulse when a count should be added to memory. This pulse is used as the OK-add-1-count pulse for the timing and synchronization circuit, used to enable the input so the next pulse may be accepted and used to clear the pulse stretcher.

The add one count and count enable outputs of the timing and synchronization circuit are applied to the input of the function module, which determines whether the counts from the comparison section of the circuit are to be added into or subtracted from the memory. The first location in each address is determined by the divide by 5 circuit, and this circuit ensures that the function module adds a new count only into the units level in an address.

The continuous output from memory is applied to a digital-to-analog converter, which generates an analog display for a cathode ray tube device, i.e., the oscilloscope that the pulse height analyzer could be plugged into.

The latched output from the memory is applied to the input of a character generator and synchronizer. This circuit generates the seven-segment characters that are displayed on the cathode ray tube screen for the numerical display.

This model pulse height analyzer could be economically used as a plug-in unit for a Tektronix 561 oscilloscope. The pulse height analyzer would use the oscilloscope deflection circuit and cathode ray tube

for display purposes and some of the internal power supplies of the oscilloscope.

CHAPTER 8

DESCRIPTION OF A MÖSSBAUER DATA ANALYZER

The previously described circuits may be used in a Mössbauer data analyzer as shown in Figure 38.

The master clock of the Mössbauer analyzer is applied to the input of a divide or not-divide circuit. The memory address selector determines whether the master clock frequency is to be divided or not.

In the region where this frequency is divided, the divided frequency is applied to the input of the timing and synchronization circuit; the $\Phi 1$ output of the timing and synchronization circuit is applied to the input of an up/down counter. The output of the counter is applied to the input of a digital-to-analog converter, and its output is applied to the input of a smoother circuit. Whether the counter counts up or counts down is determined by the output of a flip-flop. The input of the flip-flop is the end of memory reset generated by the memory address selector. Therefore the counter counts up on one cycle of memory and counts down on the next cycle of memory. This counting scheme through the digital-to-analog converter generates a triangular wave output voltage. This triangular wave output voltage is the driving voltage for the motion device for the Mössbauer analyzer.

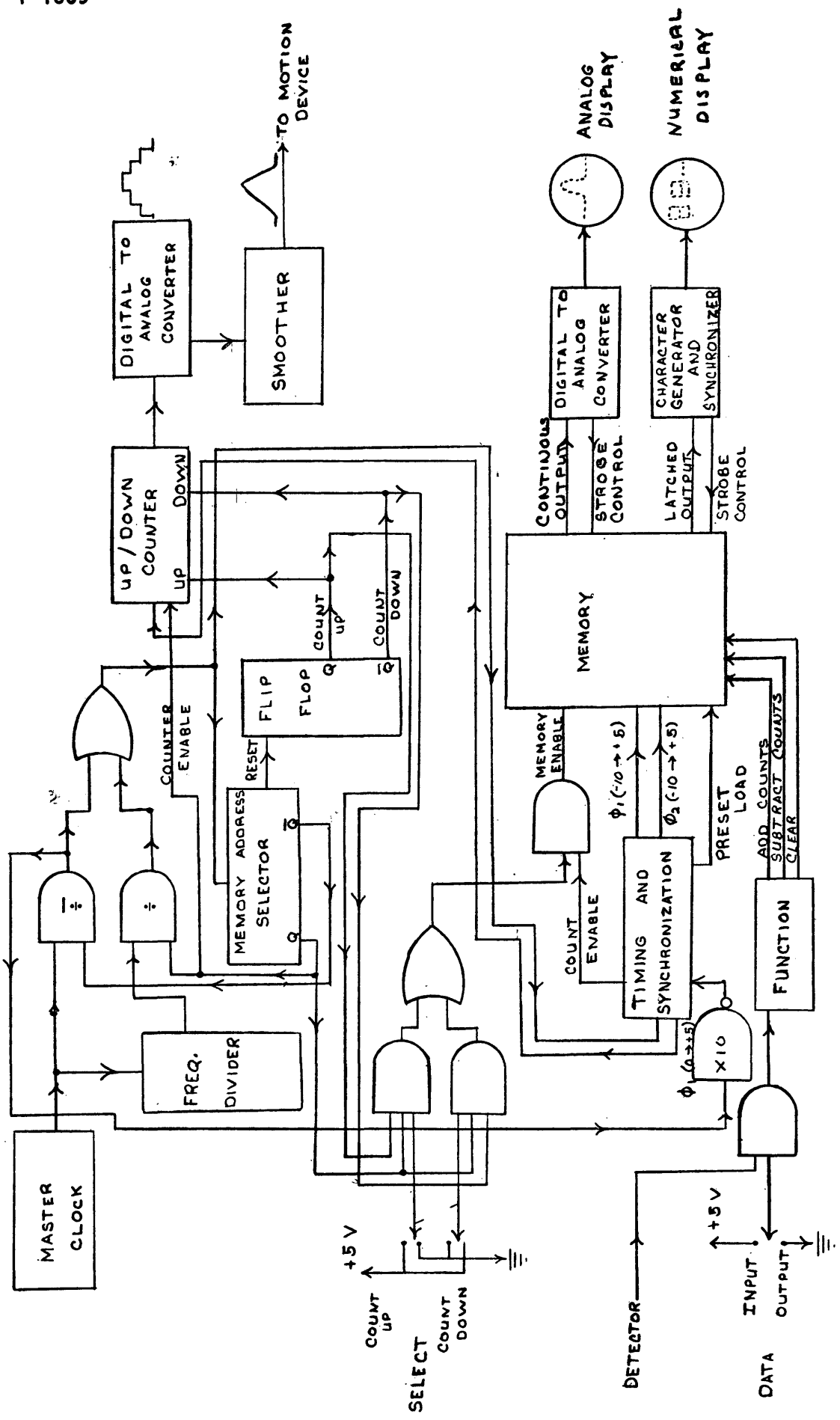


Figure 38

Block Flow Diagram - Mössbauer Data Analyzer

The same pulses that generate the triangular wave output voltage shift the memory of the analyzer; the memory, therefore, is synchronized with the motion device. When the memory is within the selected bounds determined by the memory address selector, the memory is shifting slowly (clock frequency divided), the triangular output is changing, the input to the memory is enabled, and the pulses corresponding to the velocity of the motion device are added into or subtracted from the memory.

When the memory is not within the selected bounds the master clock frequency is not divided. The up/down counter used to generate the triangular wave output voltage is disabled; consequently, the triangular wave output is not changing during the high-frequency shifting of memory. The memory input is also disabled during this time; nothing can be altered in the memory locations, therefore, that has not been selected by the memory address selector.

The external count-up/count-down switch allows the flexibility of counting either on the positive or on the negative slope of the triangular wave.

The detector pulses are applied to the input of the function module, which determines whether the pulses are to be added into or subtracted from the memory. The function module also clears the memory.

The continuous output of the memory is applied to a digital-to-analog converter, which generates an analog display of the data in memory on a cathode ray tube.

The latched output of the memory is applied to the input of a character generator, which will generate the numerical display for the cathode ray tube.

The circuit configuration for the Mössbauer analyzer generates a triangular output voltage which is synchronized with the memory. The memory input is enabled, causing the counts received at the detector to change memory contents only while the triangular wave output is changing.

BIBLIOGRAPHY

1. Intel Corporation, 512 bit dynamic recirculating shift register: Mountain View, California, Intel Corporation, p. 5 (1970).

2. Ibid., p. 6.

3. Brockman, D. M., Synchronous ramp generator maintains output linearity: Electronics, v. 46, no. 2, p. 170 (1972).

4. Hunter, Lloyd P., Handbook of semiconductor electronics: New York, New York, McGraw-Hill Book Co., p. 3 - 13 (1956)

5. Texas Instruments, Engineering Staff, The integrated circuits datalog for design engineers: Dallas, Texas, Texas Instruments, p. 6-49 - 6-53.

6. Giles, James N., Fairchild semiconductor linear integrated circuit applications handbook: Mountain View, California, Fairchild Semiconductor, p. 45 (1966).

7. Ibid., p. 35.

APPENDIX

Operation of J-K Master-Slave Flip-Flop

A J-K flip-flop is a bistable device whose output is determined by the values of the J and K inputs and the clock pulse.

The truth table for an SN7473 J-K master-slave flip-flop is given in Table 7, page 79. The inputs to the master are governed by the clock pulse. The clock pulse also determines the state of the coupling between the master and the slave. The operating sequence is

1. Isolate the slave from the master;
2. Enter information from the J and K inputs into the master;
3. Disable J and K inputs;
4. Transfer the information from the master into the slave.

The above numbers correspond to those on the clock wave form in Figure 24, page 80.

If J = K = "1" then from Table 7 the Q output of the flip-flop, on the t_{n+1} pulse, will assume the value that $\overline{Q}$ had at time t_n. A flip-flop connected in this manner changes state on each clock pulse. If, for example, J = "1" and K = "0" at point 3 in Figure 24, then at point 4 the value of Q is "1" Similarly if J = "0" and K = "1" at point 3,

then at point 4, Q is "0" The value of Q will not change with the clock pulse if J = K = "0"