PASSIVATED CONTACTS FOR HIGH EFFICIENCY MONOCRYSTALLINE SILICON SOLAR CELLS

by

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ABSTRACT

Global energy demands have been increasing and the ability of fossil fuels to meet these demands is limited. Due to the associated climate change concerns, most of the current new energy installations have been based on renewable energy resources such as wind and solar. However, to further develop solar energy as a renewable energy resource, improvements in silicon-based solar cells, which represent more than 90% of the current photovoltaics market, is critical. In this thesis work we explore strategies for more efficient and cheaper solar cells. Efficiency improvements are enabled via passivated contacts, which serve both as a contact layer and a passivation layer for the crystalline silicon (*c*-Si) surface, and are a potential candidate for next-generation industrial *c*-Si solar cells. In this thesis work, we identify a few salient features of passivated contacts comprising of a polycrystalline Si (*poly*-Si) deposited on top of ultrathin, 1.5–2.2 nm thick SiO_x layers forming a metal/*poly*-Si/SiO_x/*c*-Si contact stack. *Poly*-Si/SiO_x contact passivation and conduction depends on both the SiO_x thickness and contact annealing temperature. Depending on the processing conditions, two different scenarios for conduction through the SiO_x layer are observed: uniform tunneling conduction or locally enhanced conduction. The locally enhanced conduction occurs through 10s of nanometer size regions with either no SiO_x layer, or a thinned-down tunneling SiO_x layer. The performance of the *poly*-Si/SiO_x contacts on a pyramidal textured Si surface, which is critical for light-trapping, is also studied. The poorer passivation on a textured surface is related to the surface morphology: both the pyramidal morphology and nanoscale roughness over the pyramidal shape, causing SiO_x related nonuniformities. Both the pyramidal morphology and nanoscale roughness can be modified using wet-chemical etching via HF:HNO_3 solution. Such a morphological change improves surface passivation, but deteriorates the light trapping properties

of the Si surface. We also explored strategies to replace current solar cell metallization processes based on the expensive Ag metal with a cheaper Cu metal, which necessitates a conductive Cu diffusion barrier interlayer between Cu and Si. The superior Cu diffusion barrier properties and thermal stability of a Cu/NiSi/Si stack over a Cu/Ni/Si stack is demonstrated.

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CHAPTER 1

INTRODUCTION

1.1. Why photovoltaics?

Global energy demands have been increasing and the ability of fossil fuels to meet these demands are limited. As shown in Fig. 1.1 most of the current energy demand is met using fossil fuels, and at current energy consumption rates, coal, oil and gas reserves may not last for more than a century [1]. Also, there has been a rising concern of climate change due to increased levels of CO_2 in the atmosphere due to consumption of fossil fuels, and some of these effects are even observed today [2, 3]. Nuclear energy is a good alternative, but safety and extensive capital investment has always been a major concern. Especially, after the Fukushima Daiichi nuclear disaster in 2011, several countries are changing their energy policies to reduce or even phase out all nuclear power stations. Hydroelectricity and bio-fuels have their own limitations, and in the long run renewable clean energy sources such as solar, wind, and geothermal seem to be the most promising options.

Sun is the primary source of energy for Earth. The total solar energy absorbed by the Earth is approximately 3,850,000 exajoules (EJ) (1 EJ = 10^{18} J) per hour, which is more energy than the world consumed in one year in 2002. The 2000 World Energy Assessment report found that the annual usable potential for solar energy was 1,574─49,837 EJ, which is far greater than the current annual global energy demand of 560 EJ. While these numbers have been calculated under certain assumptions, they nevertheless show the vast potential present in harvesting solar energy to generate electricity using the photovoltaic (PV) effect discovered by Edmond Becquerel in 1839 [4].

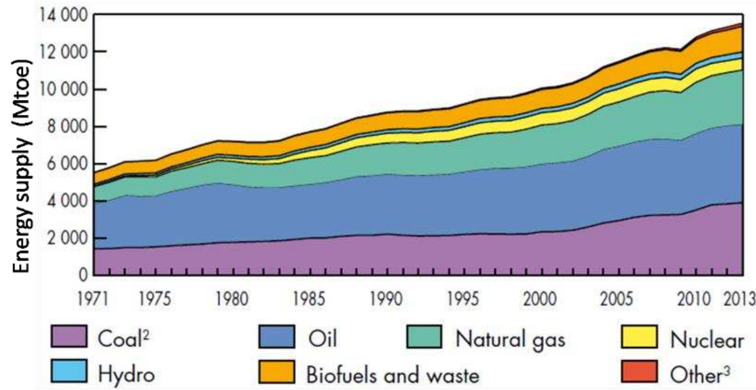

Figure 1.1 World total primary energy supply in mega ton of oil equivalent (Mtoe). Others – thermal, solar, wind, etc. Figure reproduced from Ref. [5].

1.2. Types of photovoltaic technologies

In 2001, Green categorized PV technologies into three generations based on their efficiency and cost/unit area [6]. 1st-generation PV included wafer-based solar cells such as multicrystalline Si (*mc*-Si) and monocrystalline Si (*c*-Si) cells, which had moderate efficiencies, 12─21%, but high-costs. 2nd-generation PV technologies included thin-film solar cells such as CdTe, $CuIn_xGa_{(1-x)}Se_2$ (CISG), and amorphous Si, which can be grown on either flexible substrates or on substrates such as glass, making them quite cheap. Their low efficiency, 6-13%, limited their application at the time. 3rd-generation cells were based on advanced concepts which have the potential to overcome the Shockley-Queisser limit for single-junction solar cells [7-9]. These included advanced concepts such as photon frequency conversion, hot-carriers, multiple carrier excitation [9]. Tandems were also considered a part of 3rd-generation PV. Tandems use layers of multiple semiconducting materials, with different band gaps to absorb solar light in the most efficient way [10, 11]. While 3rd-generation cells resulted in high-efficiency, they were primarily used for niche applications due to their significantly higher costs. It was projected at the time that efficiency improvement in 2nd-generation PV would overshadow the high-costs of 1st-generaltion Si PV,

replacing Si as the dominant PV technology. However, Fig. 1.2 clearly shows that this did not happen, and Si continues to dominate the PV market. Newer technologies such as band-gap tunable perovskites have emerged, which have the potential to be cheap and have high-efficiency [12-14]. Thus, the rapidly evolving current and upcoming PV technologies, cannot be properly distinguished into the three generations as categorized by Green. Instead, it is more accurate to categorize them as Si-based, thin-film based, and tandems, which can be a combination of the previous two. III-V-on-Si and perovskite-on-Si are the two tandem technologies, which might find application in large scale PV [15]. For III-V, the main challenges are high material costs, and low-growth rates which make them unsuitable for high-throughput manufacturing. Perovskites have gained significant research interest in the last few years, but long-term reliability and large area uniform depositions are issues that need to be addressed [16-18]. Apart, from these material issues, another significant challenge with tandems is their integration in current inverters and other system-level equipments [19, 20]. Tandems can be connected in either 2-, 3-, or 4-terminal configuration with 2-terminal being the cheapest, and 4-terminal the most efficient. The projections in Fig. 1.3 show that tandems based on a Si bottom cell might come into industrial scale manufacturing by 2023.

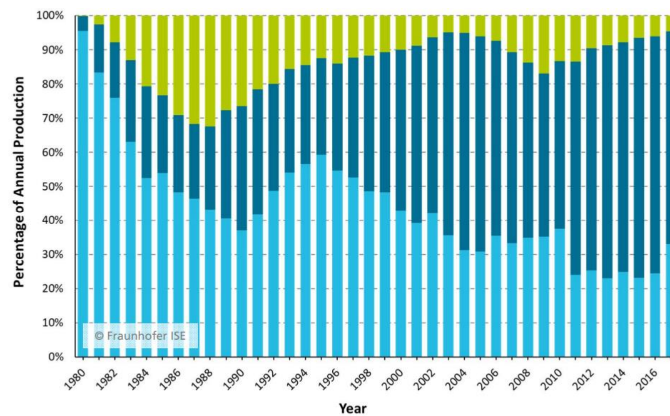

Figure 1.2 Percentage of global annual production of power from different PV technologies: *c*-Si (light blue), *mc*-Si (dark blue) and thin-films (green). Figure reproduced from Ref. [21].

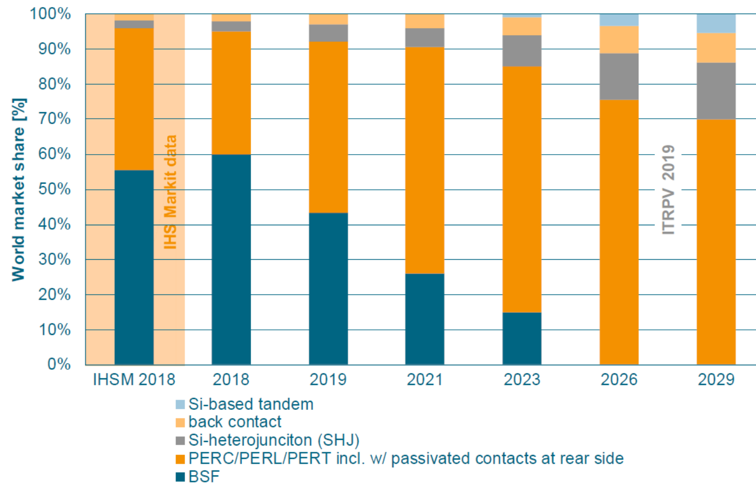

Figure 1.3 Worldwide market projections for different PV cell technologies. Figure reproduced from Ref. [15].

1.3. Basics of silicon solar cells

1.3.1. Working of a solar cell and important cell parameters

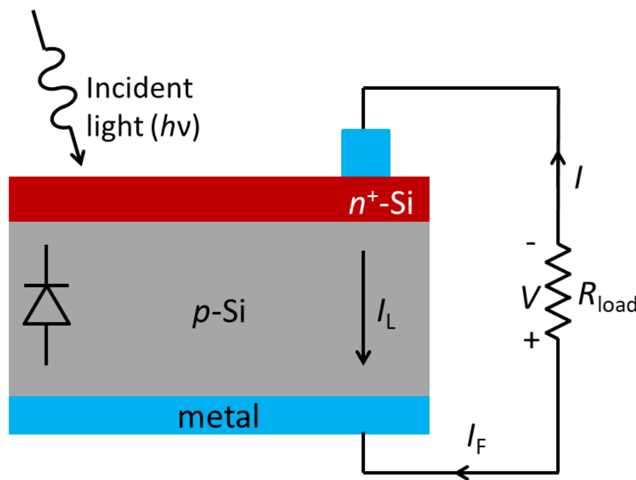

Figure 1.4 Schematic of a *p-n* junction solar cell under illumination.

In the simplest of terms, a solar cell can be considered as a single *p-n* junction device (see Fig. 1.4) [22]. An incident photon of energy equal to or greater than the bandgap (E_g) of the semiconductor is absorbed by the semiconductor material in a solar cell, thus exciting an electron

to the conduction band or a higher energy level, leaving behind a positively charged vacancy in the valence band, referred to as a hole. Thus, an electron-hole pair is created due to the absorption of light. Any energy greater than E_g is lost by the excited electron due to thermal losses. Conversely, a photon with energy less than E_g is not absorbed by the semiconductor. Both these factors limit the Shockley-Queisser efficiency of a single-junction solar cell [7], to ~33.77% for an ideal bandgap of 1.34 eV [23], and ~29.43% for 1.1 eV *c*-Si bandgap [8]. Electrons and holes created in the semiconductor due to such photon absorption are referred to as excess carriers. The excited carriers diffuse freely in the bulk of the material, and as they randomly diffuse near the *p*-*n* junction, the built-in electric field causes the electrons to drift towards the *n*-side and holes towards the *p*-side. This separation and accumulation of electron and holes creates a potential difference across the device, which can be used across an external load of resistance *R* as shown in Fig. 1.4.

The fundamental *I*-*V* relation for a solar cell is derived from the ideal diode equation, and is given as [24],

$$I = I_L - I_o \left[exp\left(\frac{eV}{kT}\right) - 1\right] \quad (1.1)$$

where, I_L is the light-generated current due to absorption of the incident photons, I_o is the saturation/recombination current, which depends on the extent of recombination in the cell, *V* is the voltage drop across the load, *T* is the semiconductor temperature, *e* is the unit charge of an electron, and *k* is the Boltzmann's constant. Figure 1.5 shows the *I*-*V* (black) and power-voltage (red) curve of a solar cell under illumination. In this *I*-*V* curve, there are two extremes: one for the current and the other for the voltage. When the cell is shorted, i.e., the *p* and *n* terminals are directly connected to each other, there is no voltage drop across the load: the current that flows under these conditions is at its maximum, and known as the short-circuit current, I_{sc}. Usually, the internal

resistance in a solar cell is small and, hence, I_{sc} can be approximated as the light-generated current. It must be noted that the light generated current depends on the intensity of the incident light. The other extreme in the *I-V* curve is when the cell is connected to an infinite resistance load, i.e., no current can flow, and the corresponding voltage across the device is the open-circuit voltage, V_{oc}. Simplistically, the higher the concentration of the light-generated carriers at the two terminals of the cell at steady state under illumination, the higher the V_{oc}. Thus, V_{oc} is a measure of the extent of carrier recombination in the cell and a lower recombination would lead to a higher V_{oc}. Recombination is further discussed in Section 1.3.2. From Eq. 1.1 the V_{oc} of a cell (i.e. I=0) can be written as

$$V_{oc} = \frac{kT}{e} ln\left(\frac{I_L}{I_o} + 1\right). \quad (1.2)$$

The curve in red in Fig. 1.5 is the resultant power from the cell. A cell is usually operated at the maximum power point, P_{max}, and V_{mp} and I_{mp} are the voltage and current at the maximum power point. The maximum power point corresponds to the largest area rectangle, light green (see Fig 1.5), that can be drawn within the bounds of the *I-V* curve. The fill-factor (*FF*), which is essentially the ratio of the areas of the light green and light blue rectangles in Fig. 1.5, relates solar cell efficiency (η) to I_{sc} and V_{oc}. The *FF* can thus be defined as

$$FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}}, \quad (1.3)$$

and the cell efficiency, in terms of *FF* as

$$\eta = \frac{I_{mp}V_{mp}}{P_{in}} = \frac{FF \times I_{sc}V_{oc}}{P_{in}}, \quad (1.4)$$

where P_{in} is the incident solar power. As the above values depend on the intensity of the light used, most values are reported under standard 1-Sun conditions, air mass (AM) index 1.5.

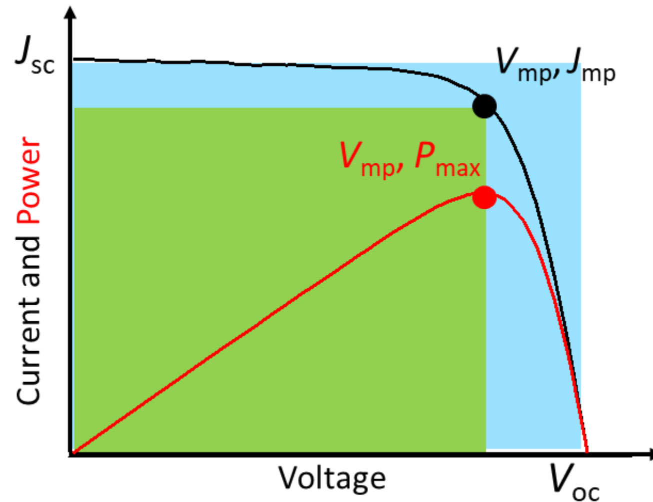

Figure 1.5 Typical current-voltage (*I*-*V*, black) and power-voltage (*P*-*V*, red) curve for a solar cell.

Thus, V_{oc}, I_{sc} and *FF* are the three key parameters that need to be maximized for highest solar cell efficiency. For highest V_{oc}, the number of defects, both in bulk and near the surface of the semiconducting absorber material need to be low. For highest I_{sc}, light-trapping in the absorber material needs to be improved. For highest *FF*, a high V_{oc} and low resistance losses are critical. These losses are related to both series resistance, and shunt resistance in the cell. Below we discuss how to increase V_{oc} and I_{sc} of a cell.

1.3.2. Carrier recombination in solar cell

Recombination of excited carriers can occur at defects present either in the bulk or near the surface resulting in efficiency loss. Below we discuss the various carrier recombination mechanisms in a semiconductor material.

Bulk recombination: As the name suggests, bulk recombination relates to the recombination of the photo-generated electrons and holes within the bulk of the semiconductor, significantly away from any surface or interface. While some recombination pathways are inherent to the semiconductor material (radiative and Auger), others are due to presence of defects and/or impurities in the material (Shockley-Read-Hall).

a. Radiative (band-to-band) recombination: An electron from the conduction band combines with a hole in valence band, releasing a photon of energy equal to that of the band gap. This is the preferred recombination pathway for light emitting diodes and lasers.
b. Shockley-Read-Hall (SRH) recombination: Due to defects in the crystal structure of the semiconductor, energy states are created within the band gap. Electrons in the conduction band can drop to this energy level prior to recombining with a hole in the valence band. In SRH recombination, the energy can be released as thermal energy.
c. Auger recombination: It is a recombination mechanism that involves three charge carriers: when an electron and hole recombine, the energy that is released is absorbed by another electron in the conduction band, exciting it to a higher energy state. This excited electron eventually falls back to the conduction band edge through thermal losses. Auger recombination is predominant when the concentration of the light generated excess carrier is significant.

The total extent of recombination in the bulk of a semiconductor depends on the recombination through each of these mechanisms, and can be quantified by defining the minority carrier lifetime, τ_{bulk}, as

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{band}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}}, \tag{1.5}$$

and

$$\tau_{bulk} = \frac{\Delta n}{Recombination\ rate} \ . \tag{1.6}$$

The bulk recombination lifetime can also be related to the average diffusion length (L_{diff}) of a light-generated carrier from its point of origin to the point of recombination as $L_{\text{diff}} = (D \cdot \tau_{\text{bulk}})^{0.5}$, where D is the diffusion coefficient for a charge carrier. Silicon being an indirect band gap material has a low absorption coefficient for the incident photons, and the most optimum Si wafer thickness is ~100 μm for highest efficiency [8]. However, to minimize cell breakage due to structural limitations of *c*-Si wafers in manufacturing, the *c*-Si wafers used in solar cells are ~170 μm thick. Hence, having a high carrier lifetime and diffusion length of the base *c*-Si wafer is critical for producing high-efficiency devices, as the light-generated carriers need to travel through the thickness of the device without recombining to be collected at the metal contacts near the surface.

Surface recombination: Besides bulk recombination of charge carriers, another major pathway for recombination is at the semiconductor surface. The periodicity of the crystal lattice of the semiconductor is disrupted at the surface or interface creating unsatisfied or dangling bonds, which act as recombination centers. Due to surface recombination, a region of low carrier density is created near the surface, and carriers from the bulk which are at a higher concentration diffuse towards the surface under illumination. Hence, the rate of surface recombination depends also on how fast the carriers from bulk can diffuse towards the surface, and is quantified by the term, surface recombination velocity (S, cm/s). While an extremely well-passivated surface will have a very low S, the S for a surface with heavy recombination is limited to ~10^7 cm/s. This is because, the maximum velocity at which carriers can move is limited to ~10^7 cm/s for most semiconductors.

Various methods are used to reduce the surface recombination velocity and will be described in detail shortly.

1.3.3. Passivation of a solar cell

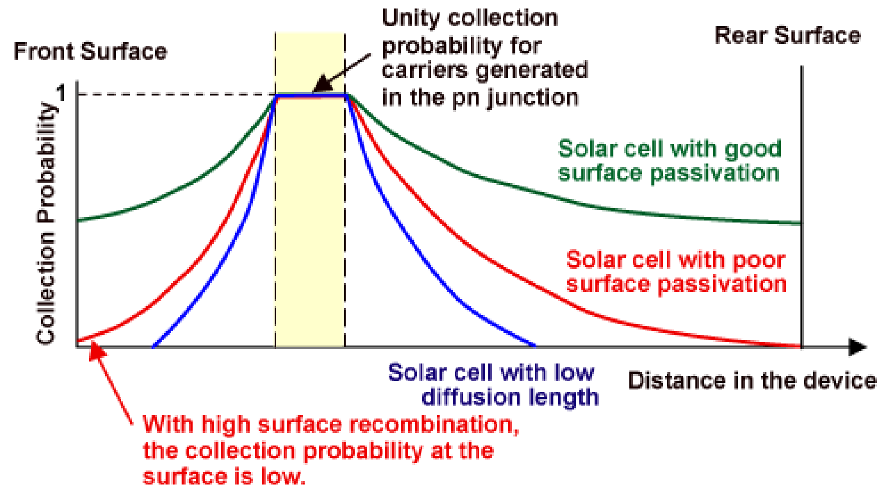

Figure 1.6 Charge collection probability versus the distance for charge collection at the front and rear contacts in a solar cell. The three curves on each side of the *p-n* junction represent collection probabilities for three different levels of surface passivation. Figure reproduced from Ref. [25].

The importance of passivation in a typical solar cell architecture is illustrated in Fig. 1.6. A well-passivated device will have low recombination losses. Electron-hole (e^--h^+) pairs can be generated throughout the thickness of the device, and need to be separated by the junction before they recombine. A poor-quality bulk material will have a short carrier diffusion length and, hence, only the e^--h^+ pairs created near the junction will be separated quickly and collected. Similarly, if surface passivation is poor, e^--h^+ pairs will rapidly recombine near the semiconductor surface/interface resulting in losses. Thus, a high-efficiency solar cell needs to have excellent passivation throughout the device.

<u>Improving bulk lifetime</u>: As previously mentioned, recombination in the Si-bulk can occur due to presence of defects which can act as Shockley-Read-Hall recombination centers. These defects

can be either crystallographic defects, thus creating a disruption in the periodicity of the crystal, or defects due to presence of impurities, i.e. non-Si atoms. The extent of such defects and/or impurities can be controlled at two processing stages: either during the casting or ingot fabrication step, and after an ingot is sliced into Si wafers.

a. Ingot level: The ingot fabrication process has a significant impact on the extent of defects and impurities in the Si ingot. The three most common ingot manufacturing processes are: casting process for multicrystalline Si, Czochralski (Cz) process for monocrystalline Si, and float zone (Fz) process also for monocrystalline Si. These have been listed in the increasing order of their costs, and bulk lifetimes. While the general process of ingot manufacturing is well known, the final crystal quality significantly depends on the processing conditions, which are usually trade-secrets of the wafer manufacturer. Amount of incorporated metal impurities, intrinsic defect concentration, doping uniformity and oxygen content are a few factors that are influenced by the crystal growth process and can affect cell performance [26, 27].

b. Wafer level: Si wafers formed after dicing a Si ingot can also be processed to improve the lifetime of the Si bulk. The amount of metal contaminants in the wafer bulk can be significantly reduced by a $POCl_3$ gettering process, thus resulting in higher lifetimes [28, 29]. The wafers are annealed in the presence of $POCl_3$ and O_2 gas mixture, forming a P rich layer near the wafer surface, which selectively getters the metal contaminants. This layer can be left as is or can be subsequently etched off resulting in high bulk lifetimes. For Cz-Si, oxygen precipitates can form and grow during high temperature processing, and act as recombination sites [30]. One of the ways to improve the quality of Cz wafers, and get rid of the oxygen precipitates is a thermal processing step called *Tabula Rasa* (TR) [31],

which improves carrier lifetime. This process essentially involves flash annealing of the *c*-Si wafer at temperatures of 1050–1100 °C. For multicrystalline Si wafers, the passivation of the grain boundaries is challenging, and is usually achieved by hydrogenation of the grain boundaries by deposition of a hydrogen-rich layer, e.g. SiN_x, followed by a thermal annealing process [29].

Improving surface passivation: Surface passivation is critical for high-efficiency solar cells because the metal contacts which collect the photo-generated carriers, are present at the wafer surface. Poor surface passivation can significantly reduce the carrier concentration near the surface, resulting in lower solar cell efficiency. The effective surface recombination velocity, S_{eff}, can be written as [32]

$$S_{eff} = \frac{1}{\Delta n_d} \times \frac{n_s p_s - n_i^2}{\frac{n_s + n_i}{S_{p0}} + \frac{p_s + n_i}{S_{n0}}} , \tag{1.7}$$

where n_s and p_s are the steady-state carrier concentrations at the surface, Δn_d is the excess minority carrier concentration at the edge of the space charge region near the surface, and n_i is the intrinsic carrier concentration. S_{p0} and S_{n0} are the hole and electron recombination velocity and written as

$$S_{p0} = v_{th,p} D_{it} \sigma_p \text{ , and } S_{n0} = v_{th,n} D_{it} \sigma_n , \tag{1.8}$$

where $v_{th,p}$and $v_{th,n}$ are the thermal velocity of holes and electrons, respectively, D_{it} is the interface defect density, and σ_p and σ_n are the hole and electron capture cross-section respectively.

Based on the above two equations, there are two strategies to reduce surface recombination velocity, and hence, the extent of surface recombination.

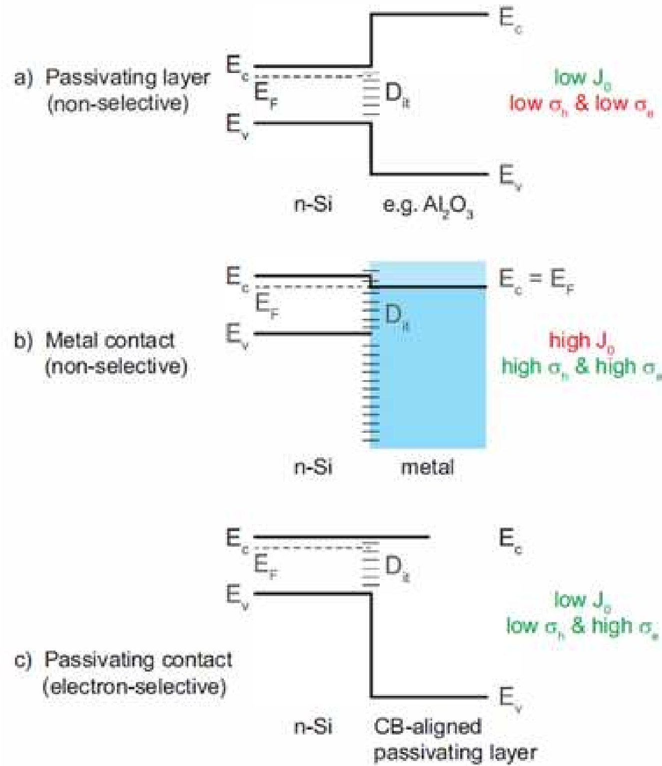

Figure 1.7 Schematic of band diagrams of various contacting materials with *c*-Si. E_c and E_v are the conduction and valence band edges, respectively. E_F is the Fermi level. σ_h and σ_e are the mobilities of the holes and the electrons, respectively. D_{it} is the interface defect density. J_o is the surface recombination current. Figure reproduced from Ref.[33].

a. Chemical passivation: One way to lower S_{eff} based on Eq. 1.7, is to reduce the rate at which defect states capture electrons and holes, i.e. lower S_{n0} and S_{p0}. This is achieved by either reducing the number of defect states, or reducing the carrier capture cross-section (see Eq. 1.8). Such a passivation scheme, referred to as chemical passivation, involves reducing the dangling bonds and other defects at the *c*-Si surface, and can be achieved by growing dielectrics or wide bandgap semiconductors on the *c*-Si surface. Such passivating layers include silicon dioxide (SiO_2) [34], hydrogenated amorphous silicon nitride (*a*-SiN_x:H) [35], hydrogenated amorphous silicon (a-Si:H) [36], and aluminum oxide (Al_2O_3) [37, 38]. Interface states, which cannot be passivated by film deposition, can be further

passivated by annealing in hydrogen. It is speculated that the improved passivation is achieved by the H originating from either the deposited dielectric layers, and/or from the gas phase [39]. While the deposited dielectric layers provide excellent surface passivation, they do not have good electrical transport properties for holes and electrons due to the conduction and valence band offsets as shown in Fig. 1.7a.

b. Field-effect passivation: Another way to lower S_{eff} based on Eq. 1.7, is to reduce the concentration of either electrons or holes, i.e. lower n_s or p_s, respectively. This is because both an electron and a hole are required for recombination to occur. The presence of an electric-field near the surface, which selectively repels away either electrons or holes from the surface, reduces their surface concentration, and hence the surface recombination rate. Such a passivation scheme is referred to as field-effect passivation [32]. The excellent surface passivation obtained using Al_2O_3 and SiN_x films is due to, chemical passivation from an interfacial SiO_x layer, and field-effect passivation from the negative and positive fixed charge [32, 35, 37, 38, 40] in these films, respectively. Recently, excellent surface passivation has also been demonstrated by using ionic polymer based films such as Nafion [41]. However, these films do not form an interfacial layer to reduce the dangling bond density at the *c*-Si surface. As a result, the chemical passivation is very poor, but excellent passivation is obtained purely via field-effect passivation, since these films have 1–2 orders of magnitude higher fixed charge than conventional thin-films. In addition to obtaining excellent surface passivation, field-effect passivation is also quite important in reducing the recombination at the metal–*c*-Si interface at the points of contact. A metal-semiconductor contact can be a heavy recombination site, as metals can create several states within the forbidden bandgap of *c*-Si as shown in Fig. 1.7b. These interface states

cannot be passivated by any chemical passivation methods. Instead, by making the contact charge-selective via field-effect passivation, the recombination at the metal to *c*-Si interface can be significantly reduced. This is achieved by heavily doping the semiconductor right underneath the metal contact [42], forming a high-low junction which can be either p^+-p or n^+-n thus creating an electric field making it charge-selective. This ensures that only electron or only holes are present at the metal to *c*-Si interface thus reducing recombination. However, there is a trade-off as heavy doping enhances recombination in the doped region.

Based on the above we can say that the requirements of low recombination contacts are good surface chemical passivation, carrier selectivity (high V_{oc}), and low contact resistance (high *FF*) as shown in Fig. 1.7c. Additionally, they should allow incident light to pass through them without significant absorption (high I_{sc}). Such contacts are termed as passivating contacts, and are the focus of this thesis. For the purpose of this thesis, we may also refer to them as "passivated" contacts.

1.3.4. Light-trapping in a silicon solar cell

As shown in Eq. 1.4, the efficiency of a solar cell depends in the I_{sc}, which is essentially a metric of how well light can be absorbed by the solar cell resulting in excited e^--h^+ pairs. Since *c*-Si is an indirect bandgap material, and hence a poor absorber of light, efficient light-trapping schemes are critical for high-efficiency *c*-Si solar cells. As a result, the *c*-Si wafer needs to be significantly thicker, at least 110 µm [8], as compared to other absorber materials like *a*-Si, CdTe, GaAs, etc., which can be a few microns thick (Fig. 1.8). But higher thickness by itself is not sufficient, and to ensure that most of the incident light is absorbed in a *c*-Si solar cell, three schemes are used: (a) the front-side surface of a Si solar cell is textured; (b) an anti-reflection coating (ARC)

is deposited on the front-side; and (c) the back-side of the cell has a reflective metal layer, which reflects any light not absorbed by the Si in the first pass back into the cell. The metal layer also serves as a back-contact. Surface texturing of a Si(100) wafer is performed using a KOH-based wet chemical etching process [43]. The resulting surface texture (see Fig. 1.9a) has 1–10 μm wide square pyramids with their edges along the Si(110) direction and their faces along the Si(111) plane. Such a surface is referred to as a random pyramidal textured Si surface. Figure 1.9b shows that texturing significantly reduces the reflectivity of the surface as compared to flat Si surface. The reflectivity is further reduced by an ARC layer such as SiN_x, which is optimized for complete reflection of a particular wavelength of light, and this is usually done for 600 nm as it generates the most power in the cell. All these schemes result in a higher I_{sc} and hence, higher cell efficiency.

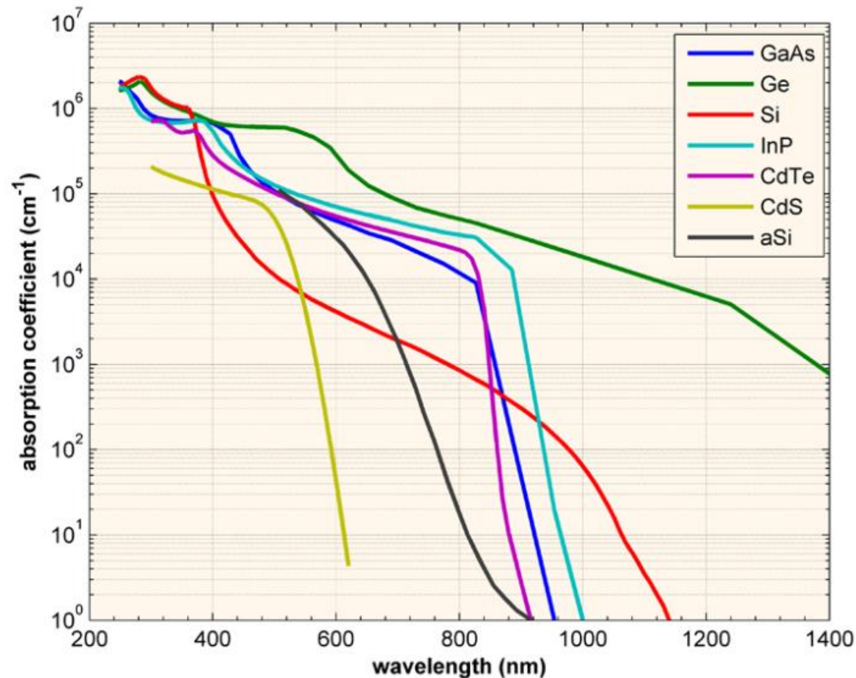

Figure 1.8 Wavelength dependent absorption coefficient of different absorber materials. Figure reproduced from Ref. [44].

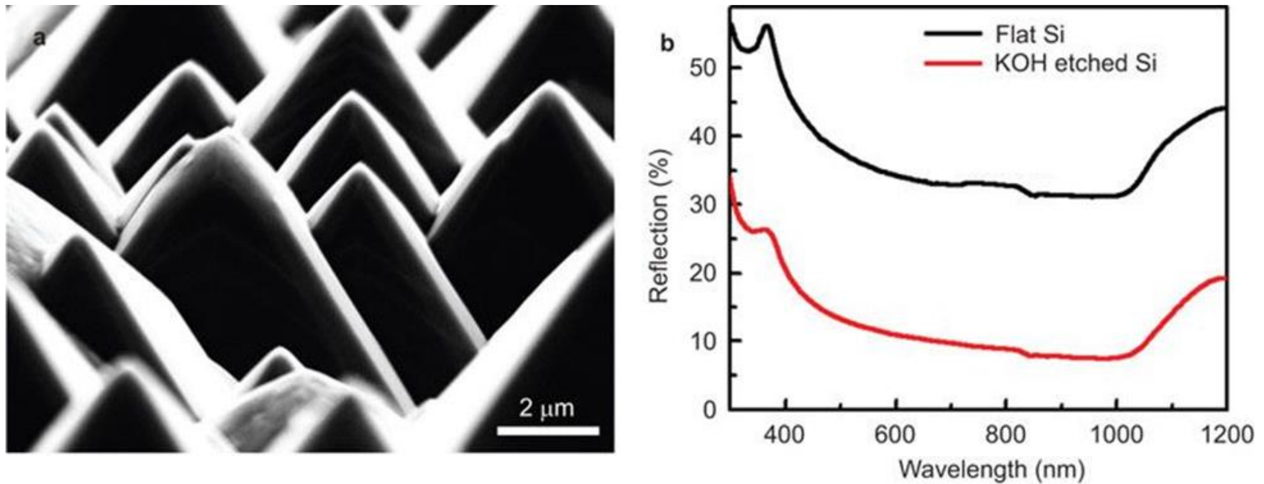

Figure 1.9 (a) SEM image of KOH-etched *c*-Si surface. (b) Reflection spectra of a flat (black) and textured (red) Si surface. The reflection value at 300 nm wavelength is also listed. Figure edited from Ref. [45].

1.4. Types of crystalline silicon solar cells

Starting with *c*-Si wafer as a base, a number of cell designs have been studied. These use different passivating layers as well as have different geometrical structures. A few of the most common cell designs are shown in Fig. 1.10 [46]. In general, we can classify solar cells as homojunction and heterojunction cells. This nomenclature is based the types of materials used to create the *p*-*n* junction. In homojunction *c*-Si cells, the active material is only *c*-Si, while in heterojunction cells, it is *c*-Si along with *a*-Si:H, and specific metal oxides as transparent conductors or tunneling transport layers.

The most basic solar cell is the homojunction *c*-Si solar cell with a full-area, front-side diffused emitter and SiN_x ARC (see Fig. 1.10a). Front metal contacts are formed using a screen-printed Ag-paste firing process. This involves screen printing the paste on top of the SiN_x ARC layer, followed by a >800 °C short-annealing (firing) process. During the firing process, the paste components etch through the SiN_x layer [47, 48], and react with the underlying Si, forming a metal-

semiconductor contact. The back contact is a full-area Al contact, which is annealed at a high temperature after deposition to create a back-surface-field (BSF). The base *c*-Si wafer is *p*-type, and annealing causes the Al to diffuse into the *c*-Si creating a p^+ region (Al is a *p*-type dopant in Si) between the Al and *c*-Si. This creates a hole-selective, high-low, p^+-p junction contact. Such a cell structure has limited efficiency, 16–20%, because SiN_x and the full-area Al-BSF are not very good surface passivation layers. To improve surface passivation, the SiN_x layer can be replaced by an Al_2O_3/SiN_x stacked layer on both the front and the back side. Furthermore, the contact area of the Al-BSF is reduced to just a few percent of the total wafer surface area by making local contacts instead of a full-area contact. This is called the passivated emitter rear contact (PERC) or passivated emitter with rear locally diffused (PERL) cell (see Fig. 1.10b). Al_2O_3 films provide excellent surface passivation with low recombination velocities (< 5 cm/s) [49], by forming a thin SiO_x layer at the interface [50-52]. Al_2O_3 also induces a fixed negative charge [40], thus providing field-effect passivation for cells fabricated from *p*-type *c*-Si wafers. The metal still contacts directly to *c*-Si, with a local BSF at the back resulting in losses at the metal to *c*-Si interface. On the rear side, contacts are formed by locally etching of the Al_2O_3/SiN_x stack via laser ablation, followed by screen-printing and firing of the metal paste. Efficiencies of ~24% have been reported for such a cell [53], and these have a efficiency potential of ~24% on an industrial scale as well [54]. Since metal does not allow for the transmission of light, the metal contacts on the front side also result in shadowing losses in the cell. This problem can be remedied by the interdigitated-back-contact (IBC) *c*-Si solar cell (see Fig. 1.10c) [55], consisting of alternating p^+- and n^+-Si regions to which the metal is contacted. Such a cell has resulted in efficiencies as high as ~25% using diffused emitters and conventional contacting schemes.

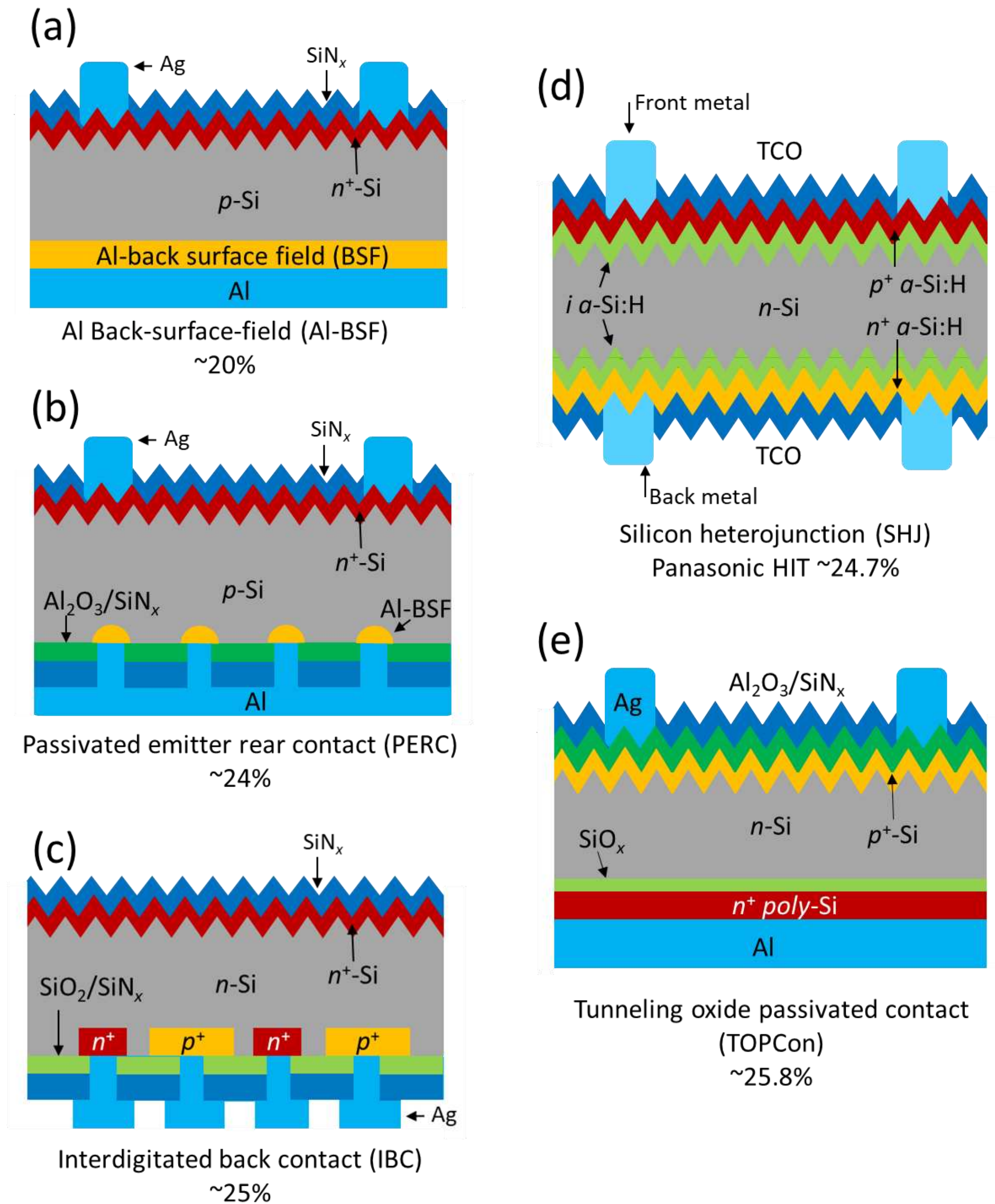

Figure 1.10 Types of c-Si based solar cells. Figure modified from Ref. [46].

In the above cell structures, the metal connects to the c-Si directly resulting in significant recombination at the metal to c-Si interface. The passivated contact device eliminates this by using

other semiconductor materials for contacting. The original Panasonic heterojunction cell with intrinsic thin layer (HIT) consists of *a*-Si:H as passivating layer (see Fig. 1.10d). Efficiencies as high as 24.7% have been reported for such devices, respectively. The cell is based on the concept of separating the metal contact from *c*-Si using passivating conductive films with a wider bandgap than *c*-Si [56]. *a*-Si:H layers are good buffering layers as their bandgap is slightly greater than *c*-Si, and can be easily doped during the growth process [57]. The cell has a thin intrinsic *a*-Si:H (*i a*-Si:H) layer in direct contact with *c*-Si, which provides surface chemical passivation. The doped *a*-Si:H layer on top of this *i a*-Si:H layer provides the necessary field-effect passivation and charge separation. On top of this doped *a*-Si:H layer is a transparent conductive oxide (TCO) such as indium tin oxide (ITO), hydrogenated indium oxide, or Zn-doped indium oxide [58]. TCOs act as antireflection coatings, and are required for charge collection as doped *a*-Si:H has poor lateral conductivity. In HIT cells, as the metal is not contacting *c*-Si directly, recombination losses associated with metallization are low. Cheaper metals such as Cu can be used instead of Ag as the ITO layer is a good barrier to Cu [59]. However, HIT cells pose certain limitations as well, which are outlined below.

- Processing temperatures limited to below 200–250 °C;
- Carrier lifetime in the amorphous layers is low and, hence, any absorption in this layer on the front side is mostly parasitic [60];
- Doping of TCOs makes them more conducting, but free carriers also cause more parasitic absorption losses.

The current leader in non-IBC *c*-Si cell efficiencies (25.8%) is the tunneling oxide passivated contact (TOPCon) cell (see Fig. 1.10e) [61]. The concept behind its development is similar to the HIT cell. It uses a 1–2 nm thick SiO_x on *c*-Si, and doped polycrystalline Si (*poly*-Si)

on SiO_x, to create a *c*-Si/SiO_x/*poly*-Si passivated contact structures. SiO_x is a very good surface passivation layer for *c*-Si due to the low *c*-Si/SiO_x interfacial defect densities, ~10^9–10^{11} $cm^{-2}eV^{-1}$, and can provide electrical transport through tunneling when the SiO_x layer thickness is <1.5 nm [62, 63]. For contacts with SiO_x thickness >2 nm, the electrical transport occurs through 10s of nanometers large local conduction pinholes in the SiO_x layer. These conduction pinholes can be regions of either tunneling SiO_x layer [64], and/or regions where the SiO_x layer is absent [65]. Heavily doped *poly*-Si layers on tunneling SiO_x have been shown to provide good field-effect passivation [66, 67]. The separation of the *poly*-Si layer from *c*-Si through SiO_x is critical as it prevents the epitaxial growth of the *poly*-Si layer during crystallization. In the TOPCon structure, the *poly*-Si/SiO_x passivated contact is only present on the rear side. The front side is a diffused boron emitter limiting solar cell efficiency. A higher cell efficiency of ~26.1% has been reported by using the n^+ and p^+-*poly*-Si/SiO_x contacts on the rear side of an IBC cell architecture [68]. Similarly, a ~26.7% cell has been reported using a SHJ-IBC cell approach, and holds the current single-junction *c*-Si cell efficiency record [69]. However, even though IBC cells result in record high-efficiencies, the large of processing steps involved makes the IBC cell architecture unsuitable for current large-scale industrial manufacturing.

1.5. Challenges with *poly*-Si/SiO_x passivated contacts

While *poly*-Si/SiO_x contacts have resulted in excellent cell efficiencies, a few aspects are still not well understood, and limit the technological application of these contacts.

a. Carrier conduction mechanism through the SiO_x layer: The ideal SiO_x thickness for passivation and carrier conduction is not clear. Contacts with SiO_x thicknesses between 1.4–2.2 nm have been successfully demonstrated [61, 68, 70], but it is also known that the

tunneling probability through the SiO_x layer significantly reduces with increasing SiO_x thickness [62], leading to series resistance losses in the solar cell. Hence, in addition to conduction through tunneling, conduction through local openings in the SiO_x layer, i.e. "pinholes", and/or a mix of tunneling and pinhole conduction have been proposed [63, 65, 67, 71-73], to explain the conduction through thicker SiO_x layer contacts.

b. Poor passivation of boron-doped contacts: Boron-doped *poly*-Si/SiO_x contact result in significantly poorer passivation than phosphorous-doped contacts. This has been observed by several research groups [70, 74, 75], and is likely related to the accumulation of B in the SiO_x layer [76, 77], causing a degradation of the passivation quality. Improvements in the p^+ *poly*-Si/SiO_x passivation has been demonstrated by doping with Ga instead of B, but the final contacts were not conductive enough for solar cell application [78].

c. Poor passivation on a textured Si surface: While excellent passivation using *poly*-Si/SiO_x contacts has been demonstrated on polished and planar Si surfaces, the contact passivation is significantly poorer on a pyramidal textured Si surface [79]. The increased recombination has been related to a net higher defect density at the SiO_x/*c*-Si interface [79-81], which has a dominant Si(111) crystallographic orientation on a textured Si surface instead of Si(100) orientation on a planar surface. However, even on a textured surface, the poorer passivation is more prominent for B-doped, than P-doped contacts [82]. This suggests that recombination mechanisms due to reasons other than the high-defect density of SiO_x/Si(111) interface are limiting the passivation quality.

d. Blistering of *poly*-Si/SiO_x contacts: During *poly*-Si/SiO_x contact processing, a *a*-Si:H layer is deposited on an oxidized wafer surface, and the contact is then annealed to temperatures >850 °C. Blistering of the deposited *a*-Si:H layer, and blistering during crystallization to

poly-Si can lead to film discontinuity, and hence need to be addressed [83-85]. Blistering occurs due to the release of H_2 from the *a*-Si:H films, and due to poor adhesion of the *a*-Si:H or *poly*-Si film to the underlying SiO_x layer [86]. The extent of blistering is affected by the *a*-Si:H growth conditions [87, 88], *a*-Si:H to *poly*-Si annealing conditions [84], and surface conditioning of the underlying SiO_x layer [70, 89]. The process used for deposition of *a*-Si:H affects the H content on the films, thus affecting the extent of blistering. Hence, blistering is observed to a higher extent in plasma-deposited *a*-Si:H than in low-pressure chemical vapor deposited *a*-Si:H layers [90, 91].

e. Screen-printed metallization of *poly*-Si/SiO_x contacts causes degradation of passivation: The current method for front-side metallization of crystalline Si (*c*-Si) solar cells is based on fire-through screen-printed Ag paste, which after printing is heated at high temperatures, ~800 °C, to create a metal contact to the *c*-Si emitter. The contact forms after penetration of the paste through the SiN_x anti-reflection coating and the Al_2O_3 passivation layer [47, 48]. Similarly, non-fire through pastes also exists, which are directly applied on the *c*-Si surface on rear-side of solar cells, and annealed at ~800 °C. In both paste types, the components from the metal paste react with the Si, forming a contact. Such a metallization strategy causes significant degradation of the *poly*-Si/SiO_x contact due to the paste components consuming the *poly*-Si/SiO_x contact layers [92]. While, this can be mitigated by growing ~200 nm thick *poly*-Si layers [93], the thicker *poly*-Si layers cause optical losses as discussed later. Hence, development of metallization paste-chemistries which will mitigate such a damage to the contact by reacting with only a few nanometers of the *poly*-Si surface, or stopping at the *poly*-Si surface is of interest [94].

f. Optical losses due to parasitic absorption in *poly*-Si layer: *Poly*-Si has a similar bandgap to *c*-Si, and needs to be heavily doped to reduce the metal-to-*poly*-Si contact resistance. Hence, when *poly*-Si is used on the front side of the solar cell it causes significant parasitic absorption losses. Similarly, it causes free-carrier absorption losses when used on the rear side. These optical losses can be reduced by thinning the *poly*-Si layer [95], but at the cost of increased recombination due to metallization, as discussed above. Another strategy is to use wider band-gap Si based materials such as nanocrystalline Si [96], or alloying the deposited *a*-Si:H with C or O [97, 98].

As noted above, there are significant fundamental and technological challenges associated with the industrialization of *poly*-Si/SiO_x passivated contacts for next generation Si solar cells. In this thesis we focus on understanding the carrier transport mechanism through the SiO_x layer, and the poor passivation of *poly*-Si/SiO_x contacts on a textured Si surface.

1.6. Types of Si thin films and monocrystalline Si ingot manufacturing

Now that we have discussed some of the important aspects of Si solar cells, and the strategies used to improve solar cell efficiency, it is important to clarify a few things about vapor deposition of Si thin films, and bulk Si growth. This is important since the electrical and optical properties of Si are vastly influenced by its bonding structure, and also the way Si ingots are grown.

1.6.1. Amorphous, nanocrystalline and polycrystalline silicon

High-efficiency cells require thin films for obtaining excellent surface passivation and conduction. Some of these thin films are based on Si and can be classified as amorphous, nanocrystalline, or polycrystalline. The electronic and optical properties of these films depend on the nanostructure and bonding configuration. Amorphous silicon (*a*-Si) is characterized by short-

range order. While the Si-Si bond lengths and nearest-neighbor atomic configurations in *a*-Si are very similar to *c*-Si, which results in short-range order up to the first two coordination shells, however, unlike *c*-Si there is no long-range order. Hydrogenated *a*-Si (*a*-Si:H) deposited from plasmas contains 5─10 atomic percent H, which passivates the dangling bond defects [99]. Nanocrystalline Si and polycrystalline Si (*poly*-Si) films contain crystalline Si grains that are a few nm to a few 10s of nm in size [100]. Unlike *poly*-Si, which primarily contains small *c*-Si grains only, nanocrystalline Si is a mixture of Si crystals embedded in an *a*-Si:H matrix. The different structural properties of these Si films result in different electrical and optical properties.

1.6.2. Types of monocrystalline Si wafers: Czochralski and float zone

Over the past few decades, considerable effort has been invested into manufacturing low defect density *c*-Si wafers. Czochralski (Cz) and float zone (Fz) are the two dominant manufacturing techniques [101]. Cz-Si is grown by drawing *c*-Si from a Si melt in a quartz crucible using a seed crystal. Temperatures as high as 1500 °C are used, which result in incorporation of oxygen (>10^{18} atoms/cm^3) and carbon (>10^{17} atoms/cm^3) contaminants from the crucible into the melt. This is avoided in Fz process by locally heating a polycrystalline rod using a radio frequency field, and then drawing a single crystal from it. As there is no direct contact with the heating element and no crucible is present (hence the name), Fz-Si has oxygen and carbon concentrations <10^{16} atoms/cm^3. Cz-Si is the choice for industrially-feasible high-efficiency solar cells due to its low cost and higher impurity tolerance [102].

1.7. Working principle of measurement techniques used

In this section we will briefly describe the working principle of a few measurement techniques which are relevant to this thesis.

1.7.1. Sinton lifetime spectroscopy

The effectiveness of the bulk and surface passivation of a Si wafer can be determined using the 'Sinton lifetime tester' (WCT-120) instrument (see Fig. 1.11). It works on the quasi-steady-state-photoconductance (QSSPC) lifetime measurement method developed by Sinton [103-105]. It uses a flash lamp to create excess carriers in the Si wafer. Their concentration and decay rate are then determined using an in-built radio frequency (rf) coil at the base of the instrument, which measures the change in photoconductance as a result of the generated excess carriers. The change in photoconductance ($\Delta\sigma_L$) is related to the excess carrier concentration (Δn), electron and hole mobilities (μ_n, μ_p), and thickness (W) of the wafer as

$$\Delta\sigma_L = q\Delta n(\mu_n + \mu_p)W. \tag{1.9}$$

Based on this, the effective carrier lifetime, τ_{eff} can be written as

$$\tau_{eff} = \frac{\Delta\sigma_L}{J_{ph}(\mu_n + \mu_p)}, \tag{1.10}$$

where, J_{ph} is the photogeneration rate determined using a reference wafer and $\Delta\sigma_L$ is measured by the rf coil thus giving the effective lifetime. For a n-type wafer with dopant concentration (N_D), the extent of quasi-fermi level splitting, i.e. i-V_{oc}, can be written as

$$i\text{-}V_{oc} = \frac{kT}{e} ln\left[\left(\frac{\Delta p(N_D+\Delta n)}{n_i^2}\right) + 1\right], \tag{1.11}$$

where, n_i is the intrinsic carrier concentration in the semiconductor. It must be noted that the instrument measures average values over the sample area above the coil which can be a few centimeters in diameter. Both, τ_{eff} and i-V_{oc} quantify the extent of total passivation, i.e. the bulk and the surface. The contribution of surface passivation to the total passivation can be quantified

by the surface recombination velocity (S_{eff}), or the emitter recombination current density, J_o. While S_{eff} is usually used to quantify the extent of chemical passivation, J_o is typically used to quantify the emitter quality, and can also be extended to quantify the extent of surface passivation in the presence of an electric field [106]. Under high-injection condition, these various parameters are related by the equation,

Figure 1.11 Sinton lifetime tester WCT-120 from Sinton Instruments. Figure reproduced from Ref. [107].

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{eff}}{W} + \frac{J_o\left(N_{dop} + \Delta n\right)}{q n_i^2 W} + \frac{1}{\tau_{Auger}}. \quad (1.12)$$

Equation 1.12 is valid for a Si wafer with an emitter on one side (J_o), and passivated with a dielectric layer on the other side (S). Rearranging the terms results in,

$$\left(\frac{1}{\tau_{eff}}-\frac{1}{\tau_{Auger}}\right)=\left(\frac{J_o}{qn_i^2W}\right)\Delta n+\left(\frac{1}{\tau_{bulk}}+\frac{S_{eff}}{W}+\frac{J_oN_{dop}}{qn_i^2W}\right). \quad (1.13)$$

Equation 1.13 is a straight line of the form $y = mx + c$, with Δn as the dependent variable. This allows for the calculation of the J_o term, thus quantifying surface passivation quality.

1.7.2. Photoluminescence imaging

Passivating layers which will be studied in this work should not only provide good passivation but should also be resistant to metallization damage. Metallized Si wafers cannot be tested using the Sinton tool as the metal interferes with the coupling of the rf from the coil with the semiconductor. Hence, to determine the carrier lifetime after metallization, we will use the photoluminescence (PL) imaging technique [108, 109]. This technique uses an in-house 810 nm laser diode as an excitation source, and a digital camera with a GaAs filter to block the laser diode light is used for imaging the *c*-Si wafer as shown in Fig. 1.12. Areas of the wafer which are well passivated appear bright as they have a higher carrier concentration leading to a higher band-to-band recombination while those with poor passivation appear dark. PL is also useful to image spatial nonuniformities in the passivation quantity. The intensity of PL (I_{PL}) for a *n*-type wafer is related to the excess carrier concentration (Δn) as,

$$I_{PL} = A_i B \Delta p(N_D + \Delta n), \quad (1.14)$$

where, A_i is the scaling factor and B is radiative recombination coefficient. The *i*-V_{oc} can then be related to the PL intensity as

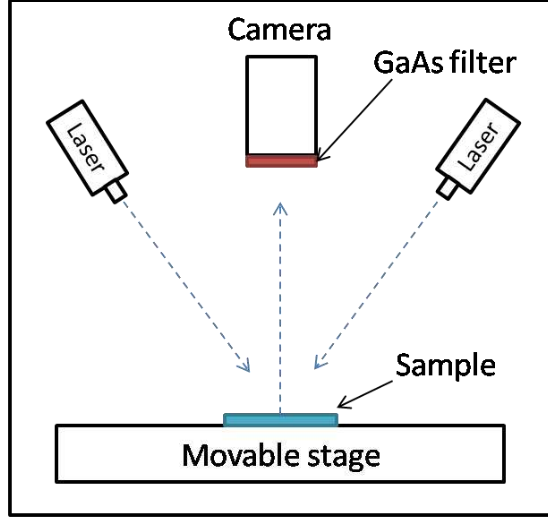

Figure 1.12 Schematic of the photoluminescence imaging setup.

$$i\text{-}V_{oc} = \frac{kT}{e} ln\left(\frac{I_{PL}}{A_i B n_i^2}\right). \qquad (1.15)$$

Thus, the effect of various processing steps (here 1 and 2) on the i-V_{oc} can be determined using Eq. 1.16.

$$\Delta iV_{oc\ 1\rightarrow 2} = \frac{kT}{e} ln\left(\frac{I_{PL,\ 2}}{I_{PL,\ 1}}\right). \qquad (1.16)$$

1.7.3. Transmission line method

Determination of the contact resistance, R_c, between metal contacts and the underlying semiconductor film as well as the sheet resistance, R_s, of the semiconductor film in semiconductor devices is important as it can directly affect device performance. For example, the fill-factor for a solar cell (refer to Section 1.3.1) is dependent on the series resistance in the cell. Hence, to determine the electrical conductivity of the contacts discussed later in Chapters 2 and 3, we need to perform transmission line method (TLM) measurements, which are described below.

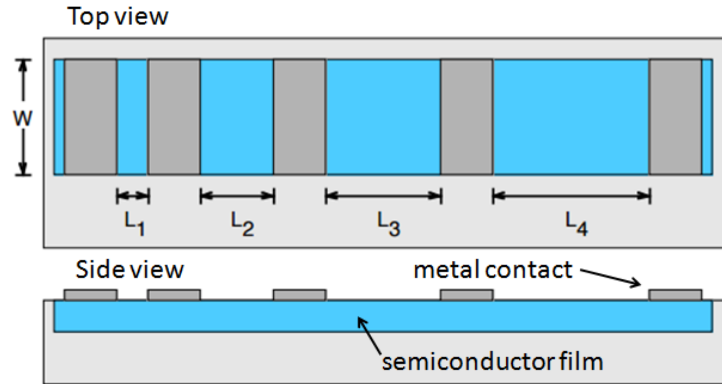

Figure 1.13 Schematic of structure for TLM measurement. Figure reproduced from Ref. [110].

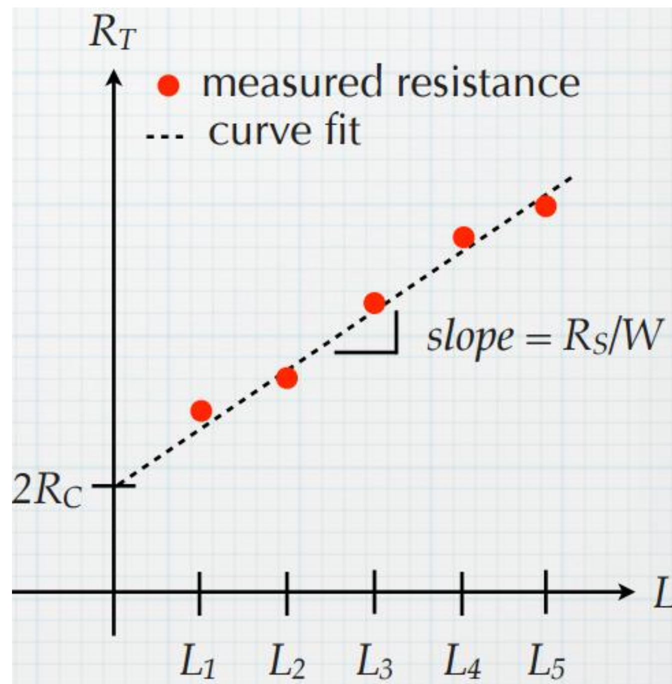

Figure 1.14 Determining contact and sheet resistance from TLM measurement. Figure reproduced from Ref. [110].

As shown in Fig. 1.13, metal contacts with the same area are deposited at different known distances (L_1, L_2, L_3, …) on a semiconductor film. The resistance, R_T, between two neighboring metal contacts is related to R_s and the distance between the contacts L_i $(i = 1, 2, 3 \ldots)$ as

$$R_T = \frac{R_s}{W}(L_i + 2L_T), \quad (1.17)$$

where, W is the width of the metal contact and L_T is the transfer length of the contact, i.e., the effective distance an e^- traverses below the two contacts before being collected. L_T can be related to R_c as

$$R_c = \frac{R_s L_T}{W}. \quad (1.18)$$

By plotting R_T as a function of L_i as shown in Fig. 1.14, the sheet and contact resistances can be determined from the slope and the intercept, respectively.

1.7.4. Electron-beam induced current

Electron-beam induced current (EBIC) is a technique used to quantify the local passivation and electrical properties in a semiconductor device [111, 112]. The measurement is performed in a scanning electron microscope (SEM). Two electrical connections are made to the sample on either sides of a *p*-*n* or a high-low junction prior to mounting in the SEM. A focused electron beam within the SEM is used to locally generate electron-hole pairs in the sample. These carriers are separated by the built-in electric field, and subsequent result in a current that is then mapped over the scanned region. Due to carrier diffusion and penetration of the electron beam into the semiconductor, the concentration of the excited carriers decreases with increasing distance from the point of incidence, as schematically shown in Fig. 1.15. The intensity in EBIC depends on the efficiency with which the excited carriers can be collected, thus resulting in a current. The presence of defects or inhomogeneities in the device lead to carrier recombination near the point of incidence of the electron beam, thus resulting in lower current. Similarly, inefficient collection of the excited carriers either due to the absence of an electric field, or due to carrier conduction

limitations results in a lower current. Thus, the carrier collection probability at a particular location in EBIC measurement depends on local defect density, presence of a local electric field, and local carrier conduction. Hence, EBIC measurements can result in maps which have either no features due to spatially uniform carrier collection, darker features due to poorer carrier collection, or brighter features due to enhanced local carrier collection. Some of the main advantages of EBIC is that it is a non-destructive technique and can be performed on actual device samples. The resolution depends on the semiconductor material and the energy of the incident electron beam, and can be as low as 50 nm for Si. However, the biggest advantage of EBIC is that electrically active regions of interest can be imaged via the SEM itself. Such regions can also be marked and further analyzed via tools such as transmission electron microscopy (TEM). Thus, a one is to one correlation can be obtained between the electrical and structural property of the region of interest, making EBIC-SEM + TEM a very powerful technique.

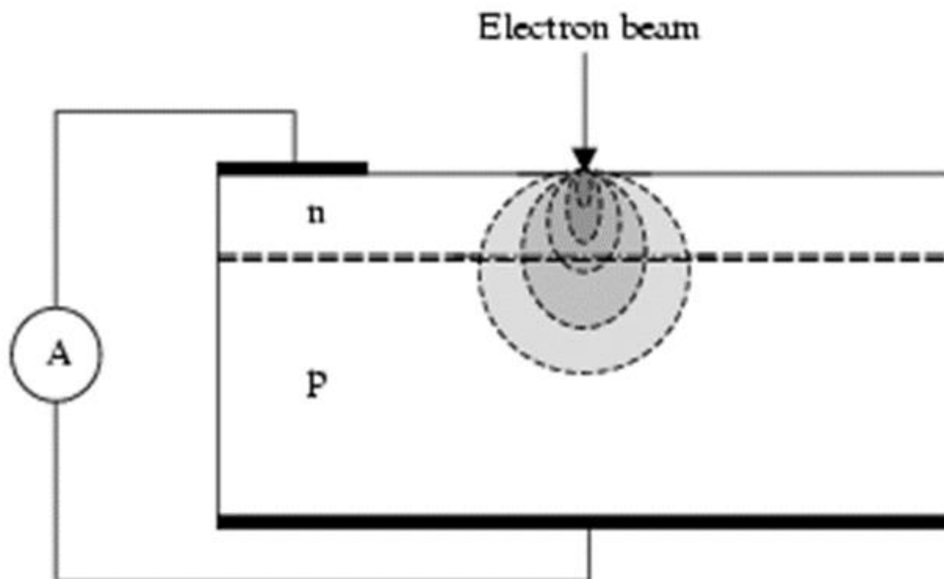

Figure 1.15 Schematic of EBIC measurement setup. The change in carrier concentration away from the point of incidence of the electron-beam is also qualitatively shown on a grey scale.

1.8. Thesis Outline

The work performed in this Ph.D. thesis is to develop a better understanding of technologies to enable high-efficiency and low-cost next-generation monocrystalline Si solar cells. Aspects related to passivation, surface texturing and metallization are studied. Chapters 2–5 relate to passivated contacts comprising of a metal/*poly*-Si/SiO_x/*c*-Si contact stack, to enable next-generation Si photovoltaic (Si-PV) technologies. Chapter 6 relates to strategies to replace the current Ag-based metallization process with cheaper Cu-based metallization process for Si solar cells.

In Chapter 2, the role of SiO_x thickness within the *poly*-Si/SiO_x contact stack is discussed [113]. The best passivation is obtained for SiO_x thickness of 1.4–1.6 nm, when both the chemical passivation from the SiO_x layer and field-effect passivation from the doped *poly*-Si layer are optimized. While chemical passivation improves with increasing SiO_x thickness, field-effect passivation deteriorates with increasing SiO_x thickness. Furthermore, SiO_x layers <1.6 nm thick are sufficiently conductive for solar cell applications, but become significantly resistive when SiO_x thickness is >1.7 nm. The above results are valid only when the annealing temperature of a *poly*-Si/SiO_x/*c*-Si stack is limited to 850 °C.

Chapter 3 relates to understanding the interdependence between SiO_x thickness and *poly*-Si/SiO_x contact annealing temperature, on passivation and conductivity through the SiO_x layer [64]. While increasing annealing temperature deteriorates the chemical passivation, it improves field-effect passivation. Depending on the processing conditions, two different scenarios for conduction through the SiO_x layer are observed: uniform tunneling conduction or locally enhanced conduction. Transmission electron microscopy (TEM) images reveal that the locally enhanced conduction occurs through few 10s of nanometer size thinned-down tunneling SiO_x layer

regions, in an otherwise insulating SiO_x layer. These conduction-enabling nonuniformities in the SiO_x layer, referred to as "pinholes" are mapped via electron-beam induced current (EBIC) measurements.

Chapter 4 relates towards understanding the poorer passivation of *poly*-Si/SiO_x contacts on a textured surface as compared to a planar surface. Texturing improves the light-trapping properties of the Si cell, and hence is critical for high-efficiency devices. The effect of surface crystallographic orientation and surface morphology is investigated using both device and surface sensitive characterization techniques. We relate the poor passivation on a textured surface to nonuniformities in the SiO_x layer on a textured surface. These nonuniformities originate due to both the microscopic pyramidal textured Si surface morphology, and due to nanoscale roughness on the pyramid faces.

Chapter 5 relates to the modification of the pyramid textured Si surface using both basic and acidic wet chemical etching processes. The important parameters that affect etch-rate and the resulting surface morphology are determined. Etching affects the microscopic pyramidal shape, surface crystallographic orientation, surface area, and nanoscale roughness. While etching results in improved *poly*-Si/SiO_x contact passivation, the light-trapping properties of the Si surface also deteriorate after etching.

Finally, Chapter 6 relates towards metallization of Si solar cells using Cu [114]. Since Cu is a significant contaminant for Si, causing solar cell efficiency losses, Cu contacts on Si need a conductive Cu diffusion barrier interlayer. The effectiveness of Ni and NiSi barrier layers is studied. NiSi layers show both, better Cu diffusion barrier properties, and better thermal stability than Ni layers in a Cu/barrier layer/Si stack.

CHAPTER 2

EFFECT OF SILICON OXIDE THICKNESS ON POLYSILICON BASED PASSIVATED CONTACTS

Modified from a paper published in *Solar Energy Materials and. Solar Cells*[#]

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The contact structure studied in this thesis comprises of polycrystalline Si (*poly*-Si) and SiO_x layers on a monocrystalline Si (*c*-Si) wafer resulting in a *poly*-Si/SiO_x/*c*-Si stacked structure. This contact structure needs to provide both passivation of the *c*-Si surface, while also allowing conduction of the photogenerated carriers through the *poly*-Si and SiO_x layers. Low resistivity of these layers is critical to enable high fill-factor of the resulting solar cell. While conductivity of the *poly*-Si layer can be improved by doping it with suitable dopants such as phosphorous or boron, SiO_2 is inherently an insulator, resulting in poor carrier conduction. However, when the SiO_2 thickness is <2 nm, carrier transport through the SiO_2 layer is possible through the tunneling mechanism. Hence, understanding the dependence of SiO_2 layer thickness on contact resistivity and passivation is critical for development of *poly*-Si/SiO_x passivated contacts and is the focus of this chapter.

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2.1. Abstract

In this chapter, we discuss the effect of SiO_x thickness (1–3 nm) on the performance of *poly*-Si/SiO_x/*c*-Si passivated contacts. Our results show that for both *n*- and *p*-type contacts, there is an optimum SiO_x thickness of 1.4–1.6 nm for obtaining the highest implied open-circuit voltage (i-V_{oc}) of ~739 and ~700 mV, respectively. For contacts with SiO_x thicker than 1.6 nm, the i-V_{oc} drops due to reduced field-effect passivation. We attribute this to the fact that a thicker SiO_x layer hinders the diffusion of both phosphorous and boron into the *c*-Si wafer, for the *n*- and *p*-type contacts, respectively, resulting in a junction that is very close to the *c*-Si/SiO_x interface, which increases carrier recombination most likely due to the presence of defects at this interface. The resistivity measured through the metal/*poly*-Si/SiO_x/*c*-Si stack is independent of SiO_x thickness up to 1.6 nm, and increases exponentially by several orders of magnitude with further increase in SiO_x thickness due to inefficient tunneling conduction. Finally, the extent of metallization-induced degradation of the *poly*-Si/SiO_x/*c*-Si contacts is worst for the thinnest SiO_x investigated (~1 nm), and interestingly it is not completely mitigated even for a ~3 nm thick SiO_x.

2.2. Introduction

Monocrystalline Si (*c*-Si) solar cells with passivated contacts based on the ultrathin SiO_x and doped polycrystalline Si (*poly*-Si) layers in a metal/*poly*-Si/SiO_x/*c*-Si structure can achieve efficiencies >25% [61, 68]. These contacts use a 1–2 nm thick tunneling SiO_x on *c*-Si, and doped *poly*-Si on SiO_x, to create a *poly*-Si/SiO_x/*c*-Si passivated contact structure [74, 115, 116]. The separation of the doped *poly*-Si layer from *c*-Si through SiO_x is critical as it provides a very low recombination interface to the wafer and prevents the epitaxial growth of the *poly*-Si layer during the required high temperature annealing of these contacts. The ultrathin ~1–2 nm SiO_x enables

electrical transport via tunneling [117-119], and/or pinholes in the SiO_x layer [67, 71, 120], and is a very good surface passivation layer for *c*-Si due to the low *c*-Si/SiO_x interfacial defect densities [121, 122]. Additional field-effect passivation is obtained due to the heavily doped *poly*-Si layer deposited on the tunneling SiO_x layer. A combination of these two passivation mechanisms leads to a very low emitter recombination current density, J_o [56, 67, 123]. The separation of the metal contacts from the *c*-Si absorber, via the use of the doped *poly*-Si/SiO_x stack helps reduce the metallization-induced carrier recombination, while enabling carrier separation and collection.

The high-temperature stability, excellent passivation, and manufacturing flexibility demonstrated by these contacts make them a suitable candidate for next-generation *c*-Si solar cell technologies. However, to incorporate them into industrial-scale manufacturing, it is important to understand their salient features while identifying the allowed processing windows for these contacts. Currently, in the literature, different techniques have been reported for the fabrication of the *poly*-Si/SiO_x/*c*-Si contacts. The SiO_x layer can be grown either via dry thermal oxidation [70] or by chemical oxidation with nitric acid [74, 116] or UV/O_3 [124]. Even though these SiO_x films have different stoichiometry, surprisingly they show marginal effect on the final passivated contact performance [124]. The doped *poly*-Si film can be grown via either plasma-enhanced chemical vapor deposition (PECVD) [70, 74] or low-pressure chemical vapor deposition [116]. Additionally, these *poly*-Si films can be doped in numerous ways such as during growth of hydrogenated amorphous Si (*a*-Si:H) [70], ion-implantation of intrinsic *poly*-Si [116], $POCl_3$ and BBr_3 thermal diffusion [75], or with suitable dopant pastes and inks [78]. The morphology of the doped Si layers can be either polycrystalline [70], microcrystalline [74], or an amorphous matrix embedded with Si nanocrystallites [98]. However, even with all these variabilities, the final contact performance is similar, with i-V_{oc} values being ~735–740 mV for phosphorous doped *n*-type and

~700–710 mV for boron doped *p*-type contacts [70, 74]. The only common feature in these contacts is that the tunneling SiO_x layer is ~1.5 nm thick, and the contacts need to be annealed between 850–900 °C after *a*-Si:H deposition for obtaining the highest i-V_{oc} values. The loss of performance upon annealing above 900 °C has been attributed to significant SiO_x break-up, which results in localized loss of the chemical passivation provided by the SiO_x layer [125, 126]. A different approach, the *poly*-Si on oxide (POLO) [71, 75] contacts reported by the Institute for Solar Energy Research in Hamelin (ISFH) have a very similar *poly*-Si/SiO_x stacked structure but with a thicker, ~2.2 nm, SiO_x. However, these contacts are processed at a much higher temperature of ~1000–1050 °C to achieve record high i-V_{oc} values of 748 and 729 mV for both the *n*- and *p*-type contacts, respectively [82]. For these POLO contacts, the higher temperature is quite crucial since it results in pinholes in SiO_x that provide direct conduction pathways between the *poly*-Si and underlying *c*-Si absorber resulting in very low through-contact resistivities [71, 120, 127].

Here, we focus on understanding the role of the thickness of the thermally-grown SiO_x layer on the contact performance where the contact annealing temperature is limited to 850 °C. Under these conditions, we do not expect SiO_x breakup, which can significantly affect charge transport and surface passivation. We show that SiO_x thickness within 1.4–1.6 nm leads to the highest i-V_{oc} values of ~739 and ~700 mV for *n*- and *p*-type contacts, respectively. We hypothesize that this SiO_x thickness range provides an optimum balance between the chemical passivation from the SiO_x layer and the field-effect passivation from the dopants, as both of these depend on the SiO_x thickness. We show that carrier transport through the contact reduces by several orders of magnitude when the SiO_x thickness is increased from 1.6 to 1.9 nm due to inefficient tunneling. Finally, we show that the extent of metallization-induced degradation of the poly-Si/SiO_x contacts

is worst for the thinnest SiO_x investigated (~1 nm), and interestingly is not completely mitigated even for a ~3 nm thick SiO_x.

2.3. Experimental Details

As-sawn, phosphorous-doped, *n*-type Czochralski (*n*-Cz) Si(100), 8 Ω·cm resistivity, ~190 µm thick wafers (Woongjin Co. Ltd, South Korea) were subjected to a KOH based etch for planarization and saw-damage removal. The wafers were then cleaned using standard wafer cleaning procedures of piranha, RCA-1 and RCA-2 [128, 129], followed by a treatment with 1% aqueous HF to remove the SiO_x formed as a result of the RCA-2 cleaning process. A dry thermal SiO_x film was then grown on the wafers in a quartz tube furnace at nearly atmospheric pressure with a 6:1 N_2-to-O_2 gas flow ratio. The thermal SiO_x thickness was varied by changing the oxidation time between 0.5 to 30 min for temperatures between 700–800 °C. The SiO_x thickness at each oxidation condition was determined by spectroscopic ellipsometry on single-side-polished *n*-Cz Si(100), 1–100 Ω·cm resistivity wafers that were loaded into the furnace at the same time as the saw-damage removed wafers.

Doped *a*-Si:H was then deposited on both sides of the oxidized *c*-Si wafers using a SiH_4/H_2 capacitively-coupled, radio-frequency plasma powered at 13.56 MHz. The flow rates of SiH_4 and H_2 were 2 and 100 standard cm^3/min (sccm), respectively. Additionally, for boron or phosphorous doping, 1 sccm of B_2H_6 (2.6% in H_2) or PH_3 (3% in H_2) were introduced into the chamber. The *c*-Si wafer was placed on the grounded substrate holder at a temperature of 300–350° C with an input power to the plasma source of 8 W to grow a ~20 nm thick *a*-Si:H layer. The resulting samples were then annealed at 850 °C for 30 min in a quartz tube furnace under N_2 atmosphere to convert *a*-Si:H to a *poly*-Si layer via solid-phase crystallization. A hydrogen-induced passivation

step followed, which involved deposition of Al_2O_3 via atomic layer deposition using trimethylaluminium and H_2O as precursors at 200 °C followed by annealing in forming gas (1:9 H_2:N_2 mixture) at 400 °C for 20 min. Quasi-steady-state photoconductance decay measurements were performed using a Sinton lifetime instrument (WCT-120) to extract the $i\text{-}V_{oc}$ values [130] for symmetric test structures on saw-damage removed wafer, similar to those shown in the inset of Fig. 2.1. Dopant depth profiles through the *poly*-Si layer into the *c*-Si wafer were measured on single-side-polished samples via secondary ion mass spectrometry (SIMS) using 1.5 keV ion bombardment energy from an oxygen source.

On the symmetric *poly*-Si/SiO_x/*c*-Si/SiO_x/*poly*-Si structures on the saw-damage removed wafers, using suitable shadow masks ~1 μm thick Al was deposited via electron-beam (*e*-beam) evaporation in a tool with a base pressure of ~10^{-7} Torr. Aluminum was deposited either as a 3×2 cm^2 pad to determine metal-induced degradation, or as rectangular or circular pads that were much smaller in size, for resistivity measurements. Post-metallization, the *n*-type contact samples were annealed at 400 °C in forming gas for 5 min, since previous experiments [70] show that it results in lower metallization-induced degradation of the contact. However, the *p*-type contact did not require a post-metallization anneal. Metallization-induced degradation was determined using photoluminescence (PL) imaging, which measures the intensity from radiative carrier recombination in the sample under steady-state conditions at a fixed illumination intensity and wavelength [131]. The *poly*-Si layer sheet resistivity, and the Al to *poly*-Si contact resistivity was determined using the smaller rectangular Al pads with varying spacing using the transmission line method (TLM) [132]. The structure with the TLM pattern was then subjected to reactive ion etching using SF_6 with the Al pads on the front as etching masks. After etching, the *poly*-Si and SiO_x layers were completely removed in the unmasked regions along with a few microns of the

underlying *c*-Si. The opposite un-metallized side of the *c*-Si wafer was also etched to completely remove the *poly*-Si and SiO_x layers. The resulting structures were utilized to determine the through-contact resistivity for the n^+-n high-low junction by TLM analysis, and the diode resistivity at 0.59 V of the p^+-n diode from its current-voltage (J-V) curve.

2.4. Results and Discussion

Below we discuss the effect of SiO_x thickness on passivation, conduction through SiO_x, and metallization induced degradation of the contact.

2.4.1. Effect of SiO_x thickness on *c*-Si surface passivation

Figure 2.1 shows the effect of SiO_x thickness on the i-V_{oc} of symmetric *n*- and *p*-type passivated contact test structures shown in the inset. Contacts with a thermally grown SiO_x show an i-V_{oc} that is at least 50 mV higher than the i-V_{oc} obtained for the RCA SiO_x with a very similar thickness, implying that the SiO_x growth method affects *c*-Si surface passivation. Also, there is a clear trend in Fig. 2.1, which shows that for both *n*- and *p*-type contacts, the i-V_{oc} first increases, reaches a maximum of ~739 and ~700 mV for *n*- and *p*-type contacts, respectively, at ~1.5 nm SiO_x thickness, and then decreases with further increase in SiO_x thickness. While the lower i-V_{oc} for contacts with SiO_x <1.4 nm can be attributed to poorer chemical passivation of dangling bonds on the *c*-Si surface, the decrease in i-V_{oc} for contacts with SiO_x >1.6 nm is quite surprising since a thicker SiO_x layer should result in improved passivation of the *c*-Si wafer surface [133]. The reason for inferior passivation quality for contacts with SiO_x >1.6 nm is attributed to lesser field-effect passivation, which is discussed below.

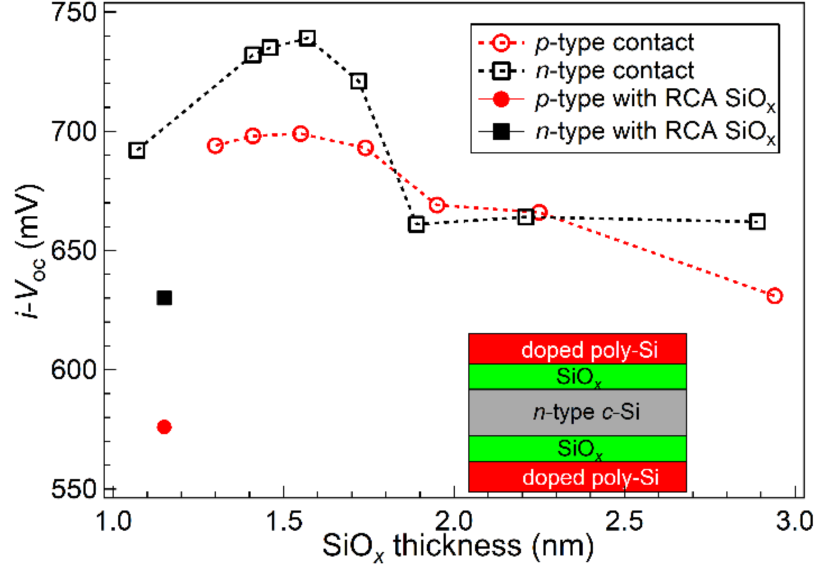

Figure 2.1 Effect of thermally grown SiO_x thickness on the i-V_{oc} of symmetric n- (□) and p-type (○) passivated contact test structures shown in the inset. The i-V_{oc} for n- (■) and p-type (●) passivated contacts with ~1.15 nm thick RCA SiO_x is shown for comparison. The dashed lines are a guide to the eye.

Figure 2.2 shows the Auger corrected inverse effective lifetime, $1/\tau_{eff} - 1/\tau_{Auger}$, versus minority carrier concentration, Δn, curves evaluated from the Sinton lifetime instrument under high injection condition. These measurements have been shown for n^+ *poly*-Si/SiO_x/n-type c-Si symmetric contacts for two different SiO_x thicknesses, 1.46 and 2.21 nm. From Eq. 1.12, the dependence of effective lifetime (τ_{eff}) on Δn under high injection condition for the symmetric test structure can be written as shown in Eq. 2.1

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Auger}} = \frac{1}{\tau_{bulk}} + \frac{2 \cdot J_o(N_{dop} + \Delta n)}{q n_i^2 W}\ , \qquad (2.1)$$

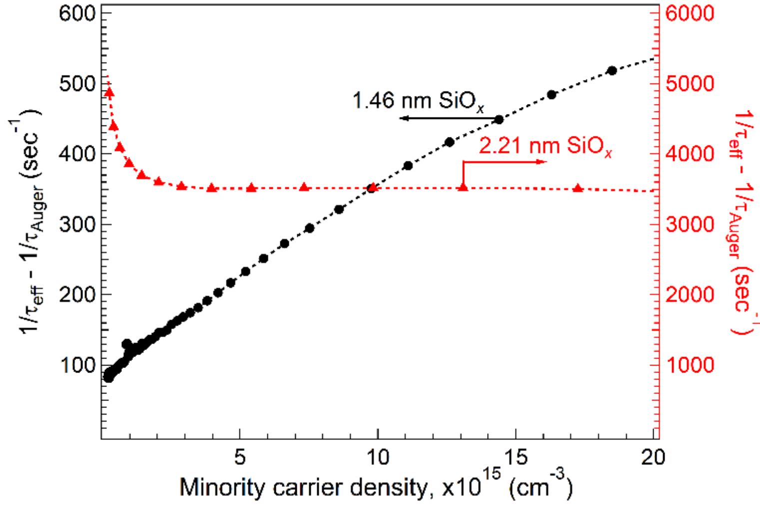

Figure 2.2 The Auger corrected inverse effective lifetime versus minority carrier concentration plot for the n^+ *poly*-Si/SiO_x/*n*-type *c*-Si symmetric contact with SiO_x thickness of 1.46 nm (●) (left axis) and 2.21 nm (▲) (right axis). The dashed lines are a guide to the eye.

where τ_{bulk} is the bulk carrier lifetime in the *c*-Si substrate, W is the sample thickness, n_i is the intrinsic carrier concentration, N_{dop} is the doping concentration, q is the unit charge of an electron, and J_o is the emitter saturation current density [106]. Physically, J_o is related to the photogenerated carrier recombination associated with either a *p-n* or a high-low junction. Figure 2.2 shows that for the contact with 1.46 nm SiO_x, the Auger corrected inverse effective lifetime increases linearly with the minority carrier concentration. The slope of this curve results in a low J_o value of 2.86 *f*A/cm^2, at $\Delta n = 5\times10^{15}$ cm^{-3}, which indicates excellent surface passivation of the wafer, and is consistent with the high i-V_{oc} of 735 mV (see Fig. 2.1). In contrast, the flatness of the Auger corrected inverse effective lifetime (see Fig. 2.2) for the contact with the 2.21 nm thick SiO_x, resulting in 662 mV i-V_{oc} (see Fig. 2.1), shows that the Auger corrected inverse lifetime is almost independent of Δn. Mathematically, such a relationship can be obtained if τ_{bulk} is very low such that the first term on the right-hand side in Eq. 2.1 dominates over the J_o term. However, we have confirmed that the different oxidation treatments do not degrade the bulk *c*-Si lifetime: this was

verified by etching the symmetric test structures shown in the inset of Fig. 2.1 in KOH solution to remove the *poly*-Si and SiO_x layers, and a few microns of *c*-Si surface. The samples were then RCA-cleaned, passivated with Al_2O_3 and subjected to forming gas anneal. The i-V_{oc} on all the resulting structures was between 720–730 mV indicating high bulk lifetime in *c*-Si. The lack of dependence of the Auger corrected inverse effective lifetime on the minority carrier concentration may also suggest that $J_o \approx 0$. Therefore, Eq. 2.1 may no longer be valid for the 2.21 nm thick SiO_x contact likely because the SiO_x is so thick that the recombination of the photo-generated carriers is not governed by the high-low junction expected to form between the n^+ *poly*-Si layer and *n*-type *c*-Si wafer. The carrier recombination instead may be governed by the SiO_x passivating layer. Equation 1.12 can then be modified as

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Auger}} = \frac{1}{\tau_{bulk}} + \frac{2 \cdot S}{W} , \tag{2.2}$$

where S is the surface recombination velocity. Thus, this indicates a change in the nature of the passivated contact when the SiO_x thickness changes from 1.46 to 2.21 nm.

Figure 2.3, similar to Fig. 2.2, shows the Auger corrected inverse effective lifetime versus minority carrier concentration curves for p^+ *poly*-Si/SiO_x/*n*-type *c*-Si symmetric contacts for three different SiO_x thicknesses, 1.4, 2.2, and 2.9 nm. It is evident in Fig. 2.3 that the plot for the contact with 1.4 nm SiO_x is increasing linearly, indicating the formation of an emitter. However, as SiO_x thickness increases the plots are less linear. For the contact with 2.9 nm SiO_x it is significantly non-linear with increasing Δn, indicating that the contact is no longer an emitter. Additionally, unlike for the *n*-type contact with 2.21 nm SiO_x shown in Fig 2.2, the Auger corrected inverse effective lifetime for the *p*-type contact with 2.9 nm SiO_x (see Fig. 2.3) shows some dependence on the minority carrier concentration. The likely reason for the above observations is due to the

reduced dopant diffusion from the *poly*-Si into the *c*-Si wafer due to a thicker SiO_x layer and is discussed below.

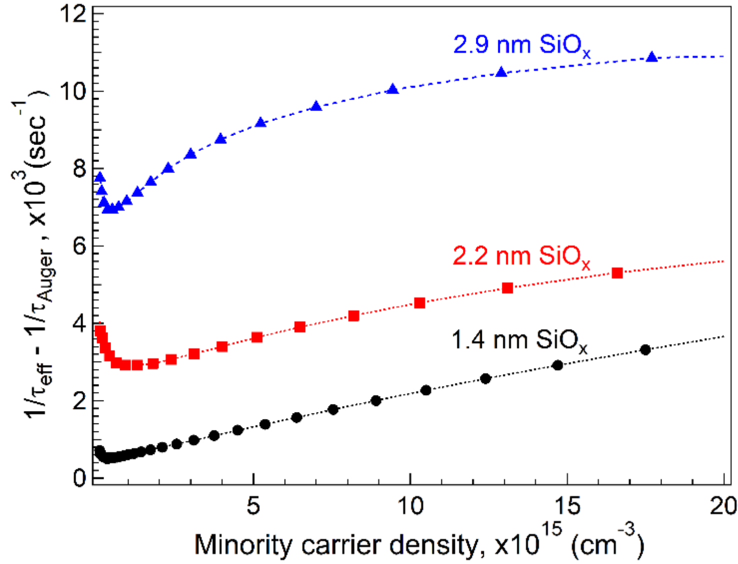

Figure 2.3 The Auger corrected inverse effective lifetime versus minority carrier concentration plot for the p^+ *poly*-Si/SiO_x/*n*-type *c*-Si symmetric contact with SiO_x thickness of 1.4 (●), 2.2 (■) and 2.9 (▲) nm. The dashed lines are a guide to the eye.

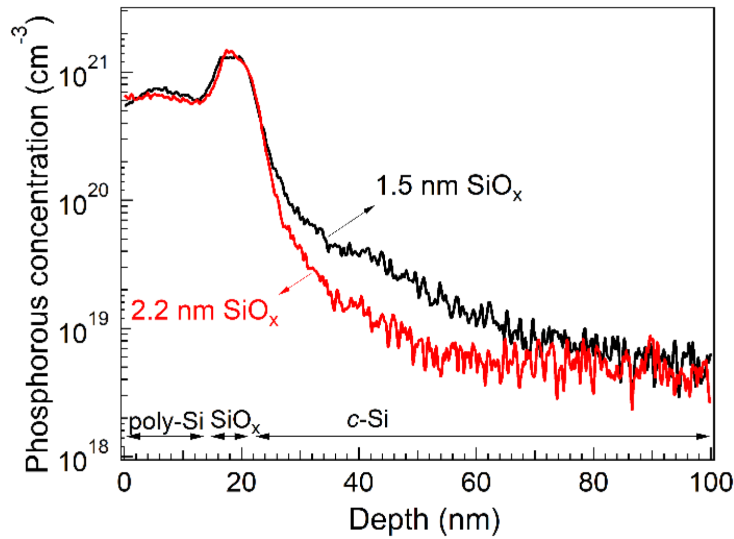

Figure 2.4 SIMS depth profile of phosphorous in the n^+ *poly*-Si/SiO_x/*n*-type *c*-Si contact with 1.5 (black) and 2.2 nm (red) thick SiO_x.

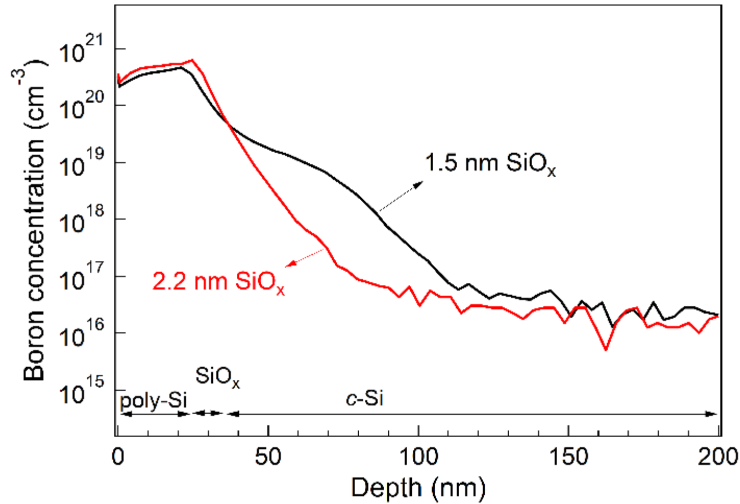

Figure 2.5 SIMS depth profile of boron in the p^+ *poly*-Si/SiO_x/*n*-type *c*-Si contact with 1.5 (black) and 2.2 (red) nm thick SiO_x.

Figures 2.4 and 2.5 show the phosphorous and boron depth profiles, respectively, within the *poly*-Si/SiO_x/*c*-Si stacked layers measured using SIMS. The phosphorous profiles were measured via time-of-flight SIMS, while the boron profiles via dynamic SIMS. The profiles have been plotted till the depth where the phosphorous and boron concentrations reach SIMS detection limits. The depth profiles are shown for contacts with two different SiO_x thicknesses of 1.5 and 2.2 nm. Regardless of SiO_x thickness, the dopant concentration is very similar in the *poly*-Si film and the SiO_x layer. However, the profiles within the *c*-Si region, directly underneath the SiO_x layer are significantly different, with the dopants diffusing deeper into the wafer, up to ~80 nm, for the contact with the thinner, 1.5 nm, SiO_x than for the contact with the marginally thicker, 2.2 nm SiO_x. Dopant diffusion from the *poly*-Si through SiO_x into the *c*-Si wafer has been previously observed for similar passivated contacts, and likely occurs during the high temperature annealing step, 850 °C for this study, which is essential to obtain the high i-V_{oc} values [70, 95, 116]. As a result of this dopant diffusion, the *p*-*n* and the high-low junction depletion regions are not formed between the edge of the doped *poly*-Si film and the *c*-Si wafer, but instead lie completely within the *c*-Si

wafer forming a diffused junction. Yang et al. [116] created similar passivated contact structures using ion implantation. In those experiments, the authors varied the dopant depth profiles into *c*-Si using ion-implantation of intrinsic *a*-Si, and concluded that both very shallow and very deep diffusion profiles result in poorer passivation compared to an intermediate dopant depth.

Relating the SIMS profiles in Figs. 2.4 and 2.5 to the Auger corrected inverse effective lifetime plots in Figs. 2.2 and 2.3 for the contact with the >2.2 nm thick SiO_x layer, we can infer that reducing the extent of dopant diffusion into the wafer, causes deviation of the contact properties from the ideal J_o behavior. This effect is quite significant for the n^+ *poly*-Si/2.21 nm SiO_x/*n*-type *c*-Si contact, as shown by the lack of dependence of Auger corrected inverse effective lifetime on Δn in Fig. 2.2. It is less prominent for the p^+ *poly*-Si/2.9 nm SiO_x/*n*-type *c*-Si contact, since it shows some dependence on Δn as shown in Fig. 2.3. This is most likely because the energy barrier for carriers to cross the junction is significantly less for a high-low junction due to a smaller band offset than for a *p*-*n* junction. Thus, the deviation of the contact properties from the ideal J_o behavior (see Figs. 2.2 and 2.3) can be inferred as a reduction in the net electric field experienced by the carriers near the *c*-Si surface, i.e., lesser field-effect passivation, and hence, lower i-V_{oc}. Another possible reason for the drop in i-V_{oc} with increasing SiO_x thickness can be due increased voltage drop across the SiO_x layer. However, the voltage drop across the SiO_x layer, calculated using PC1D simulations based on the measured dopant profiles, is small and it cannot account for the i-V_{oc} versus SiO_x thickness trend shown in Fig. 2.1. Hence, the likely cause for the lower i-V_{oc} for contacts with >1.6 nm SiO_x layer (see Fig. 2.1) is due the reduction in the extent of field-effect passivation. On the other hand, the lower i-V_{oc} for contacts with SiO_x thickness <1.4 nm can be attributed to poorer chemical passivation of dangling bonds on the *c*-Si surface [133]. To summarize, there is a balance between the extent of chemical passivation provided by the SiO_x

layer, which increases as SiO_x thickness increases, and the extent of field-effect passivation provided due to dopant diffusion through the SiO_x layer into the *c*-Si wafer, which reduces as SiO_x thickness increases.

2.4.2. Effect of SiO_x thickness on contact transport properties

Along with excellent passivation of the wafer to generate a high V_{oc}, passivated contacts should also allow for transport of the photogenerated carriers to ensure a high fill-factor and, hence, a high cell efficiency. Figure 2.6 shows the resistivity through the *poly*-Si/SiO_x/*n*-type *c*-Si stack for *n*- and *p*-type contacts with different SiO_x thickness for test structures shown in the inset. For the *n*-type contacts, the contact resistivity was evaluated with the TLM [132] approach, and shows that for contacts with SiO_x thickness <1.6 nm, the contact resistivity is low, and ~20 $m\Omega\cdot cm^2$ irrespective of SiO_x thickness. However, for these *n*-type contacts, a slight increase in the SiO_x thickness to 1.9 nm significantly increases the contact resistivity by 5 orders of magnitude, and this trend continues as SiO_x thickness is increased further. Such a significant rise in contact resistivity is consistent with poorer tunneling transport through the SiO_x layer. A similar analysis using the TLM approach is not possible for the p^+ *poly*-Si/SiO_x/*n*-type *c*-Si contact since it forms a *p-n* diode with the *n*-type *c*-Si wafer. However, when we measured the *J-V* curves across the *p-n* diodes for different SiO_x thicknesses using test structures as shown in inset of Fig. 2.6, we noticed that the forward current through the diodes with the thicker SiO_x layer was significantly lower than for the ones with thinner SiO_x layer. To quantify the extent of reduction in current, we calculated the inverse of the slope of the *J-V* curves at a fixed forward biasing voltage of 0.59 V and termed it as "diode resistivity," which is plotted on the right axis in Fig. 2.6. While this parameter does not represent true contact resistivity of the structure, it clearly demonstrates the effect of SiO_x thickness on transport through the *p-n* diode. Similar to the *n*-type contact (see Fig. 2.6), the diode

resistivity of the p-type contact is almost constant for <1.6 nm SiO_x thickness, and increases by several orders of magnitude when the SiO_x thickness increases from 1.6 nm to more than 1.7 nm. We also measured the metal to *poly*-Si contact resistivity via TLM for test structures shown in the inset of Fig. 2.7. Those values (not shown) were significantly lower than the contact resistivity measured through the metal/*poly*-Si/SiO_x/*c*-Si stack shown in Fig. 2.6. Hence, all the observed changes in contact resistivity shown in Fig. 2.6 can be attributed to the effect of changes in the SiO_x layer thickness. The similar behavior of the contact resistivity through the metal/*poly*-Si/SiO_x/*c*-Si stack for the n- and p-type contacts (see Fig. 2.6), confirms that the SiO_x layer no longer allows for efficient tunneling when the SiO_x thickness increases beyond 1.6 nm, making them impractical for use in a solar cell. It also verifies that unlike the POLO contacts from ISFH [75], our contacts with >1.6 nm SiO_x, after annealing at 850 °C, do not form sufficient pinholes within the SiO_x layer to allow for direct carrier transport between the *poly*-Si layer and the *c*-Si substrate [120]. However, we do expect pinholes in SiO_x if the contact is annealed at temperatures >950 °C, enabling carrier conduction.

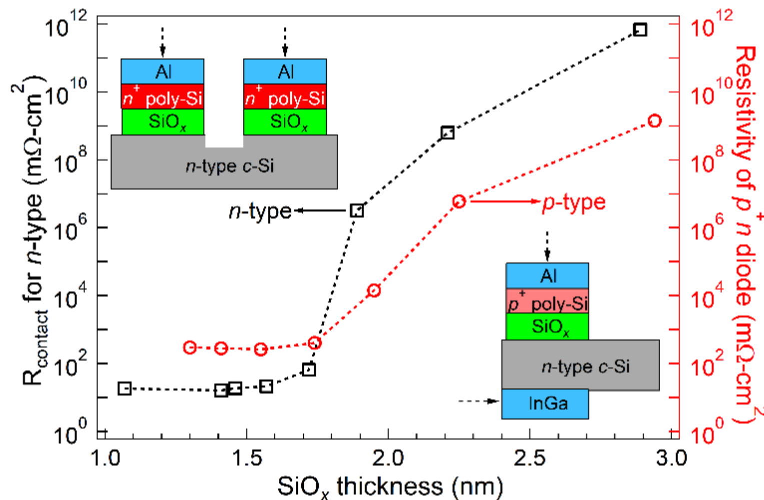

Figure 2.6 Effect of thermally grown tunneling SiO_x thickness on the through contact resistivity of n-type contact (□) (left axis), and p^+n diode resistivity of p-type contact (○) (right axis), on n-type c-Si wafer. Test structures for both are shown in the inset with the dotted arrows showing contact points for the measurement probes. The dashed lines are a guide to the eye.

Sheet resistivity (R_{sheet}) of the contact is another important parameter which affects lateral carrier conduction and, hence, cell efficiency. Figure 2.7 shows the R_{sheet} of the *n*- and *p*-type passivated contacts with different SiO_x thicknesses determined using TLM analysis for test structures shown in the inset. For contacts with SiO_x thickness <1.6 nm, the R_{sheet} is low and constant, ~90 and ~600 Ω/sq for *n*- and *p*-type contacts, respectively, but significantly increases with further increase in SiO_x thickness. It plateaus out at ~500 Ω/sq for the *n*-type contact with SiO_x thickness >1.9 nm and is >5500 Ω/sq for the *p*-type contact with similar SiO_x thickness. We suspect that the variation of the R_{sheet} of the *p*-type contact between 5500 and 9000 Ω/sq is likely due to inaccuracies with the TLM analysis. For the contacts with the thicker SiO_x layer, the R_{sheet} values are high and constant due to the current being restricted to the thin, ~20 nm, *poly*-Si sheet, since the SiO_x layer is non-conducting (see Fig. 2.6). However, the R_{sheet} values for the contacts with SiO_x <1.6 nm are much lower, since the SiO_x layer is conducting at these thicknesses (see Fig. 2.6). Thus, the effective conductive sheet in the TLM measurements for SiO_x <1.6 nm consists of both the *poly*-Si sheet, as well as the sheet formed underneath the SiO_x layer within the underlying *c*-Si substrate due to dopant diffusion: dopant diffusion from the *poly*-Si layer into the *c*-Si substrate through the SiO_x layer for SiO_x thickness <1.6 nm is apparent from the depth profiles shown in Figs. 2.4 and 2.5. This effectively creates two conductive sheets increasing the cross-sectional area for conduction, resulting in lower values of R_{sheet}. The effect of such a sheet, forming a diffused junction, on R_{sheet} of passivated contact is most accurately witnessed for the *p*-type contacts because the formation of the *p*-*n* diode with the *n*-type wafer restricts the current only to the *poly*-Si layer and the diffused sheet. In case of the *n*-type contact, a high-low junction is formed, which is a lower energy barrier for the charge carriers than a *p*-*n* junction. Therefore, for the *n*-type contact on a *n*-type *c*-Si wafer, the sheet resistivity of the wafer, which was ~280

Ω/sq, will also have some role to play in overall resistance measurement when the SiO_x layer is conducting. The significant reduction in R_{sheet} from ~5500 to ~600 Ω/sq for the *p*-type contacts (see Fig. 2.7) clearly shows that the diffused sheet is much more conductive than the *poly*-Si layer. This further signifies the importance of the formation of a diffused sheet underneath the SiO_x layer, within the *c*-Si. Not only is it beneficial for obtaining lower lateral conductivity, but also for passivation as discussed in Section 2.4.1. The lower R_{sheet} is quite important in cell architectures with *poly*-Si passivated contacts at both the front- and the back-side of the solar cell [95].

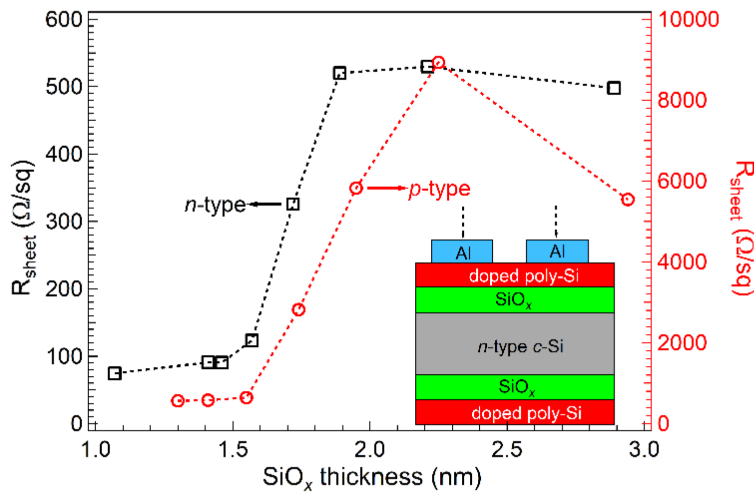

Figure 2.7 Effect of thermally grown tunneling SiO_x thickness on the sheet resistivity of *n*- (□) and *p*-type (○) passivated contacts for test structures shown in the inset. The dotted arrows in the inset show the contact points for the probes during the measurement. The dashed lines are a guide to the eye.

2.4.3. Effect of SiO_x thickness on metallization-induced degradation

Figure 2.8 shows the PL images for *n*- and *p*-type passivated contacts with different SiO_x thickness after metallization with Al. Darker regions in these PL images indicate lower carrier concentration, signifying greater metallization-induced damage. Note that the PL images of the samples were recorded for different shutter speeds of the CCD camera, and hence, the absolute

brightness of no two samples should be directly compared. Comparing the PL intensity of the metallized region on the sample, to the PL intensity prior to metallization, can be treated as a measure of the extent of metallization-induced degradation, and can be quantified as

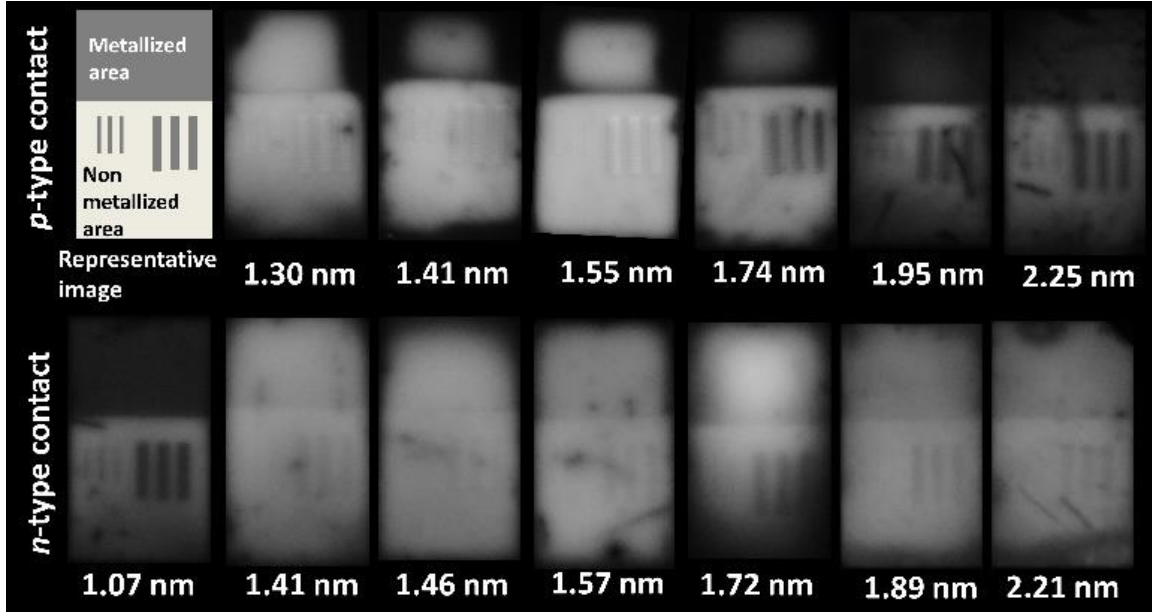

Figure 2.8 Photoluminescence images of *p*- and *n*-type passivated contacts with different SiO_x thicknesses after metallization with ~1 μm thick Al deposited via *e*-beam evaporation. Also shown (top left) is a representative image of the metallized area on the samples. The images are obtained for different collection times for the detector.

$$i\text{-}V_{oc,\ before\ metal} - i\text{-}V_{oc,\ after\ metal} = \frac{kT}{q} ln\left(\frac{I_{before\ metal}}{I_{after\ metal}}\right), \tag{2.3}$$

where, I is the measured PL intensity of the sample, T is the temperature of the sample, and k is the Boltzmann constant. Figure 2.9 shows the i-V_{oc} values for the *n*- and *p*-type contacts before and after metallization. The i-V_{oc} values before metallization have been replotted from Fig. 2.1, while those after-metallization have been calculated using Eq. 2.3. The PL images for the *p*-type samples (see Fig. 8) were recorded without a mirror underneath the sample, which results in some optical effects. However, these optical effects were accounted for in the i-V_{oc} calculation after

metallization. In Fig. 2.9, the i-V_{oc} for the n-type contact with the 1.07 nm thick SiO_x layer reduces by ~40 mV due to metallization, indicating significant metallization-induced degradation. However, the decrease in i-V_{oc} values for the n-type contacts with SiO_x thickness between 1.4–2.3 nm is between 7−15 mV indicating moderate metallization-induced degradation. In contrast, for the p-type contacts, the decrease in i-V_{oc} is between −30 to −45 mV, indicating significant metallization-induced degradation. The significant degradation for the n-type contact with 1.07 nm SiO_x is likely because such a thin SiO_x layer does not provide a sufficient barrier for creation of metal-induced defects in the c-Si substrate. Following that argument, one would expect the thicker SiO_x layer to insulate the underlying c-Si from metallization damage better, which does not seem to be the case based on the data shown in Fig. 2.9.

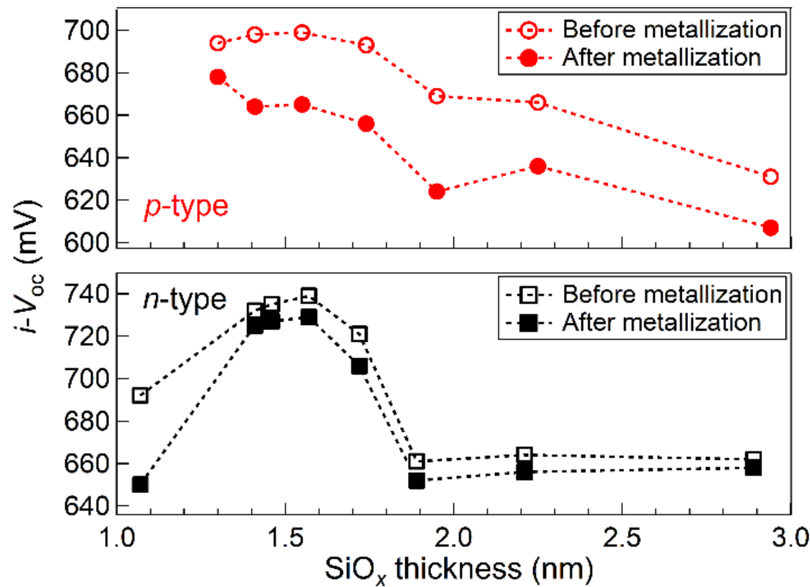

Figure 2.9 Effect of thermally grown tunneling SiO_x thickness on the i-V_{oc} of samples before metallization of n- (□) and p-type (○) contacts, and after metallization of n- (■) and p-type (●) contacts. The dashed lines are a guide to the eye.

We would like to point out that since V_{oc} is not an additive term, comparing the change in i-V_{oc} for samples which have very different pre-metallization i-V_{oc}, is not a completely accurate methodology for comparing the extent of metallization-induced degradation. For example, a change in i-V_{oc} due to metallization of −10 mV indicates much more significant metallization-induced damage on a sample with a pre-metallization i-V_{oc} of 660 mV, than on a sample with a pre-metallization i-V_{oc} of 740 mV. Instead, comparing the change in J_o due to metallization is much more accurate. We estimate J_o from the i-V_{oc} changes (Eq. 2.3) assuming diode ideality factor $n = 1$. For the *n*-type contact with the highest i-V_{oc}, the i-V_{oc} drops from 739 to 729 mV, while the J_o increases from 2.0 to 3.7 fA/cm^2 due to metallization-induced degradation. Similarly, for the *p*-type contact, the i-V_{oc} drops from 699 to 665 mV, while the J_o increases from 18.3 to 116 fA/cm^2. This clearly shows that our *p*-type contacts are much more sensitive to metallization-induced damage than our *n*-type contacts. Since pre-metallization J_o cannot be determined for both the *n*- and *p*-type contacts over the entire investigated SiO_x thickness range (see Fig. 2.2 and 2.3), determining change in J_o due to metallization becomes challenging. Hence, based on the above explanation, we can infer that the samples with thicker SiO_x likely show a higher extent of metallization-induced degradation. Since the *poly*-Si film on each sample was deposited and processed identically, it is quite interesting to observe that the extent of metallization induced degradation is affected by the buried SiO_x thickness. In order to understand the results shown in Fig. 2.8, we compared our results with studies on metallization of passivated emitter rear contact (PERC) solar cells [134]. For cells with diffused emitters such as the PERC cell, it has been shown that better passivation is obtained by lowering the surface dopant concentration, but for reducing metallization-induced degradation, the concentration of dopants right underneath the metal contacts needs to be high [106, 134]. However, the SIMS profiles in Fig. 2.4 and Fig. 2.5 show

that the surface concentration of dopants is very similar for contacts with different SiO_x thicknesses, and thus, metallization-induced degradation should be independent of SiO_x thickness. However, Al is known to have a detrimental effect on *c*-Si [135] and SiO_x [136], and hence, we hypothesize that the defect-sensitive, charge-separating depletion region is closer to the deposited Al for contacts with >1.8 nm SiO_x than for those with the <1.6 nm SiO_x, as the thicker SiO_x inhibits dopant diffusion from *poly*-Si into *c*-Si to a greater extent (see Fig. 2.4 and 2.5). This likely makes the contacts with the thicker SiO_x layer more susceptible to metallization-induced degradation.

2.5. Conclusions and Summary

We have studied the effect of the thickness of thermally-grown SiO_x on passivated contact performance for *c*-Si solar cells. For obtaining excellent passivation of the *c*-Si wafer while making it less susceptible to metallization-induced degradation, the SiO_x thickness within the passivated contact should be within 1.4–1.6 nm for a contact annealing temperature of 850 °C. We speculate that the lower limit is to ensure good chemical passivation of the *c*-Si surface dangling bonds by the SiO_x layer, while the upper limit is to provide excellent field-effect passivation achieved by diffusion of dopants from the *poly*-Si layer through the SiO_x into the *c*-Si wafer creating a diffused junction. Even within the tunneling regime, SiO_x thickness affects the extent of dopant diffusion which and has been verified by SIMS depth profiles for both boron- and phosphorous-doped contacts. This, in turn, influences the measured sheet resistivity of the contact. A marginal increase in the SiO_x thickness from 1.6 to 1.7 nm significantly increases the contact resistivity through the metal/*poly*-Si/SiO_x/*c*-Si stack, which indicates that SiO_x >1.7 nm has poor carrier tunneling properties. Finally, the extent of metallization-induced degradation of *poly*-Si/SiO_x contacts is worst for the thinnest SiO_x investigated (~1 nm), and interestingly is not completely mitigated even for a ~3 nm thick SiO_x. We expect our results to change when the contact annealing temperature

is increased to temperatures where pinholes in the SiO_x layer may form and is further discussed in the next chapter.

2.6. Acknowledgements

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CHAPTER 3

UNDERSTANDING THE CHARGE TRANSPORT MECHANISMS THROUGH ULTRATHIN SiO_x LAYERS IN PASSIVATED CONTACTS

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In the previous chapter we determined that the SiO_x thickness needs to be between 1.4–1.6 nm to obtain best passivation while still enabling carrier conduction through the SiO_x layer. However, *poly*-Si/SiO_x contacts consisting of a >2 nm thick SiO_x layer, with good passivation and conduction have been reported by Gan *et al*. [67], and Romer *et al*. [75]. However, these contacts were processed at a much higher annealing temperature of 1000–1050 °C, unlike the 850 °C annealing temperature we used in Chapter 2. The transformation of an insulating SiO_x layer to a conductive one, after annealing of a *poly*-Si/SiO_x/*c*-Si stack at higher temperatures is due to structural changes in the SiO_x layer. Specifically, the SiO_x layer can ball-up and allow direct contact between the *poly*-Si layer and the *c*-Si wafer [125, 126], allowing carrier conduction. However, in theory this should also result in deterioration of the passivation quality, due to loss of chemical passivation from the SiO_x layer [74], thus deteriorating device performance. In this

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chapter we map such conduction-enabling nonuniformities in the SiO_x layer using electron-beam induced current measurements, and investigate their nanostructure using area-specific transmission electron microscopy.

3.1. Abstract

We report on the microscopic structure of the SiO_x layer and the transport mechanism in polycrystalline Si (*poly*-Si) passivated contacts, which enable high-efficiency crystalline Si (*c*-Si) solar cells. Using electron-beam induced current (EBIC) measurements, we accurately map nanoscale conduction-enabling pinholes in 2.2 nm thick SiO_x layers in a *poly*-Si/SiO_x/*c*-Si stack. These conduction-enabling pinholes appear as bright spots in EBIC maps due to carrier transport and collection limitations introduced by the insulating 2.2 nm SiO_x layer. Performing high-resolution transmission electron microscopy at a bright spot identified with EBIC reveals that conduction pinholes in SiO_x can be regions of thin tunneling SiO_x rather than a geometric pinhole. Additionally, selectively etching the underlying *poly*-Si layer in contacts with 1.5 and 2.2 nm thick SiO_x layers using tetramethylammonium hydroxide results in pinhole-like etch features in both contacts. However, EBIC measurements for a contact with a thinner, 1.5 nm SiO_x layer do not reveal pinholes, which is consistent with uniform tunneling transport through the 1.5 nm SiO_x layer. Finally, we theoretically show that reducing the metal to *c*-Si contact size from microns, like in *p*-PERC, to tens of nanometers, like in *poly*-Si contacts, allows lowering of the unpassivated contact area by several orders of magnitude thus resulting in the excellent passivation, as has been demonstrated for these contacts.

3.2. Introduction

Solar is a prime candidate for meeting future world energy demands, and Si photovoltaics (PV) is the leading technology dominating the solar market. Processing and manufacturing optimization have made Si PV economically comparable to fossil-fuel-based energy sources. However, to utilize its full potential, and lower the net $/kWh cost of electricity, it is important to increase the cell efficiency. Efficiency improvements in monocrystalline silicon (*c*-Si) based solar cells have been achieved by transitioning from the traditional Al-back-surface field (20.3%) [137], to *p*-type passivated emitter rear contact (*p*-PERC) (25.0%),[137-139] to polycrystalline Si (*poly*-Si) contacts (26.1%) [68], to Si heterojunction cells (26.7%) [69]. These improvements are enabled by lowering or almost completely eliminating the fraction of the silicon surface that is directly in contact with the metal used for charge collection. Amongst these high-efficiency architectures *poly*-Si contacts are prime candidates for next-generation Si PV because their high thermal stability makes them compatible with current mainstream cell manufacturing processes like Ag-paste firing [56, 67, 75, 97, 115, 116, 133, 140]. However, the wide-scale industrial implementation of these structures has been limited due to high processing costs, and a lack of fundamental understanding from a manufacturing perspective.

The very low defect density at the SiO_x/*c*-Si interface is crucial to enable the ultrahigh efficiencies reported for these cells. Passivation with SiO_x has been previously utilized in both the Al-BSF and *p*-PERC cells [121, 122]. The *poly*-Si/SiO_x/*c*-Si structure has also been well studied in various Si based electronic devices such as bipolar junction transistors [73, 141]. The *poly*-Si/SiO_x contact structure was introduced to *c*-Si solar cells by Yablonovitch in the 1980's [56], followed by Gan in the 1990's [67]. However, only recently significant improvements to this structure were reported, which resulted in a 25.1% cell efficiency, a record in 2015 [142]. Since

then, interest in this topic has piqued but one of the main factors still not well understood is the carrier transport through the SiO_x layer [63, 65].

Based on the thickness of the SiO_x layer, *poly*-Si/SiO_x passivated contacts can be classified into two broad categories. The first category is described as tunneling contacts with SiO_x thickness ≤1.5 nm, incorporated into a *poly*-Si/SiO_x/*c*-Si stack, which is then annealed between 850–900 °C, and has resulted in 25.8% cell efficiency [61]. For these contacts, tunneling through the SiO_x layer is likely the dominant conduction mechanism [63, 117-119]. The second category, described as pinhole contacts in the literature, consist of an SiO_x layer with thickness >2 nm within the *poly*-Si/SiO_x/*c*-Si stack. These contact are annealed at significantly higher temperatures between 1000–1050 °C, and have resulted in 26.1% cell efficiency [68]. For these contacts the dominant conduction mechanism is proposed to be direct conduction between the *poly*-Si layer and the *c*-Si absorber through geometric pinholes in the SiO_x layer, which are formed due to the high temperature annealing step [65, 67]. Nanoscale pinhole formation via balling-up of SiO_x is governed by thermodynamics, and occurs so as to reduce the surface energy of the thin continuous SiO_x layer [125, 126]. The extent of balling-up depends on both SiO_x thickness and annealing temperature and a thicker SiO_x layer balls up at a higher temperature. Hence, both these parameters need to be taken into consideration while optimizing the *poly*-Si/SiO_x/*c*-Si contact performance for passivation and conduction. While evidence of localized conducting regions in an otherwise insulating SiO_x layer can be inferred by measuring conductivity through the SiO_x layer [75, 143], and via selective etching with a tetramethylammonium hydroxide (TMAH) solution [120], the actual observation of the pinhole structure through imaging techniques is challenging due to their small size, likely 10s of nm, and low surface density, ~10^5–10^9 cm^{-2} [71].

In this work, we aim to verify the existence of pinholes in both thick (>2 nm) and thin (<2 nm) SiO_x passivating contacts using electron-beam-induced current (EBIC) measurements that allows for the detection of conductive regions non-destructively while revealing their microscopic origin through high-resolution transmission electron microscopy (TEM). Our EBIC measurements support the hypothesis that uniform tunneling transport and locally enhanced conduction through thinner SiO_x regions are the dominant transport mechanisms in contacts with 1.5 and 2.2 nm SiO_x, respectively. Performing TEM at a region identified as potential pinhole with EBIC reveals this location to be a thinner SiO_x region facilitating tunneling transport instead of direct conduction between *poly*-Si and *c*-Si. To maintain consistency with the terminology previously used in the literature,[75] we will use the term "pinholes" to refer to features that allow for locally enhanced conduction through an otherwise non-conducting SiO_x layer: these features are not necessarily a geometric pinhole with the absence of a SiO_x layer in that region.

3.3. Experimental Details

Experimental details regarding fabrication of symmetric *poly*-Si/SiO_x contact, and device test structures are provided below.

3.3.1. Fabrication of *poly*-Si/SiO_x symmetric test structures

As-sawn, phosphorous-doped, *n*-type Czochralski (*n*-Cz) Si(100), 8 Ω·cm resistivity, ~190 µm thick wafers (Woongjin Co. Ltd, South Korea) were subjected to a KOH based etch for planarization and saw-damage removal. The wafers were then cleaned using standard wafer cleaning procedures of piranha, RCA-1 and RCA-2 [128, 129], followed by a treatment with 1% aqueous HF to remove the SiO_x formed as a result of the RCA-2 cleaning process. A dry thermal SiO_x film was then grown on the wafers in a quartz tube furnace at nearly atmospheric

pressure with a 6:1 N_2-to-O_2 gas flow ratio. The oxidation temperature and time were varied between 700–800 °C and 5–10 min to grown either a 1.5 or 2.2 (±0.05) nm thick dry thermal SiO_x layer on the cleaned wafers. The SiO_x thickness was determined by spectroscopic ellipsometry on reference polished wafers. Doped *a*-Si:H was then deposited on both sides of the oxidized *c*-Si wafers using a SiH_4/H_2 capacitively-coupled, radio-frequency plasma powered at 13.56 MHz. The flow rates of SiH_4 and H_2 were 2 and 100 standard cm^3/min (sccm), respectively. Additionally, for boron or phosphorous doping, 1 sccm of B_2H_6 (2.6% in H_2) or PH_3 (3% in H_2) were introduced into the chamber. The *c*-Si wafer was placed on the grounded substrate holder at a temperature of 300–350° C with an input power to the plasma source of 8 W to grow a ~50 nm thick *a*-Si:H layer. The resulting samples were then annealed between 750–1050 °C for 30 min in a quartz tube furnace under N_2 atmosphere to convert *a*-Si:H to a *poly*-Si layer via solid-phase crystallization. A hydrogen-induced passivation step followed, which involved deposition of Al_2O_3 via atomic layer deposition using trimethylaluminium and H_2O as precursors at 200 °C followed by annealing in forming gas (1:9 H_2:N_2 mixture) at 400 °C for 20 min. Quasi-steady-state photoconductance decay measurements were performed using a Sinton lifetime instrument (WCT-120) to extract the implied open circuit voltage (i-V_{oc}) values [130], for symmetric test structures on saw-damage removed wafer, similar to those shown in the inset of Fig. 3.1. The samples were treated with 1% aqueous HF, and using suitable shadow masks ~1 μm thick Al was deposited via electron-beam (*e*-beam) evaporation in a tool with a base pressure of ~10^{-7} Torr. Aluminum was deposited either as a 3×2 cm^2 pad to determine metal-induced degradation, or as rectangular or circular pads that were much smaller in size, for resistivity measurements. The *poly*-Si layer sheet resistivity, and the Al to *poly*-Si contact resistivity was determined using the smaller rectangular Al pads with varying spacing using the transmission line method (TLM) [132]. The structure with

the TLM pattern was then subjected to reactive ion etching using SF_6 with the Al pads on the front as etching masks. After etching, the *poly*-Si and SiO_x layers were completely removed in the unmasked regions along with a few microns of the underlying *c*-Si. The opposite un-metallized side of the *c*-Si wafer was also etched to completely remove the *poly*-Si and SiO_x layers. The resulting structures were utilized to determine the through-contact resistivity for the n^+-n high-low junction by TLM analysis.

3.3.2. Fabrication of bifacial cells with *poly*-Si/SiO_x contacts on front and rear sides

Double-side-polished, phosphorous-doped, *n*-type float zone (*n*-Fz) Si(100), 1–5 Ω·cm resistivity, ~280 µm thick wafers were cleaned using piranha, RCA-1 and RCA-2,[128] followed by treatment with 1% aqueous HF. Subsequently, either a 1.5 or 2.2 (±0.05) nm thick dry thermal SiO_x layer was grown on the cleaned wafers in a quartz tube furnace with a 6:1 N_2-to-O_2 gas flow ratio. The SiO_x thickness was determined by spectroscopic ellipsometry. Doped or intrinsic (*i*) hydrogenated amorphous Si (*a*-Si:H) was then deposited on both sides of the oxidized wafers using plasma enhanced chemical vapor deposition (PECVD), as described above. For the contacts with 1.5 nm thick SiO_x layer, the n^+-*a*-Si:H/SiO_x/*c*-Si/SiO_x/p^+-*a*-Si:H structures were annealed at 850 °C for 30 min in a quartz tube furnace under N_2 atmosphere. For the pinhole contacts with 2.2 nm thick SiO_x layer, first the *i*-*a*-Si:H/SiO_x/*c*-Si/SiO_x/*i*-*a*-Si:H structures were annealed at 1025 °C for 30 min. Following treatment with 1% aqueous HF, doped *a*-Si:H layers were deposited to form n^+-*a*-Si:H/*i*-*poly*-Si/SiO_x/*c*-Si/SiO_x/*i*-*poly*-Si/p^+-*a*-Si:H structures and the samples annealed at 850 °C for 30 min resulting in n^+ *poly*-Si/SiO_x/*c*-Si/SiO_x/p^+ *poly*-Si structures. We performed a two-step annealing process for the 2.2 nm SiO_x contact to ensure that the extent of conduction pinhole formation in SiO_x was not influenced by the different dopant types, i.e., phosphorous and boron. Our preliminary experiments showed that the boron-doped contacts caused SiO_x balling at

a lower temperature than phosphorous doped contacts, likely due to significant interaction of boron with the SiO_x layer [76, 77]. Since, this was not an issue for 1.5 nm SiO_x contacts they were annealed in a single step. After this, the structures where coated with Al_2O_3 grown by atomic layer deposition, followed by annealing in forming gas to drive in excess hydrogen for passivation [39, 70]. A few of these samples were metallized with Al via thermal evaporation through shadow masks to create 4 cm^2 bifacial test cells. No post metallization annealing was performed. The cell performance was quantified using current-voltage (*J*-*V*) measurements.

3.4. Results and Discussion

Experimental results are provided and discussed below.

3.4.1. Interdependence of SiO_x thickness and contact annealing temperature on passivation and SiO_x conductivity

Figure 3.1 shows the effect of contact annealing temperature on the i-V_{oc} of symmetric *p*-type passivated contact test structures with either a 1.5 or 2.2 nm thick SiO_x layer. A schematic of the test structure is shown in the inset. Contacts with both SiO_x thickness show a similar trend with the i-V_{oc} first increasing with annealing temperature, reaching a maximum, and then decreasing with further increase in SiO_x thickness. Also, the curve for the contact with the thicker, 2.2 nm SiO_x layer contact appears shifted to the right, a higher temperature, as compared to the curve for the thinner, 1.5 nm SiO_x layer contact The initial increase in i-V_{oc} is due to improved field-effect passivation from increasing dopant diffusion from the *poly*-Si layer into the *c*-Si wafer [113]. The drop in i-V_{oc} at higher annealing temperatures is due to significant break-up of the SiO_x layer, leading to a loss of chemical passivation [74, 125, 126]. It must be noted that in highest i-V_{oc} is obtained at 850 and 950 °C for the contacts with the 1.5 and 2.2 nm thick SiO_x layers,

respectively. We related this to a thicker SiO_x layer mitigating dopant diffusion [113], and also breaking-up at a higher temperature [125, 126].

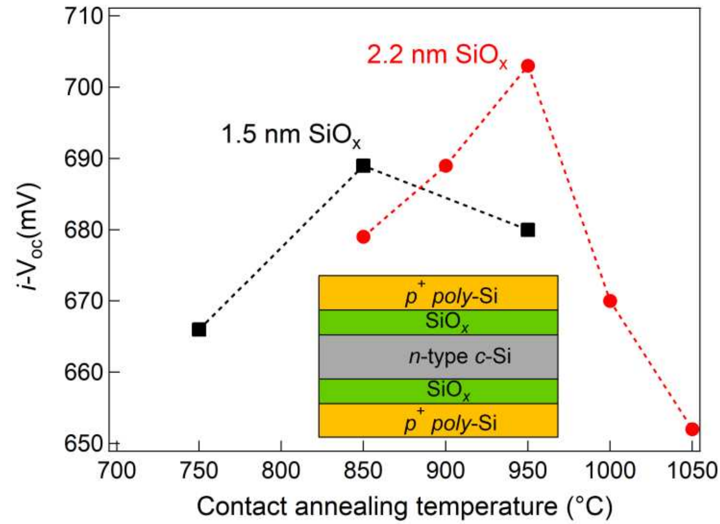

Figure 3.1 Effect of contact annealing temperature on i-V_{oc} of symmetric p^+ *poly*-Si/SiO_x contact test structures with 1.5 (■) and 2.2 nm (●) thick SiO_x layer. Schematic of test structure is shown in the inset.

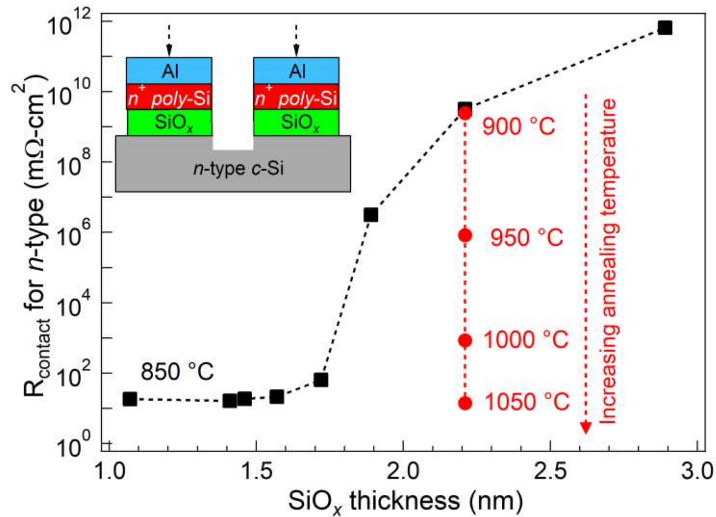

Figure 3.2 Change in through SiO_x contact resistivity of n^+ *poly*-Si/SiO_x/*n*-Si contact test structures: with different SiO_x thickness contacts annealed to 850 °C (■); and with 2.2 nm thick SiO_x layer contacts annealed to different temperatures (●). Schematic of test structure is shown in the inset. The curve is black is reproduced from Ref. [113].

Figure 3.2 shows how the contact resistivity of a n^+ *poly*-Si/SiO_x/*n*-Si stack changes with SiO_x thickness and contact annealing temperature. The curve is black is reproduced from Fig. 2.6 and shows that when the *poly*-Si/SiO_x contact annealing temperature is limited to 850 °C, the contact resistivity significantly increases with increasing SiO_x thickness for >1.7 nm thick SiO_x layers. The contact resistivity for a contact with 2.2 nm thick SiO_x layer is ~10^{10} mΩ·cm^2 at an annealing temperature of 850 °C. However, the curve is red shows that with increasing the contact annealing temperature, the contact resistivity also reduces. Values as low as ~10 mΩ·cm^2 are obtained for contact annealing temperature of 1050 °C. Such a transition of an insulating SiO_x layer to a conductive one due to higher annealing temperature is speculated to occur due to the break-up of the SiO_x layer: the break-up results in direct conduction between the *poly*-Si layer and the *c*-Si wafer [67, 71, 125, 126]. This chapter will focus on investigation of the SiO_x break-up phenomena.

Using the insights gained from the above results and some more processing optimization, bifacial solar cells with 1.5 and 2.2 nm SiO_x layers were fabricated on double-side polished Si(100) wafers. The fabrication details have been described in the experimental section 3.3.2. The open-circuit voltage (V_{oc}) for the test cells with the 1.5 and 2.2 nm SiO_x layer were 705±2 and 695±2 mV, respectively, which indicates that both the contacts are well passivating. The corresponding fill-factors for the two cells were 75.1±0.5% (1.5 nm SiO_x) and 66.3±0.5% (2.2 nm SiO_x), which translates to a series resistance of 0.86 and 1.46 Ω, respectively [144]. This indicates that the SiO_x layer in both the contacts is sufficiently conductive. Thus, we can infer that both the cells have passivated contacts suitable for the follow-up measurements. To ensure unambiguous interpretation of TMAH etching and EBIC experiments, the bifacial test cells were fabricated with polished Si wafers without a transparent conducting oxide or anti-reflection layer. Using very

similar processing conditions, we have demonstrated ~21.4% efficient *c*-Si cells with *poly*-Si contacts on the front and the back [145].

3.4.2. Etching of *poly*-Si/SiO_x contacts with TMAH to determine pinholes in the SiO_x layer

To determine the presence of discontinuities in the SiO_x layer, i.e. pinholes, we etched *poly*-Si/SiO_x contacts with TMAH solution. TMAH is very selective in removing Si over SiO_2 [146]. For example, using a 15% TMAH solution at 75 °C the etch times for our 50 nm thick n^+ *poly*-Si layer and 1.5 nm thermal SiO_x layer are ~10 and ~300 s, respectively. Hence, by performing an over-etch of the n^+ *poly*-Si, in our case for 3 min, a sufficiently large etch pit can be created in the underlying *c*-Si wafer through pinholes that may be present in the SiO_x layer: these etch pits can then be visualized by SEM. However, a similar experiment is difficult to perform for p^+ *poly*-Si contacts due to comparable etch times for a 50 nm thick boron-doped *poly*-Si film and a 1.5 nm thermal SiO_x layer. Figure 3.3 shows the SEM images of the wafer surface with different initial film stacks after etching with TMAH solution. Our control sample (see Fig. 3.3a) is a wafer with 2.2 nm thick thermal SiO_x layer, which after etching does not show any surface features. A particle on the surface was intentionally captured to ensure that we were indeed focused on the polished *c*-Si surface. However, when a n^+ *poly*-Si layer with 2.2 nm SiO_x is etched (see Fig. 3.3b), we can observe numerous inverted pyramid-like features, highlighted by dotted circles. These are most likely formed due to TMAH-induced etching in the presence of local non-uniformities in the SiO_x layer that originate due to annealing of the 2.2 nm SiO_x contact at 1025 °C. Figure 3.3c shows the SEM image of an etched wafer surface with a 1.5 nm thick thermal SiO_x layer. Surprisingly, even though this sample was without a *poly*-Si layer, we still notice the presence of numerous inverted pyramid-like features, which indicate the existence of localized non-uniformities in SiO_x. These are observed irrespective of the etching conditions, 3–15 min in TMAH at 60–75 °C. Since

it is known that SiO_x grows uniformly and almost stress-free on a flat *c*-Si surface [147], we speculate that the etch pits observed in Fig. 3.3d (n^+ *poly*-Si with 1.5 nm SiO_x contact) are simply artifacts created by non-uniform TMAH etching of the thin SiO_x layer. Hence, the formation of etch pits after TMAH etching in a n^+ *poly*-Si contact with 1.5 nm SiO_x is inconclusive. Therefore, we further studied these contacts using EBIC measurements, which is non-destructive, and is very sensitive to electronic effects.

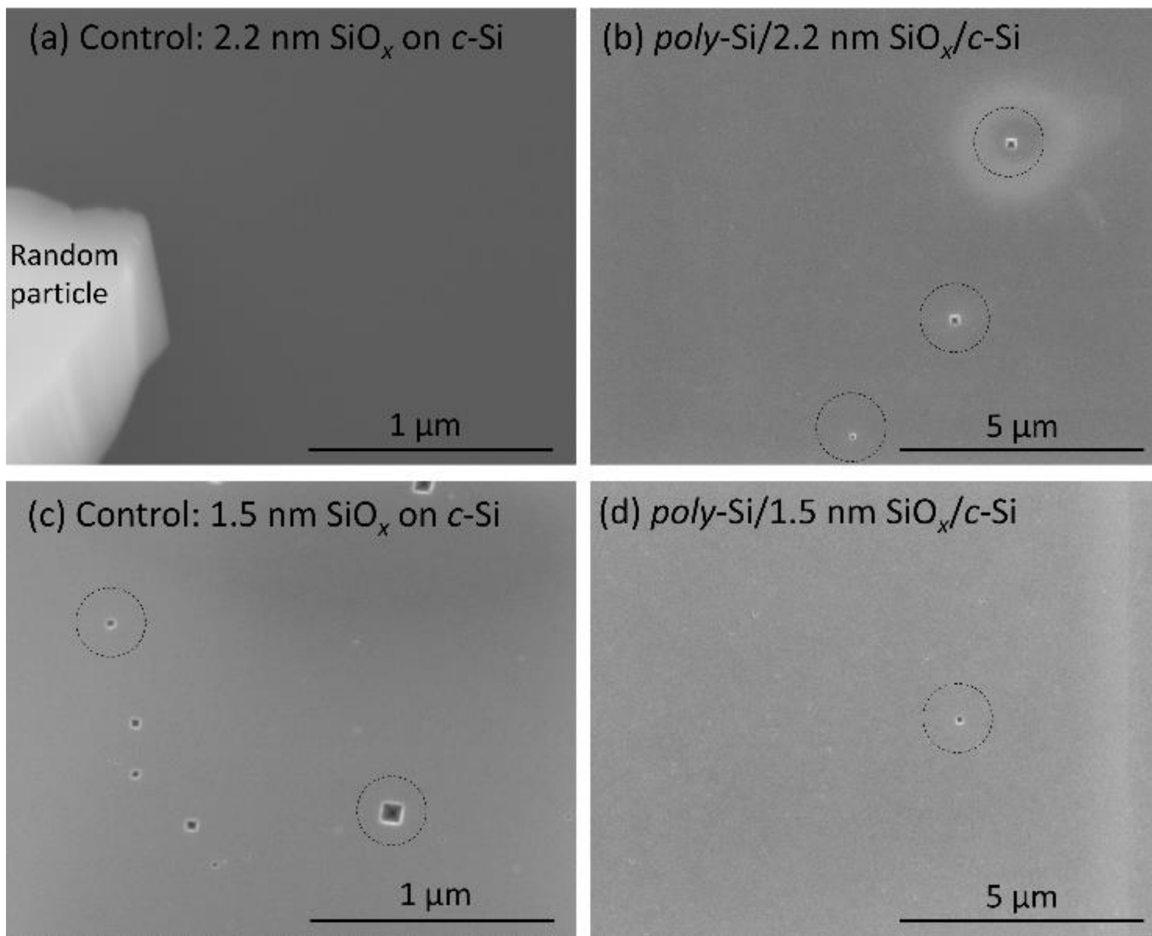

Figure 3.3 SEM images of polished *c*-Si surface after etching different test structures in 15% TMAH solution at 75 °C for 3 min. The images correspond to (a) *c*-Si wafer with 2.2 nm thick SiO_x layer; (b) n^+ *poly*-Si contact with 2.2 nm thick SiO_x layer that was annealed at 1025 °C, (c) *c*-Si wafer with 1.5 nm thick SiO_x layer; and (d) n^+ *poly*-Si contact with 1.5 nm thick SiO_x layer that was annealed at 850 °C.

3.4.3. EBIC and TEM of *poly*-Si/SiO$_x$ contacts to visualize pinholes in the SiO$_x$ layer

The intensity in EBIC images results from the separation of electron-hole pairs generated by the electron-beam within a SEM and subsequent collection of these excited carriers, which results in a current [111, 112]. The generated current is dependent on the interaction of charge carriers with defects or inhomogeneities in the device as well as the carrier collection probability. Thus, EBIC measurements can result in maps which have either no features due to spatially uniform carrier collection, darker features due to carrier recombination in regions with a high defect density, or brighter features due to enhanced local carrier collection. EBIC measurements were performed on the bifacial cells, at un-metallized regions, using a field-emission SEM (JEOL JSM-7600) with images acquired using an electron-beam accelerating voltage of 5 kV and a beam current of ~1 nA. Figures 3.4a and 3.4b show the EBIC images of the metallized test cells measured on the p^+ *poly*-Si side with the 2.2 and 1.5 nm SiO$_x$ contact, respectively. The density of bright spots in the EBIC images for n^+ *poly*-Si side of the same test cells was similar to p^+ *poly*-Si side, and therefore not discussed. We can clearly notice that while the EBIC map for the 2.2 nm SiO$_x$ contact shows numerous bright spots, the 1.5 nm SiO$_x$ contact does not show any features. We attribute the bright spots in Fig. 3.4a to enhanced conduction through the 2.2 nm SiO$_x$ layer. Figures 3.4c and 3.4d show the schematic of the proposed carrier recombination and current pathways for the 2.2 and 1.5 nm SiO$_x$ contacts, respectively. If the recombination at a pinhole in a conducting SiO$_x$ layer is significant then a pinhole should appear as a dark spot in EBIC. However, for the case of a contact where the SiO$_x$ layer is non-conducting, carrier collection probability is much higher in proximity to a pinhole, which may therefore result in a higher EBIC signal near the pinhole location [111, 112]. As shown schematically in Fig. 3.4c, there are two components to the locally enhanced EBIC signal in Fig. 3.4a: first, a depletion region forms underneath a pinhole due

to higher dopant diffusion from the p^+ *poly*-Si into the *n*-type *c*-Si wafer directly through the SiO_x pinhole compared to the 2.2 nm thick continuous SiO_x layer. The presence of a depletion region improves carrier separation and is further discussed later [113]. Second, there is reduced charge collection far from the pinholes due to lateral diffusion requirements introduced by the non-conductive nature of the 2.2 nm thick continuous SiO_x layer. Any holes excited from the electron-beam away from the pinhole need to first diffuse to a pinhole location before they can be collected by the p^+ *poly*-Si layer. These holes can undergo recombination before they reach the pinhole thus reducing the measured current. While the quantification of these and/or other effects is difficult, nonetheless, we can infer from the bright spots in the EBIC image in Fig. 3.4a that local pinhole-like transport dominates for the contacts with the ~2.2 nm thick SiO_x layer. Further analysis of the image in Fig. 3.4a shows that the intensity of the bright spots varies: this suggest that the size of the pinhole-like features varies or the carrier collection probability varies due to differences in the structures of these pinhole-like defects. We will discuss this in more detail later.

The lack of contrast in the EBIC image for the contact with the 1.5 nm SiO_x layer (Fig. 3.4b) means that the carrier collection efficiency is uniform over the sample surface. This is possible only when the resistance to carrier transport through a SiO_x layer and pinholes (if they exist) is comparable during the EBIC measurement. Thus, we can conclude that tunneling through the 1.5 nm SiO_x layer is the likely dominant carrier transport mechanism for the 1.5 nm SiO_x contact. It must be noted that the absence of any bright or dark spots compared to the background in the EBIC image for these contacts cannot be interpreted as absence of pinhole-like features. It is possible that the diffused junction underneath the SiO_x layer, which is formed due to diffusion of dopants during the 850 °C anneal [113], separates the carriers very efficiently. Hence,

recombination at pinhole-like features, which would otherwise lead to dark spots, might not influence EBIC intensity, i.e., field-effect passivation dominates over chemical passivation [32].

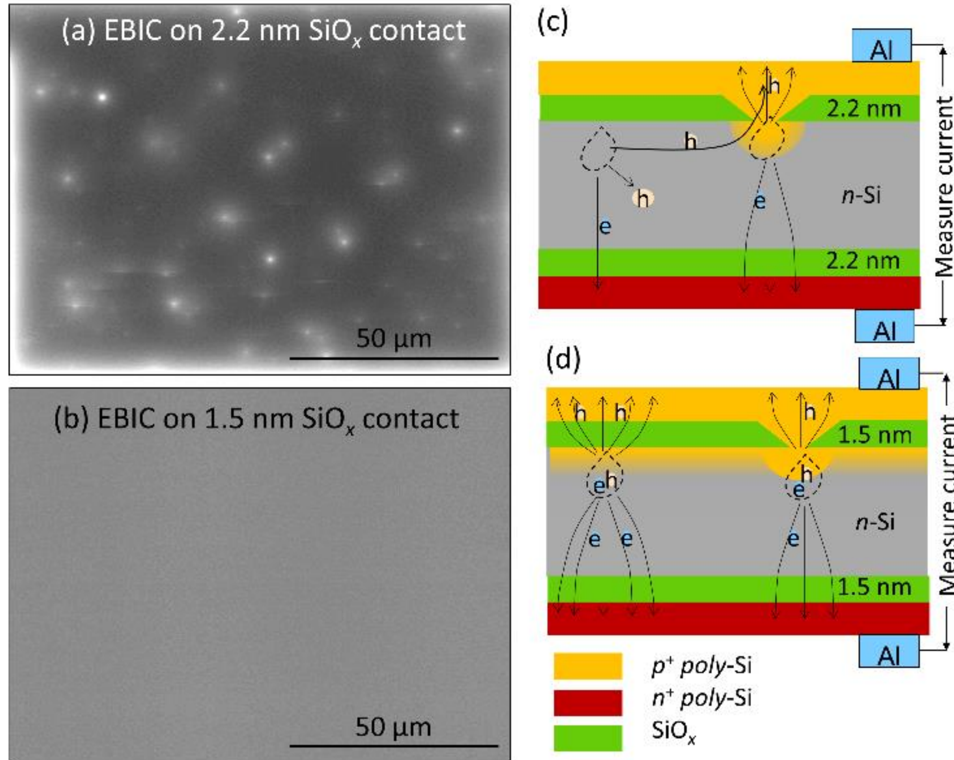

Figure 3.4 EBIC maps of p^+ *poly*-Si passivated contacts with (a) 2.2 nm and (b) 1.5 nm thick SiO_x layer. Schematic of proposed current transport pathways in passivated contact cell test structures with (c) 2.2 nm and (d) 1.5 nm thick SiO_x layer

As has been previously mentioned, the probability of detection of pinholes using techniques like TEM is very low due to their small size and low surface density [71]. To perform site-specific TEM of a potential pinhole we performed EBIC imaging in a dual-beam focused ion beam (FIB) workstation (FEI Nova NanoLab 200). After identifying a region with a few bright spots in EBIC (see dotted rectangle in Fig. 3.5a), a protective Pt layer was locally deposited on top of it. The TEM cross-section specimen was then prepared for this area by standard FIB liftout methods, and the Ga^+ ion FIB damage removed by low energy (<1 kV) Ar^+ ion milling with the

sample cooled using liquid nitrogen in a Fischione NanoMill. The milling was done close to the center of the bright spots in Fig. 3.5a. Diffraction and phase contrast high-resolution TEM imaging were then performed on the prepared sample using a TEM (FEI Tecnai G^{2}30 SuperTwin) operated at 200 kV to reduce electron-beam damage to Si. We carefully analyzed over 260 high-resolution TEM images over a 12 μm long cross-section with three bright spots (see Figure 3.5a). Most of the TEM images appear as shown in Fig. 3.5b, a uniform layer of ~2.3 nm thick SiO_x separating the *c*-Si wafer and the *poly*-Si layer. However, in one image (see Fig. 3.5c) we were able to observe significant localized thinning of the SiO_x layer. It can be seen in Fig. 3.5b that the 2.3 nm thick SiO_x layer thins down to ~1.4 nm. We refer to this thinned down SiO_x region as a conduction pinhole. We consider this as a significant finding in understanding the nature of these conduction pinholes since previous studies which have shown SiO_x balling up were performed on samples that were either intentionally annealed to very high temperatures or had a very thin SiO_x layer so as to cause significant SiO_x balling-up, which results in very poor passivation [63, 125, 126]. Our sample still retained good passivation (V_{oc} of 695 mV) and conduction. The ~1.4 nm thick SiO_x layer is within the tunneling regime and should in principle result in effects similar to an actual pinhole in the SiO_x layer, i.e., enable conduction, may create etch pits during TMAH etching, and appear as a bright spot in EBIC. Additionally, the thinner SiO_x layer will allow for more dopant diffusion than the thicker SiO_x layer, as shown by the secondary ion mass spectrometry (SIMS) depth profile in Fig. 3.5d, which has been reproduced from our previous work [113]. This enhanced dopant diffusion will create a local depletion region under the thinner SiO_x region allowing for more efficient carrier separation during the EBIC measurements, thus resulting in these conduction pinholes to appear bright as witnessed in Fig. 3.4a. We would like to clarify that in our experiments we have separated out the conduction pinhole formation step (1025 °C anneal) and the dopant

diffusion step (850 °C anneal). There are no dopants present in the *poly*-Si film when performing the 1025 °C anneal and the contacts are annealed to 850 °C after doping the *poly*-Si. Since SIMS does not have the lateral resolution to distinguish the locally thin ~1.4 nm SiO_x regions from the surrounding 2.2 nm thick SiO_x regions (see Fig. 3.5c), we instead perform SIMS on two separate samples with 1.5 and 2.2 nm thick SiO_x layers within the *poly*-Si/SiO_x/*c*-Si stack. This stack is annealed to a temperature of 850 °C, the same as our dopant drive temperature.

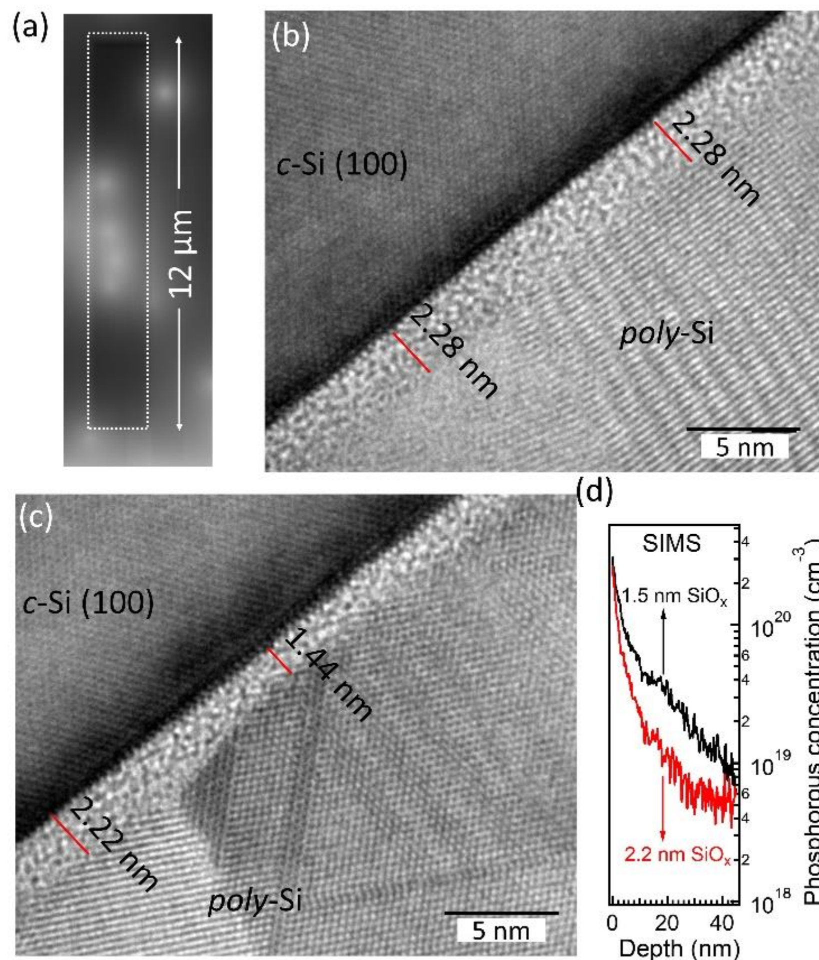

Figure 3.5 (a) EBIC image of region lifted out by FIB for TEM. Dotted rectangle shows the signal generated under the protective Pt layer. Cross sectional TEM image of pinhole type passivated contact at two different locations showing: (b) Uniform SiO_x thickness; and (c) Local thinning of SiO_x layer. (d) SIMS depth profile of phosphorous underneath the SiO_x layer of passivated contact with 1.5 (black) and 2.2 (red) nm thick SiO_x layer after annealing at 850 °C. SIMS data reproduced from Ref. [113].

The results in Figs. 3.4 and 3.5 show that tunneling through SiO_x is the dominant transport mechanism in both 1.5 and 2.2 nm SiO_x contacts. The visual identification of a conduction pinhole as a locally thinned tunneling SiO_x layer was possible due to in situ milling within the vicinity of a bright spot identified during the EBIC measurement. However, it is possible that we may have milled away the actual pinhole and are instead just imaging a section that is away from the center of a crater-shaped structure. We also cannot rule out the possibility that while some conduction pinholes may be true geometrical pinholes, others might correspond to regions with a locally thin tunneling SiO_x layer as suggested by Fig. 3.5c. This agrees with the fact that the brightness of the pinholes varies in the EBIC image for the pinhole type contact shown in Fig. 3.4a.

3.4.4. The nano-PERC concept

High performance of a Si solar cell is enabled by passivated contacts that have low contact resistivity while maintaining high degree of surface passivation. In *p*-PERC cells with an efficiency potential of ~24% [54], good surface passivation is realized by creating localized back-surface-field contacts between Al and *c*-Si through a few 10s of microns wide openings made through a dielectric Al_2O_3/SiN_x passivation layer stack deposited on *c*-Si. Below, we show that the contact performance is expected to improve remarkably by reducing the local contact (geometric pinhole) size to nanometers. Indeed, the metal to semiconductor contact area fraction f determines the surface recombination losses in the cell via the total diode current pre-factor $J_{o,\ total}$, which is given by Eq. 3.1, where $J_{o,\ pinhole}$ and $J_{o,\ oxide}$ are the pre-factors for the unpassivated metallized region and the passivated oxide region, respectively.

$$J_{o,total} = f \times J_{o,pinhole} + (1-f) \times J_{o,oxide}\ . \tag{3.1}$$

On the other hand, the total contact resistivity, which determines the fill-factor, is a sum of area-independent specific contact resistivity, $R_{pinhole}$ (in Ω·cm^2), in the pinhole and the spreading resistance within the Si wafer underneath the pinhole. The spreading resistance for effective pinhole radii, *r*, that are much less than the wafer thickness, can be approximated as $\rho_w/4r$ for a wafer bulk resistivity of ρ_w [148]. Thus the total resistance, R_{total}, is given by

$$R_{total} = \left(R_{pinhole} + \frac{\rho_w}{4r} \times \pi r^2\right)/f \approx \frac{\pi \rho_w r}{4f} . \quad (3.2)$$

The 2nd term in Eq. 3.2, which relates to the spreading resistance, is at least 2-3 orders of magnitude greater than the $R_{pinhole}$, term for pinhole sizes between 1 nm to 10 µm. The interesting conclusion to draw from Eq. 2.2 is that for the same R_{total}, as the size of pinhole decreases from ~10 µm in a *p*-PERC to ~10 nm in pinhole containing *poly*-Si contact, the unpassivated area fraction *f* can be lowered by nearly three orders of magnitude. This feature of nanostructured >2 nm SiO_x contacts allows for sufficient conduction through the pinholes in an insulating SiO_x layer in passivated contacts while resulting in very low total J_o. It must be noted that while the $J_{o,pinhole}$ term is Eq. 3.1 has some inverse dependence on the pinhole size [149], the 26.1% cell demonstrated by such contacts shows that there is a net improvement in device performance when using nanostructured contacts [68]. The above analysis interestingly shows that we can treat these pinhole containing *poly*-Si contacts as a category of PERC [139], i.e., “nano-PERC” contacts, exhibiting nanometer size holes instead of micron size holes in the passivating SiO_x layer. While in the current approach for the *poly*-Si contacts, these nanometer size pinholes are formed using high temperature annealing, we propose that other pinhole formation techniques such as nano-imprint lithography could be explored [150]. Therefore, local nano-pinhole contacts are excellent candidates for the

next generation *c*-Si photovoltaics, and could have potential uses in other photovoltaic and electronics technologies.

3.5. Conclusions and Summary

In summary, we have demonstrated the use of EBIC to map conduction-enabling pinholes in *poly*-Si/SiO_x passivated contacts. Pinhole-like structures appear as bright spots in contacts with ~2.2 nm SiO_x layer due to carrier transport and collection limitations. Site-specific TEM investigation revealed that a conduction pinhole can be a region of tunneling SiO_x layer that is ≤1.5 nm thick. The detection of similar pinholes in contacts with ~1.5 nm SiO_x layer was challenging due to artifacts created by TMAH etching and defect detection limitations in EBIC measurements: this is consistent with the tunneling nature of the 1.5 nm SiO_x layer. Thus, the carrier transport mechanism in both 1.5 and 2.2 nm thick SiO_x contacts is through tunneling, the difference being uniform tunneling in the first case while tunneling through locally thin SiO_x regions in the latter. Finally, we propose a nano-PERC concept which might allow for high efficiency *c*-Si cells.

3.6. Acknowledgements

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CHAPTER 4

EFFECT OF CRYSTALLOGRAPHIC ORIENTATION AND NANOSCALE SURFACE MORPHOLOGY ON *Poly*-Si/SiO_x CONTACTS

Modified from a future paper

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In Chapters 2 and 3 we investigated the interdependence of the SiO_x thickness and annealing temperature of a *poly*-Si/SiO_x/*c*-Si contact stack for optimum passivation and transport properties, which will enable solar cells with high V_{oc} and high *FF*, respectively. However, these experiments were performed on the well understood polished or KOH-etched planar Si surfaces, which are not efficient at light-trapping, and can hence result in low J_{sc} [43], i.e. low cell-efficiency. Hence, for the highest efficiency solar cells, passivated contacts need to be developed on a KOH-etched random pyramidal textured Si surface. However, passivation of a textured surface to obtain high V_{oc} is challenging [124, 151-153]. This has been observed across numerous cell technologies such as cells with diffused emitters, *a*-Si:H layers, and *poly*-Si/SiO_x layers. In this chapter we study *poly*-Si/SiO_x contacts on a textured Si surface. Using device results and advanced microscopies, we further show how a textured surface is very different than a polished *c*-Si surface. Our results show that the microscopic random pyramidal textured Si surface morphology with its sharp tips and valleys, and the nanoscale roughness over the pyramidal faces are the reasons for the poorer passivation on a textured surface using *poly*-Si/SiO_x contacts.

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4.1. Abstract

High-efficiency crystalline silicon (Si) solar cells require textured surfaces for efficient light trapping. However, passivation of a textured surface to reduce carrier recombination is difficult. Here, we analyze a KOH-etched, random pyramidal textured Si surface using electrical, structural and surface microscopies combined with device measurements. The effects of both microscopic pyramidal morphology and nanoscale surface roughness on passivated contacts consisting of a polycrystalline Si (*poly*-Si) deposited on top of an ultrathin, 1.5–2.2 nm, SiO_x layer is investigated. Using atomic force microscopy we show a pyramid face, which is predominantly a Si(111) plane to be significantly rougher than a polished Si(111) surface. This roughness results in a nonuniform SiO_x layer thickness as determined by transmission electron microscopy (TEM) of a *poly*-Si/SiO_x contact. Our device measurements also show an overall more resistive, and hence thicker SiO_x layer over the pyramidal surface as compared to a polished Si(111) surface, which we relate to increased roughness. Using electron-beam-induced current measurements of *poly*-Si/SiO_x contacts we further show that the SiO_x layer near the pyramid valleys is preferentially more conducting than that near the pyramid tips, edges and faces. TEM investigation confirms that this improved conduction is due to preferential break-up of the SiO_x layer near the pyramid valley, leading to direct conduction between the *poly*-Si layer and the *c*-Si wafer. Hence, both the microscopic pyramidal morphology and nanoscale roughness lead to nonuniform SiO_x layer, thus leading to poor *poly*-Si/SiO_x contact passivation. Finally, we report >21% efficient and ≥80% fill-factor front/back *poly*-Si/SiO_x solar cells on both single-side and double-side textured wafers without the use of transparent conductive oxide layers and show that the poorer contact passivation on a textured surface is limited to boron-doped *poly*-Si/SiO_x contacts.

4.2. Introduction

Solar energy is a prime candidate for meeting future world energy demands, and Si photovoltaics (PV) is the leading technology dominating the solar market. Significant processing and manufacturing optimization have brought the Si PV technology at price parity with fossil-fuel-based energy sources. However, to utilize its full potential, and to lower the net $/kWh cost of electricity, it is important to increase the cell efficiency. Even though there have been numerous reports of cell efficiencies >25% [61, 68, 137], with the current record being 26.7% [69], commercially-manufactured solar cell efficiencies remain significantly lower. Ultrahigh-efficiency Si solar cell architectures are enabled by excellent surface and contact passivation. In these architectures, the crystalline Si (*c*-Si) surface is passivated with either hydrogenated amorphous Si (*a*-Si:H), or polycrystalline silicon (*poly*-Si) with ultrathin, 1–2 nm, SiO_x layers. However, the high-temperature stability of the *poly*-Si/SiO_x contacts make them much more compatible with current industrial processes such as screen-printed metallization and firing. This in turn makes these contacts the most likely candidate for next-generation Si PV. In addition to surface passivation, excellent light-trapping is also crucial for the highest efficiency monocrystalline Si solar cells, which is usually achieved by surface texturing of a Si(100) wafer using a wet chemical etching process [43]. The resulting surface texture has 1–10 µm wide square pyramids with their edges along the Si(110) direction and their faces along the Si(111) plane. This texturing process thus affects both the morphology and the crystallographic orientation of the *c*-Si surface, and leads to enhanced carrier recombination. This effect has been observed for different Si solar cell technologies [124, 151-153]. However, there are very few studies that explore the difference in surface passivation of planar versus pyramidal Si surfaces, especially for *poly*-Si/SiO_x contacts [79, 92, 154].

The excellent passivation of crystalline Si by the *poly*-Si/SiO_x contacts is due to two combined effects: (a) the low dangling bond density at the SiO_x/*c*-Si interface [121, 122], which provides chemical passivation; and (b) the electric field created by the doped *poly*-Si layer, which selectively repels either the electrons or holes away from the Si surface. The latter mechanism is described as field-effect passivation [32]. The surface passivation quality of these junctions is quantified by the emitter recombination current density, J_o [56, 67, 123]. While a very low value of J_o <10 fA/cm^2 can be obtained using the *poly*-Si/SiO_x contacts on planar Si(100) surfaces, the contact passivation on textured Si surfaces is significantly worse with J_o ~100 fA/cm^2 [79]. This increase in J_o cannot be completely accounted for by the increased surface area on a textured surface (~1.7 times) as compared to a planar surface. The increased recombination can instead be related to a net higher defect density at the SiO_x/*c*-Si interface [79-81], which now has a dominant Si(111) crystallographic orientation on a textured Si surface instead of Si(100) orientation on a planar surface. While it has been reported that the SiO_x/Si(111) interface has a higher defect density than a SiO_x/Si(100) interface for thermally-grown SiO_2 layers [80], morphological modifications to the pyramidal surface texture such as rounding of the pyramid tips or valleys between pyramids improves *poly*-Si/SiO_x contact passivation [154, 155], despite the fact that there is only a minimal change in the Si(111) surface area fraction. Additionally, by controlling the dopant profiles and by hydrogenation of the contact structure, improved passivation of textured *c*-Si wafers was reported with J_o <10 fA/cm^2, but this did not result in high-efficiency devices [92]. Therefore, to ensure high-efficiency cells with excellent passivation and light-trapping, there is a need to understand the fundamental difference between *poly*-Si/SiO_x contacts on planar and textured *c*-Si surfaces.

Using front/back *poly*-Si/SiO_x contact cells on both single-side textured (SST) and double-side textured (DST) wafers we show that the poor *poly*-Si/SiO_x contact passivation on a textured as compared to planar Si surface is limited to boron-doped and not phosphorous-doped contacts. The effect of surface crystallographic orientation and surface morphology on oxidation and *poly*-Si/SiO_x contact performance is then investigated. Our results show that a textured Si surface oxidizes faster than a polished Si(111) surface. We relate this to surface roughness on a bare pyramid face measured using atomic force microscopy (AFM). Transmission electron microscopy (TEM) images of the *poly*-Si/SiO_x contact further verifies this and shows significant nonuniformities in the SiO_x layer thickness over the pyramid face. The local passivation on the pyramidal morphology is then studied with electron beam induced current (EBIC) measurements. While an EBIC map of a tunneling SiO_x contact (SiO_x ~1.5 nm) is similar to that of a diffused junction cell, the same measurement for a non-tunneling SiO_x contact (SiO_x ~2.2 nm) reveals that conduction through the thicker SiO_x layer occurs preferentially at the pyramid valleys. TEM results reveal that this preferential conduction at the pyramid valley is due to the absence of a SiO_x layer near the valley between the *poly*-Si layer and *c*-Si wafer.

4.3. Experimental Details

Experimental details of sample fabrication, processing, and characterization are described below.

4.3.1. Fabrication of cells with *poly*-Si/SiO_x passivated contacts on both sides

As-sawn, phosphorous-doped, *n*-type Czochralski (*n*-Cz) Si(100), 3 Ω·cm resistivity, ~195 µm thick wafers (Woongjin Co. Ltd, South Korea) were subjected to a KOH-based texturing etch resulting in ~170 µm thick DST wafers. The wafers were then cleaned using standard wafer

cleaning procedures of piranha, Radio Corporation of America (RCA)-1, and RCA-2 [128, 129]. To process a SST wafer, the DST wafer was cleaned and a ~30 nm thick thermal SiO_2 was grown at 1000 °C for 15 min in pure O_2. The SiO_2 layer on the back-side of the wafer was removed by 10% aqueous HF solution followed by a KOH-based planarization step. During the KOH-etch the SiO_2 layer on the front-side acts as a mask to protect the front-side texture. The wafers were then again treated with 10% aqueous HF solution to remove the SiO_2 layer on the front-side, thus resulting in a SST wafer. Both the SST and DST wafers were then cleaned and treated with 1% aqueous HF to remove the SiO_x formed as a result of the RCA-2 cleaning process. The wafers were then subjected to dry thermal oxidation at nearly atmospheric pressure in a quartz tube furnace at a N_2-to-O_2 gas flow ratio of 6:1 at 700 °C for 5 min resulting in ~1.5±0.05 nm thick SiO_x layer. Doped *a*-Si:H was then deposited on both sides of the oxidized *c*-Si wafers using a SiH_4/H_2 capacitively-coupled, radio-frequency plasma powered at 13.56 MHz via plasma-enhanced chemical vapor deposition (PECVD). The flow rates of SiH_4 and H_2 were 2 and 100 standard cm^3/min (sccm), respectively. Additionally, for boron or phosphorous doping, 1 sccm of B_2H_6 (2.6% in H_2) or PH_3 (3% in H_2), respectively was introduced into the chamber. The *c*-Si wafer was placed on the grounded substrate holder at a temperature of 250–350 °C with an input power to the plasma source of 8 W to grow a ~50 nm thick *a*-Si:H layer. The resulting samples with a n^+ *a*-Si:H/SiO_x/*n*-Si/SiO_x/p^+ *a*-Si:H stack were then annealed at 850 °C for 30 min in a quartz tube furnace under N_2 atmosphere to convert *a*-Si:H to a *poly*-Si layer via solid-phase crystallization. A hydrogen-induced passivation step followed, which involved deposition of Al_2O_3 via atomic layer deposition using trimethylaluminium and H_2O as precursors at 200 °C followed by annealing in forming gas (1:9 H_2:N_2 mixture) at 400 °C for 60 min. Quasi-steady-state photoconductance decay measurements were then performed using a Sinton lifetime

instrument (WCT-120) to extract the implied open circuit voltage (i-V_{oc}) and J_o values [106]. The samples were treated with 1% aqueous HF solution to remove the Al_2O_3 layer. Metallization was performed by thermally evaporating Al at a base pressure of ~10^{-7} Torr in a Temescal FC-1800 metallization tool. A ~5 µm thick Al layer was deposited on the n^+ *poly*-Si side using suitable shadow masks to form a grid and busbar pattern with ~8% shading loss, while a full-coverage blanket deposition of ~1 µm thick Al layer was performed on the p^+ *poly*-Si side, resulting in a 4 cm^2 solar cell. Since, the *p-n* junction is on the back-side of the solar cell it is referred to as a back-junction cell. A SiN_x anti-reflection layer was then deposited on the metallized n^+ *poly*-Si side using PECVD. The schematic of the resulting devices is shown in Fig. 4.1a. The cell performance was quantified using Suns-V_{oc} and current-voltage (J-V) measurements at 1 Sun AM 1.5G condition. We ensured that the probes made contact to the Al pad by applying enough force to scratch through the insulating SiN_x layer, without damaging the n^+ *poly*-Si/SiO_x contact.

4.3.2. Fabrication of test structures for determining role of surface orientation and morphology on contact resistivity and passivation

Most of the processing conditions used for all subsequent experiments were similar to those described above and hence those details will not be repeated: we will describe any differences in sample processing. Double-side-polished (DSP), phosphorous-doped, Si(100) and Si(111) float zone wafers with resistivities of 3.8 and 3.4 Ω·cm, respectively were cleaned, treated with 1% aqueous HF solution, and then subjected to dry thermal oxidation. The N_2-to-O_2 gas flow ratio was varied between 0 to 100 and the oxidation temperature between 700 to 1000 °C. The SiO_x thickness on both wafer types was measured using spectroscopic ellipsometry within a few hours after oxidation. On few of the oxidized samples, a n^+ *a*-Si:H layer was deposited on one side via PECVD and the samples were crystallized at 850 °C for 30 min. A ~1 µm thick Al layer was then

deposited as rectangular Al pads with varying spacing using shadow masks resulting in an Al/n^+ *poly*-Si/SiO_x/n-Si structure. The metal to n^+ *poly*-Si contact resistivity was determined using the transmission line method (TLM) [132]. The structure with the TLM pattern was then subjected to reactive ion etching using SF_6 plasma with the Al pads on the front acting as etching masks. The etching removed the n^+ *poly*-Si and SiO_x layers in the unmasked regions along with a few microns of the underlying *c*-Si wafer. The resulting structure was utilized to determine the through-SiO_x contact resistivity for the n^+-n high-low junction by TLM analysis. To further understand the role of surface orientation and morphology on cell performance, we fabricated front/back *poly*-Si/SiO_x devices on the DSP Si(100), DSP Si(111) and DST wafers. For these cells, the tunneling SiO_x layer was grown at 700 °C using a 6:1 N_2-to-O_2 gas flow ratio, and the oxidation times were varied between 5 and 30 min. The remaining steps were similar to those described above for fabrication of front/back *poly*-Si/SiO_x devices.

4.3.3. Characterization of the Si(111) pyramidal face with SEM, AFM and TEM

SEM imaging of the textured Si surface was performed using a JEOL 7000F SEM at an accelerating voltage of 2 kV. AFM measurements were performed using an Asylum Research MFP-3D atmospheric AFM with an Al-coated Si tip (BudgetSensors Tap190-G) in the tapping mode. Phase maps were also acquired during the topography measurement. The textured sample was cleaned and mounted on a stage at a 55° angle with respect to the AFM stage. The measurements were performed a few microns from the top edge of the sample. AFM measurements were also performed on a polished Si(111) wafer which lay flat on the AFM stage. The wafers were cleaned prior to the measurement and therefore should only be covered by a ~1 nm native SiO_x layer. Phase contrast TEM imaging was performed on a n^+ *poly*-Si/SiO_x contact on a textured wafer with a FEI Tecnai $G^2$30 SuperTwin transmission electron microscope operating at 300 kV.

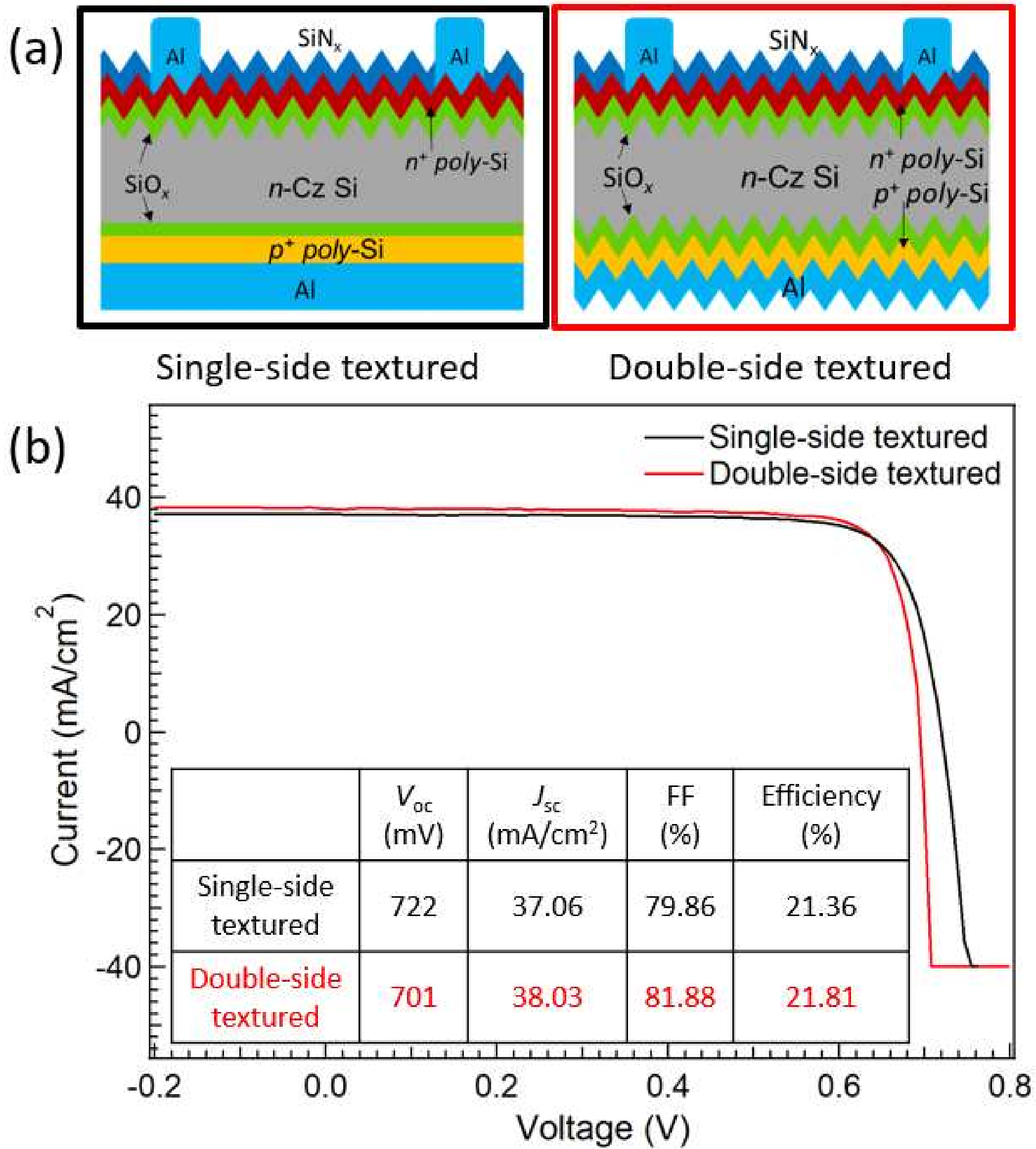
4.3.4. EBIC measurement of poly-Si/SiO$_x$ contacts on a textured surface

EBIC measurements were performed on DST front/back *poly*-Si/SiO$_x$ devices with either a ~1.5 or ~2.2 nm SiO$_x$ layer (measured on a polished Si(100) wafer). The device processing for the ~1.5 nm SiO$_x$ contact was the same as described in Section 4.3.1. However, the processing for the contact with a ~2.2 nm SiO$_x$ layer was different so to obtain best passivation and transport properties, the details of which have been discussed in Section 3.3.2. Briefly, a DST wafer was oxidized at 800 °C for 10 min using a 6:1 N_2-to-O_2 gas flow ratio which results in a ~2.2 nm thick SiO$_x$ layer (measured on a polished Si(100) wafer). A ~40 nm thick intrinsic (*i*) *a*-Si:H was then deposited on both sides of the oxidized wafer using PECVD and the samples annealed at 1025 °C for 30 min in N_2. Following a treatment with 1% aqueous HF solution, doped *a*-Si:H films were then deposited on either side to form a n^+ *a*-Si:H/*i* *poly*-Si/SiO$_x$/*n*-Si/SiO$_x$/*i* *poly*-Si/p^+ *a*-Si:H structure. The samples were then annealed in N_2 at 850 °C for 30 min to form a n^+ *poly*-Si/SiO$_x$/*c*-Si/SiO$_x$/p^+ *poly*-Si structure. Subsequent processing steps of Al_2O_3 deposition, forming gas anneal, metallization, etc. were similar to those of the *poly*-Si device with the 1.5 nm SiO$_x$ layer and described in Section 4.3.1. The fill-factors (FF) of both the cells with the 1.5 and 2.2 nm SiO$_x$ contacts was >75% indicating a conducting SiO$_x$ layer. EBIC measurements were then performed on both these cells using a JEOL JSM-7600 FESEM and Mighty EBIC quantitative EBIC setup. An electron-beam accelerating voltage of 5 kV and ~5 nA beam current were used for the EBIC measurements in both plan-view and cross-section orientations. Cross-section samples were prepared by ion milling using 4 kV Ar^+ ions resulting in a smooth surface. Plan-view EBIC measurements were performed on the n^+ *poly*-Si side while the cross-sectional EBIC was performed on the p^+ *poly*-Si side of the same device for better resolution.

4.4. Results and Discussion

Experimental results are provided and discussed below.

4.4.1. *Poly*-Si/SiO$_x$ contact passivation on planar and textured surfaces



	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
Single-side textured	722	37.06	79.86	21.36
Double-side textured	701	38.03	81.88	21.81

Figure 4.1 (a) Schematic of front/back *poly*-Si/SiO$_x$ contact cells on SST and DST *n*-Cz Si wafers. (b) Current-voltage measurements of the cells shown in “a”. The table in the inset shows their cell parameters.

Figure 4.1a shows the schematics of two cells on *n*-Cz Si(100) wafers with *poly*-Si/SiO_x contacts on both the front and rear side. Both cells consist of a n^+ *poly*-Si/SiO_x contact on the textured front side, and a p^+ *poly*-Si/SiO_x contact on the planar or textured rear side. Figure 4.1b shows the current-voltage (*J*-*V*) data for these *poly*-Si/SiO_x cells. The tunnelling SiO_x was grown at 700 °C for 5 min with a 6:1 N_2-to-O_2 gas flow ratio, which results in ~1.5 nm thick SiO_x layer (measured on a polished Si(100) wafer). These back-junction cells on both SST and DST wafers result in cell efficiencies >21%. The high-low junction on the front-side lowers the grid series resistance, enabling high FF, ≥80%, without the need of expensive transparent conducting oxide layers on the front or rear sides [95, 156]. Fabricating cells with DST wafers is of interest since it removes the need for a planarization step. Also, the J_{sc} for the DST cell is 2.7% higher compared to the SST cell, which is consistent with better light trapping due to texture on both sides [43]. However, the substantially lower open-circuit voltage (V_{oc}) for the DST cell, 701 mV, as compared to that for the SST cell, 722 mV, can be attributed to poorer passivation of p^+ *poly*-Si/SiO_x contact on a textured surface. This corresponds to a J_o value of 8.0 and 33.2 fA/cm^2 for the SST and DST device, respectively. For n^+ *poly*-Si/SiO_x symmetric test structures on DST wafers we obtained a J_o of ~3.4 fA/cm^2, which indicates excellent surface passivation of the textured surface. Since poorer *poly*-Si/SiO_x contact passivation on a textured surface is observed for boron-doped and not phosphorous-doped contacts, the poor passivation of boron-doped *poly*-Si/SiO_x contact is likely related to a boron-SiO_x interaction [76, 77], rather than only poorer SiO_x/*c*-Si interfacial passivation of a predominantly Si(111) faceted textured surface [79-81]. Even on a planar surface, boron preferentially segregates in the SiO_x layer affecting the quality of SiO_x/*c*-Si interface, which results in poorer passivation of boron-doped *poly*-Si/SiO_x contacts as compared to phosphorous-doped contacts [70].

4.4.2. Role of surface orientation and morphology on contact resistivity and passivation

To understand the origins of the poor contact passivation on a pyramidal textured Si surface we first need to first understand what makes a pyramidal textured surface different from a planar Si surface. Here, we explore how crystallographic orientation and surface morphology affect thermal oxidation of Si, and hence, *poly*-Si/SiO_x contact performance. In Chapter 2, we showed that passivation quality of the *poly*-Si/SiO_x contact is sensitive to SiO_x thickness [113]. It is also known that the oxidation rate of *c*-Si depends on surface orientation [157]. Therefore, it is important to optimize oxidation time for different crystallographic surfaces to obtain nominally similar passivation quality. In Fig. 4.2a we show the thickness of thermally-grown SiO_x layer on polished *n*-type Si(100) and Si(111) wafers of similar resistivities for different oxidation conditions. The SiO_x thickness was fitted using spectroscopic ellipsometry. The inset of Fig. 4.2a shows that for >20 nm thick SiO_2 layers grown at 1000 °C in pure O_2, thermal SiO_2 is thicker on the Si(111) surface than that on a Si(100) surface, which is consistent with previous studies [157]. However, for 1–3 nm thick SiO_x layers grown at lower temperatures, 700–900 °C (see Fig. 4.2a), we observed that the SiO_x thickness on Si(111) was consistently slightly lower than that on the Si(100) wafer for all N_2:O_2 dilution ratios ranging from 6:1 to 100:1. At only one oxidation temperature of 900 °C, 50:1 N_2-to-O_2 gas flow ratio, and 30 min oxidation time, the SiO_x on Si(111) was ~2 Å thicker than on the Si(100) surface. Since the difference in the SiO_x thickness on Si(100) and Si(111) wafers in the 1–3 nm range, which is the most relevant for *poly*-Si/SiO_x passivated contacts [113, 158], is only 1–2 Å, we further verified the differences in SiO_x thicknesses by measuring through-SiO_x conductivity in n^+ *poly*-Si/SiO_x/*n*-type *c*-Si structures. The exponential dependence of tunnelling conductivity on SiO_x thickness [62], makes contact resistivity a good metric for verifying the difference in SiO_x thickness. Figure 4.2b shows the

contact resistivity measured through an Al/n^+ *poly*-Si/SiO_x/n-type c-Si stack for different oxidation conditions. Consistent with the ellipsometry measurements, for the same oxidation conditions, the contact resistivities for Si(111) wafers were a few orders of magnitude lower than Si(100) wafers. It is important to note the significant change in SiO_x resistivity, a few orders of magnitude, when SiO_x thickness increases from 1.7 to 1.8 nm for the Si(100) wafer. This corresponds to an oxidation time of 10 and 15 min respectively at 700 °C. Such a sharp rise in contact resistivity observed near 1.7 nm SiO_x thickness is consistent with tunnelling theory [62], and indicates transition from conducting to non-conducting SiO_x for solar cell applications. In order to minimize human error during the manual sample loading in our oxidation furnaces we oxidized both the Si(100) and Si(111) wafers together. The variations in SiO_x thickness between wafers oxidized near the start and end of our hot-zone in the tube furnace is <0.05 nm.

Our results from Fig. 4.2 show that the lower growth rate of SiO_x on Si(111) as compared to Si(100) wafers is specific for SiO_x thicknesses <3 nm and that the trend is reversed for SiO_x layers >3 nm. We speculate that this may be related to fundamentally different oxidation kinetics for Si(100) and Si(111) surfaces [159]. Additionally, the Si(100) and Si(111) surface have different dangling bond density which may also lead to differences in the interfacial SiO_x layer between SiO_2 and c-Si for Si(100) and Si(111) surfaces [160]. Since the passivation quality of the *poly*-Si/SiO_x contact is sensitive to SiO_x thickness [113], thermal oxidation conditions must be optimized to take into account the effect of different surface orientations affecting SiO_x thickness, as discussed below.

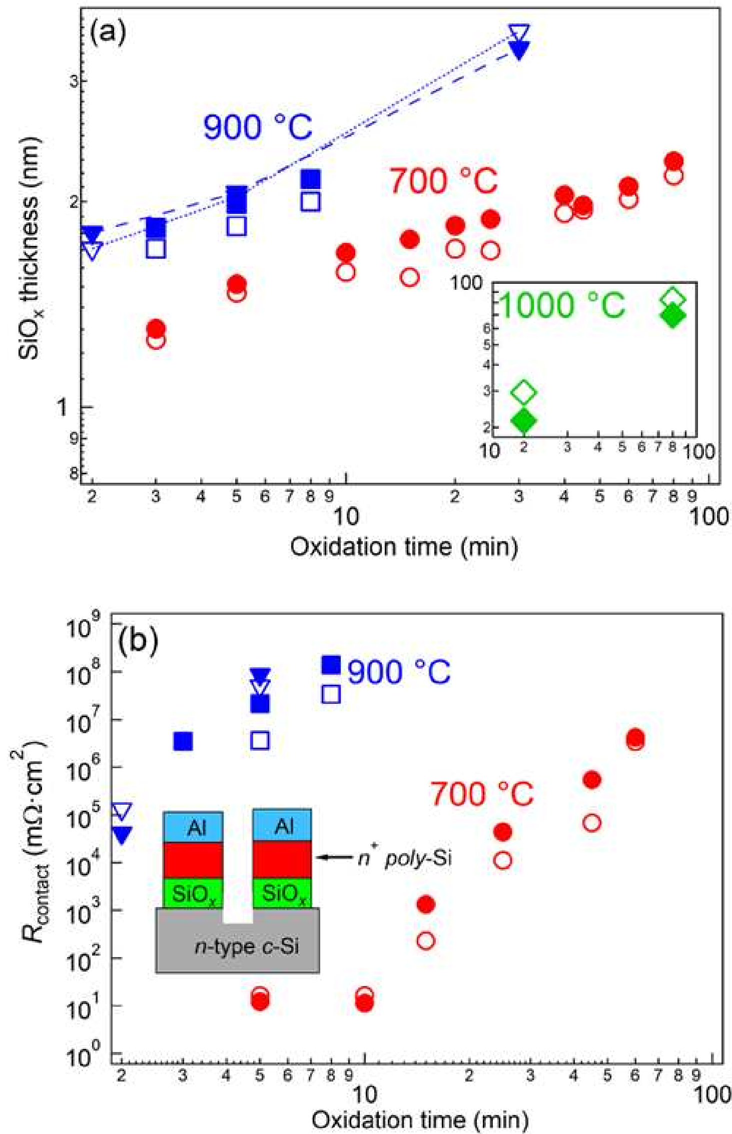


Figure 4.2 (a) Thickness of SiO_2 layer grown on Si(100) (closed symbols) and Si(111) (open symbols) surfaces as a function of oxidation time for three different oxidation temperatures of 700 (red), 900 (blue), and 1000 °C (green) (see inset) at N_2:O_2 gas flow ratios of 6:1 (●, ○), 50:1 (▼, ▽), 100:1 (■, □), and 0:1 (◆, ◇). The lines are a guide to the eye. (b) The through-SiO_x contact resistivity of a n^+ *poly*-Si/SiO_x/*n*-type *c*-Si stack on polished Si(100) and Si(111) wafers. The color scheme and symbols are the same as those described in "a".

To determine the optimum oxidation conditions for the growth of the tunnelling SiO_x layer for *poly*-Si/SiO_x contacts we varied the oxidation time between 5–30 min at 700 °C using 6:1 N_2-to-O_2 gas flow ratio and fabricated cells on DSP Si(100) and Si(111) wafers of similar

resistivities. The cell architecture is similar to that shown in Fig. 4.1a. These devices allow us to determine the effect of crystallographic orientation on *poly*-Si/SiO_x device performance. In parallel, to study the effect of pyramidal surface morphology, we also tested device performance on DST wafers which were oxidized under similar conditions to the DSP wafers. In these devices, the SiO_x thickness was between 1.4–1.9 nm on DSP wafers, but could not be directly measured with ellipsometry on the DST wafers. Figure 4.3 shows the changes in V_{oc} as a function of oxidation time. The V_{oc} for devices fabricated on DSP Si(100) and Si(111) wafers first increases with oxidation time and then decreases. However, the V_{oc} for the devices fabricated on the DST wafers decreases monotonically with increasing oxidation time. As shown previously in Fig.2.1, the V_{oc} trend observed for the devices fabricated on polished wafers to be related to an optimum balance between chemical passivation and field-effect passivation [113]. While chemical passivation from the SiO_x layer improves with increasing SiO_x thickness, the field-effect passivation due to dopant diffusion from the *poly*-Si layer through the SiO_x into the *c*-Si wafer decreases with increasing SiO_x thickness. Similar to other studies we observe the V_{oc} on Si(111) to be lower than that on Si(100) [79]. Since both the DSP Si(100) and Si(111) wafers had similar bulk lifetimes (data not shown), our results support the hypothesis that the higher defect density at the SiO_x/Si(111) interface might be the reason for poorer passivation on the Si(111) surface [79-81]. The monotonically decreasing V_{oc} for the devices fabricated on the DST wafers with increasing oxidation time therefore shows that passivation of a textured surface is different than that of polished Si(100) and Si(111) surfaces for *poly*-Si/SiO_x contacts. Furthermore, our results suggest that the best passivation for DST wafers may be obtained at a lower oxidation time compared to DSP wafers. We should mention that the V_{oc} values for the devices on DSP wafers used for this study are significantly ~20 mV lower, than those we usually obtain on our planar

saw-damage removed *n*-Cz Si(100) wafers. Hence, V_{oc} trends between the devices on DST and DSP wafers, and not the absolute V_{oc} values, should be compared.

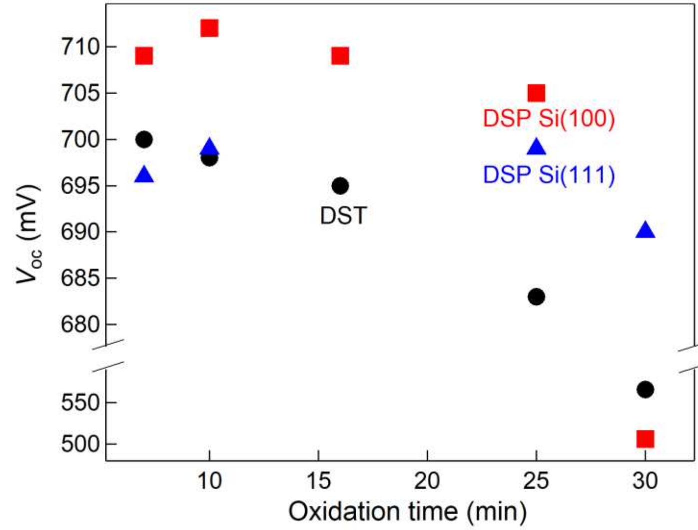


Figure 4.3 Effect of oxidation time on V_{oc} of front/back *poly*-Si devices on DST (●), DSP Si(100) (■) and DSP Si(111) (▲) wafers.

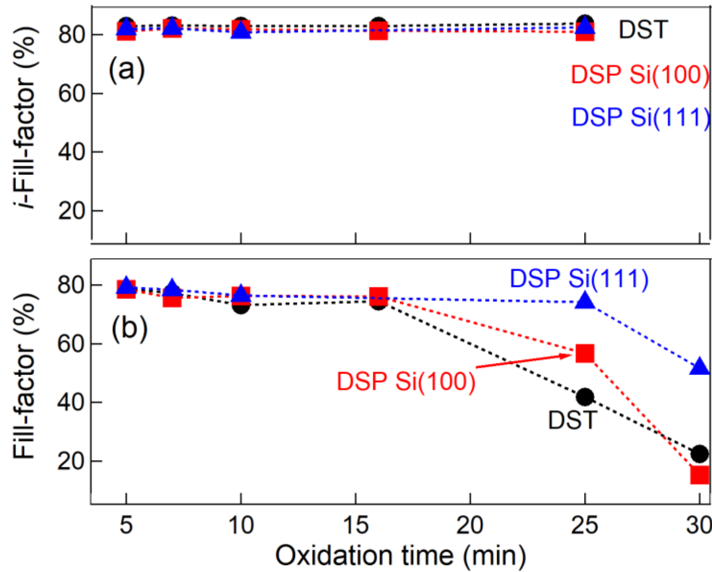


Figure 4.4 Effect of oxidation time on (a) *i-FF* and (b) *FF* of *poly*-Si devices on DST (●), DSP Si(100) (■), and DSP Si(111) (▲) wafers. The dotted lines are a guide to the eye.

In addition to a high V_{oc}, which is a measure of good passivation, the *poly*-Si/SiO_x contacts should also have a low series resistance to obtain a high fill-factor (*FF*) for the device. Figure 4.4a shows the implied fill-factor (*i-FF*) [105], for various devices as a function of oxidation time. There is no clear trend in the *i-FF,* which is between 83-84% for DST devices and between 80-82% for DSP devices. However, in Fig. 4.4b, which shows the *FF* of the same devices, we see that irrespective of the surface orientation and morphology the *FF* reduces as oxidation time increases. The highest FF of ~79% at 5 min oxidation time is measured on the DST device. Since, all the devices have similar *i-FF*, we can conclude that the reduction in *FF* with increasing oxidation time may be due to the increased series resistance from the thicker SiO_x layer, i.e., the conductivity through the SiO_x layer is limiting conductivity of the *poly*-Si/SiO_x/*c*-Si stack. Comparing the *FF* at ≥25 min oxidation time, we see that the *FF* on DSP Si(111) wafer is much higher than that on DSP Si(100), which can be explained by the slower oxidation rate on Si(111) as compared to Si(100) (see Fig. 4.2). Surprisingly, the *FF* of the DST device under similar oxidation conditions is also much lower than that for a Si(111) device. This is particularly interesting since it shows that under similar oxidation conditions, the SiO_x layer on a textured surface, which is supposed to be predominantly Si(111) faceted, is much more resistive, and hence likely thicker, than that on a polished Si(111) surface.

Our results from Figs. 4.3 and 4.4 indicate that a pyramidal textured Si surface, which should be predominantly Si(111) faceted, is very different from a polished Si(111) and Si(100) surface. This is observed for both passivation and effective oxidation rate. Since cell efficiency depends on both V_{oc} and *FF*, we can plot their product to optimize the thermal oxidation time as there can be sample to sample variations in grid shadowing which affects J_{sc}. The J_{sc} values for the DST and DSP devices were between 37–39 and 32–34 mA/cm^2, respectively. The data in

Fig. 4.5 shows the V_{oc} and *FF* product for the various *poly*-Si/SiO_x devices. Fig. 4.5 shows that for both DST and DSP devices, the highest $V_{oc}\times FF$ products are obtained at an oxidation time of 5 min. Thus, we can infer that even though the V_{oc} trends may be different between devices fabricated on DSP and DST wafers (see Fig. 4.3), the effect of reduction in *FF* with oxidation time (see Fig. 4.4b) limits device performance. Using an optimal oxidation time of 5 min, devices were fabricated using DST and SST wafers, as already shown in Fig. 4.1b. Both the DST and SST devices were made from the same batch of as-sawn wafers with comparable bulk lifetimes. Even at this optimal oxidation condition of 5 min, the p^+ *poly*-Si contact on the planar surface provides better passivation than on a textured surface. Therefore, we conclude that over the range of conditions explored in this study, a simple re-optimization of oxidation condition does not lead to a better device on a DST wafer. These results lead us to the conclusion that the pyramidal surface morphology is more difficult to passivate rather than the polished Si(111) surface. Below we investigate the surface morphology and SiO_x uniformity on a textured pyramidal surface using AFM, TEM and EBIC measurements.

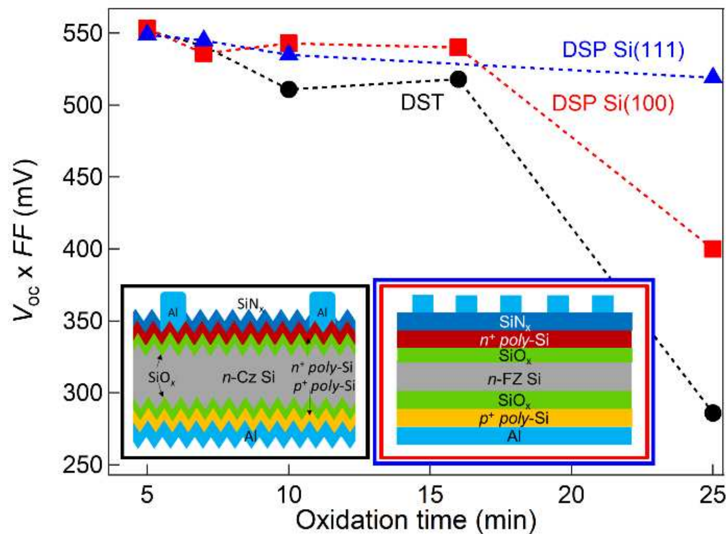


Figure 4.5 Effect of oxidation time on V_{oc} and *FF* product of poly-Si devices on DST (●), DSP Si(100) (■) and DSP Si(111) (▲) wafers. The dotted lines are a guide to the eye.

4.4.3. Surface and oxidation non-uniformities of a pyramidal Si(111) face on a textured surface

Figure 4.6a shows the scanning electron microscopy (SEM) image of a cleaned textured Si surface without a *poly*-Si/SiO_x stack. The image was obtained at a low beam accelerating voltage of 2 kV for enhanced surface sensitivity. In addition to pyramids that are ~2–3 µm in size, we can also observe a ridge-pattern on the pyramid faces, which indicates that the pyramidal Si(111) face is not atomically smooth. To determine the degree of surface roughness of the pyramidal Si(111) facet we performed AFM measurements on a cleaned textured wafer surface. Due to a delay between the sample cleaning and the atmospheric AFM measurement, we expect the wafer surface to be covered by a ~1 nm thick native SiO_x layer. The sample was mounted at an angle of ~55° during the measurement to align the pyramid face perpendicular to the AFM tip. Fig. 4.6b shows the AFM phase image of a 5×5 µm region on the textured wafer. The phase contrast image in Fig. 4.6b is shown to facilitate the determination of potential locations of the pyramid faces within the scanned area. Regions "c" and "d" on the pyramid face were rescanned and the 3D renditions of their surface topography are shown in Figs. 4.6c and 4.6d, respectively. As a control, we also imaged the surface topography of a polished Si(111) surface, which is shown in Fig. 4.6e. The significantly higher roughness of the pyramid face can be seen by comparing Figs. 4.6c and 4.6d with Fig. 4.6e. This can also be quantified by the higher standard deviation of 1.1 and 0.4 nm on the pyramidal face in regions "c" and "d" respectively, as compared to 0.1 nm measured on the polished Si(111) wafer. It must be noted that in addition to actual surface roughness, the calculated surface roughness, quantified by the standard deviation value, also depends on the size of the scanned area. Figs. 4.6c and 4.6d show that the standard deviation of the surface topography images reduces from 1.1 to 0.4 nm when the scanned area is reduced from ~800×800 to ~300×300

nm region, respectively. Hence, to accurately estimate the extent of surface roughness, it is important to scan a sufficiently large area. This increased roughness over the pyramidal Si(111) face may lead to more surface defects than on a polished Si(111) surface, which in turn may affect the growth of the SiO_x layer [161]: this will lead to an overall more resistive SiO_x on a textured surface as compared to a polished Si(111) surface as has been observed from the *FF* results in Fig. 4.4.

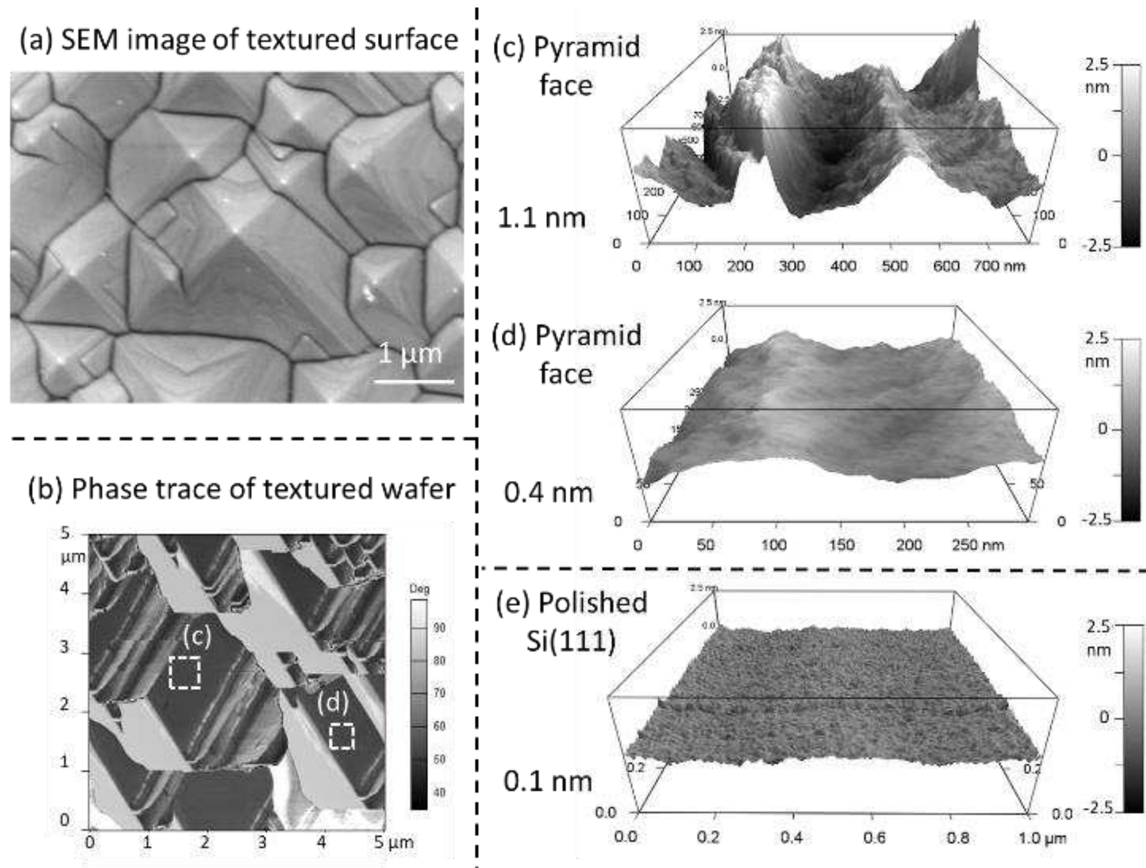


Figure 4.6 (a) SEM image of the textured Si surface. (b) Phase map of the pyramidal textured Si wafer measured with the Si wafer mounted at an angle of ~55° with respect to the AFM stage. (c, d) 3D renditions of the surface topography showing regions "c" and "d", which are highlighted as boxed areas in image "b". (e) 3D rendition of the surface topography of a polished Si(111) wafer with the wafer mounted flat with respect to the AFM stage (i.e. surface and AFM stage are parallel). The standard deviation of the height (z-axis of each image) in Figs. c–e is also shown with the surface topography images.

To determine the uniformity of the SiO_x layer on a textured surface we performed a cross-sectional TEM investigation of a *poly*-Si/SiO_x/*c*-Si stack annealed at 850 °C. The oxidation step was performed at 700 °C for 5 min in 6:1 N_2-to-O_2 gas flow ratio, which resulted in a ~1.5 (±0.05) nm thick SiO_x layer on a polished Si(100) wafer. Figure 4.7 shows the TEM images obtained at four different locations on the pyramidal Si(111) face. There is a significant nonuniformity in the SiO_x thickness, which varies between 1.4 to 2.3 nm. While a direct comparison between local surface roughness and SiO_x thickness was not performed, our TEM results clearly show that the oxidation on a pyramidal Si(111) facet of a textured Si surface is quite nonuniform. This nonuniformity of oxidation might be related to nano-roughness on the pyramid face resulting in an overall thicker and hence more resistive SiO_x layer than on a polished Si(111) surface. Thus, these observations are consistent with the lower FF for cells on DST wafers shown in Fig. 4.4b.

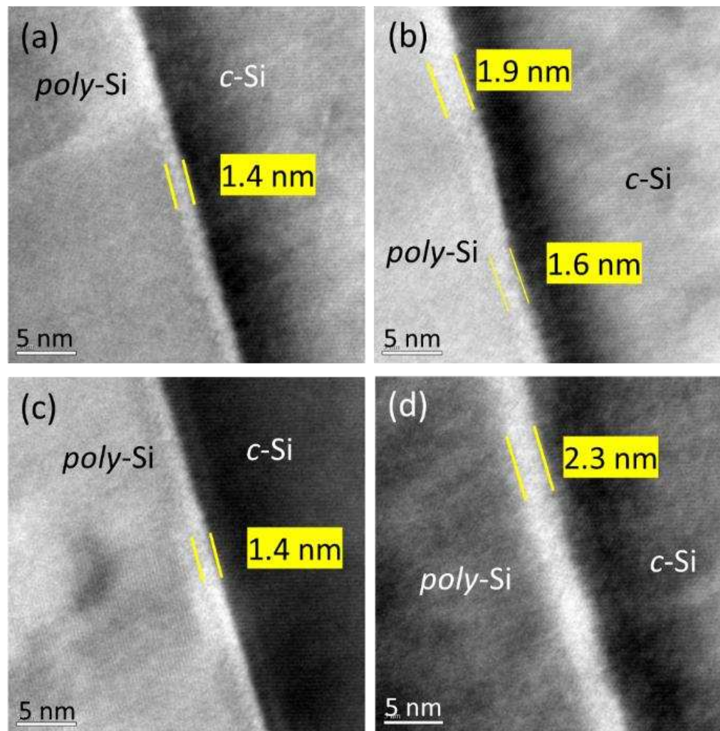


Figure 4.7 Cross-section TEM of a n^+ *poly*-Si/SiO_x/*c*-Si stack at various locations on a pyramidal textured Si surface.

4.4.4. EBIC measurement of *poly*-Si/SiO_x contacts on a textured surface

To determine if the poorer passivation of *poly*-Si/SiO_x contacts on a textured surface is related to the pyramidal morphology of the textured Si surface we further investigated these contacts with EBIC measurements. The signal intensity in EBIC images results from the separation of electron-hole pairs generated by the electron beam within a SEM and subsequent collection of these excited carriers, which results in a current which is then mapped over the scanned region [111, 112]. The generated current is dependent on the interaction of charge carriers with defects or inhomogeneities in the device as well as the carrier collection probability. Thus, EBIC measurements can result in maps which have either no features due to spatially uniform carrier collection, darker features due to carrier recombination in regions with a high defect density, or brighter features due to enhanced local carrier collection.

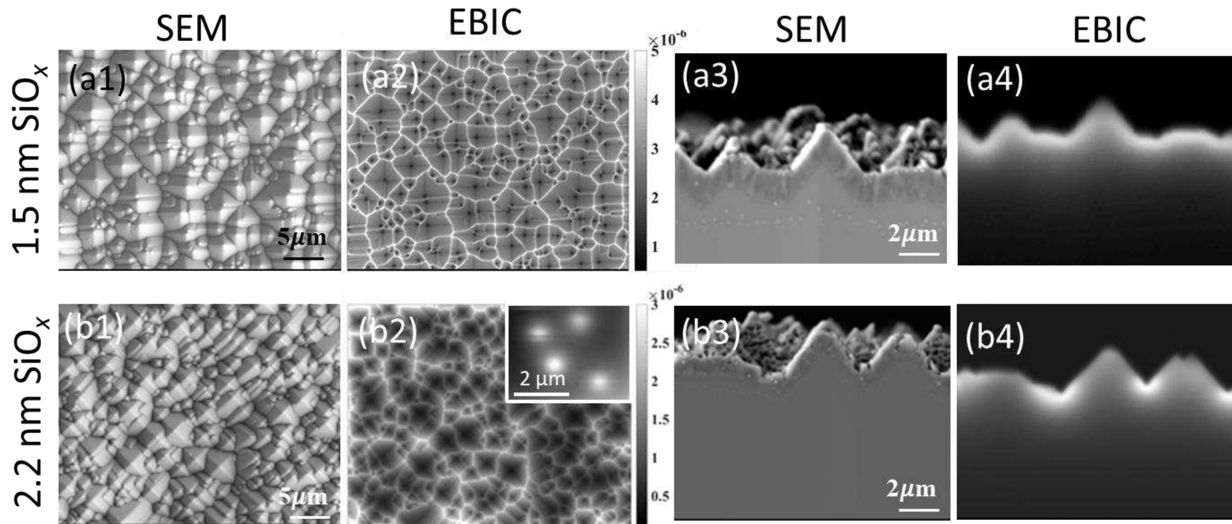


Figure 4.8 (a1) Plan view SEM image for a 1.5 nm SiO_x contact. (a2) EBIC image corresponding to the area shown in a1. (a3) Cross-sectional SEM image for a 1.5 nm SiO_x contact. (a4) EBIC image corresponding to the area shown in a3. Images b1-b4 follow the same sequence as a1-a4, but are for a 2.2 nm SiO_x contact. The plan view measurements were performed on the n^+ *poly*-Si side while the cross-sectional images were performed on the p^+ *poly*-Si side. The inset of Fig. 8b2 shows the plan-view EBIC map (not quantified) of a 2.2 nm SiO_x contact on a polished *c*-Si surface. Please refer to Chapter 3 for further details of that sample.

We investigated *poly*-Si/SiO_x contacts with either a ~1.5 or ~2.2 nm thick SiO_x layer with plan-view and cross-sectional EBIC maps, shown in Fig. 4.8. It is known that while conduction through a ~1.5 nm SiO_x contact occurs through uniform tunnelling through the SiO_x layer, for the ~2.2 nm SiO_x contact it occurs through localized thinned-down tunnelling and/or pinhole regions in the SiO_x layer [64]. Figures 4.8a1 and 4.8a2 show the plan-view SEM and corresponding EBIC images, respectively of the ~1.5 nm SiO_x contact, and Figs. 4.8a3 and 4.8a4 show the cross-sectional SEM and corresponding EBIC images, respectively, of the same contact. Figures 4.8b1-b4 follow the same sequence as Figs. 4.8a1-a4, but are for a ~2.2 nm SiO_x contact instead. The inset of Fig. 4.8b2 shows the EBIC image of a n^+ *poly*-Si/2.2 nm SiO_x contact on a polished Si surface. Please refer to Chapter 3 for details regarding the polished sample. Comparing the plan-view SEM images of the ~1.5 and ~2.2 nm SiO_x contacts (see Fig. 4.8a1 and 4.8b1) we do not see any significant differences since the original wafers were subjected to the same texturing process. However, comparing the EBIC maps for the two we notice a considerable difference (see Figs. 4.8a2 and 4.8b2). The EBIC map for the ~1.5 nm SiO_x contact (Fig. 4.8a2) has features with different intensities, with the pyramid valleys being the brightest followed by faces, then by the pyramid edges, and then the pyramid tips. These locations were identified by comparing the EBIC map (Fig. 4.8a2) with its corresponding SEM image (Fig. 4.8a1). Fig. 4.8a2 is similar to the EBIC image of a diffused emitter on a textured surface [162]. A diffused emitter consists of a few microns thick heavily-doped Si layer on a low-doped Si wafer. Since, a diffused emitter does not contain any transport-limiting SiO_x layer between the two differently doped layers, it should exhibit uniform carrier collection over a planar sample surface. However, EBIC images of a diffused emitter on a textured Si surface show features with different contrast [162]: this is due to the pyramidal nature of the surface which results in nonuniform carrier excitation and collection

efficiencies. From the similarity between the plan-view EBIC for a tunnelling SiO_x contact and that of a diffused-junction contact we can infer that the ~1.5 nm SiO_x layer is not limiting carrier transport, which is consistent with the tunnelling nature of such a ~1.5 nm thick SiO_x layer [64]. The cross-sectional EBIC image of the p^+ *poly*-Si side (see Fig. 4.8a4) on the same sample shows a uniform bright layer following the surface texture. This indicates a uniform carrier-collection over the pyramidical textured surface due to two phenomena: uniform electric-field between the *poly*-Si layer and the Si wafer, and uniform conduction through the SiO_x layer. This is again consistent with the tunnelling nature of the SiO_x layer. There is a slight darkening observed near one pyramid tip in Fig. 4.8a4, which might indicate the presence of defects, thus lowering the local EBIC intensity. However, interpretation of this is difficult without modelling due to variations in carrier excitation across the pyramidal surface. This is especially true near the pyramid tips in a cross-sectional measurement because the volume in which the electron beam needs to be absorbed is very small.

The plan-view (see Fig. 4.8b2) and cross-section (see Fig. 4.8b4) EBIC map of the ~2.2 nm SiO_x contacts are visibly different compared to the ~1.5 nm SiO_x contacts (see Fig. 4.8a2 and 4.8a4). In Fig. 4.8b2 only a few valleys between pyramids appear bright. Furthermore, it is difficult to see any contrast between the pyramid faces, edges, and tips. The enhanced brightness at the pyramid valleys is easier to see in the cross-sectional EBIC map (see Fig. 4.8b4). Comparing the EBIC results for a ~2.2 nm SiO_x contact to our previous EBIC results for a similar contact on a polished *c*-Si surface (see inset of Fig. 4.8b2), we can conclude that these local bright spots can be regions of a thinner, tunnelling SiO_x layer, sometimes referred to as “pinholes”. Such locally thin SiO_x regions not only enable conduction, but also lead to enhanced local dopant diffusion [163], improving the EBIC collection probability in the vicinity of a pinhole, thus making them appear

brighter than the background [64]. We can infer from the EBIC map of the ~1.5 nm SiO_x tunnelling contact (see Fig. 4.8a4), that the pyramidal morphology does not significantly influence EBIC contrast near valleys in the cross-sectional view. Hence, the enhanced brightness at the pyramid valleys for the ~2.2 nm SiO_x contact is not an artifact of the EBIC measurement. From the EBIC images of the ~2.2 nm SiO_x contact (Figs. 4.8b2 and 4.8b4) we can make three interesting observations: (1) the thinner conducting SiO_x regions are preferentially observed only in the valleys between pyramids; (2) the conductive regions are present as continuous channels instead of being isolated "pinholes" as has been seen on a polished *c*-Si surface (see inset of Fig. 4.8b2); and (3) not all valleys are equally bright. From these EBIC results we can conclude that the pinhole formation in the SiO_x layer due to high-temperature annealing of a *poly*-Si/SiO_x/*c*-Si stack is affected by pyramidal surface morphology, and occurs preferentially near the pyramid valleys. The SiO_x layer near a pyramid valley experiences more compressive stress than at the pyramid tips [147, 164, 165]. Since mechanical stress in the SiO_x layer can affect the diffusivity of oxygen [166], we speculate that this effect can play a role in the relative Si oxidation rate in the valleys versus the other regions. Alternatively, this mechanical stress can lead to preferential thinning of the SiO_x layer in the valleys during the high-temperature annealing step [125]. The EBIC results on the ~2.2 nm SiO_x contacts are particularly interesting since they show that surface morphology can be used to engineer and control the pinhole formation process in *poly*-Si/SiO_x/*c*-Si contacts.

4.5. Conclusions

In summary, we have performed a detailed study towards understanding the reason for the poor passivation of *poly*-Si/SiO_x contacts on a pyramidal textured surface on Si(100) wafers. By studying the effect of both surface crystallographic orientation and surface morphology, we conclude that the pyramidal faces are more difficult to passivate due to their morphology and not

because of the Si(111) orientation of the pyramidal surface. The poorer *poly*-Si/SiO_x contact passivation on a textured Si surface is limited to boron-doped and not phosphorous-doped contacts. From the electrical characterization of the cells, we infer that both the passivation of and transport through *poly*-Si/SiO_x layers on a textured surface are very different than that on polished Si(100) and Si(111) surfaces. Using AFM and TEM we relate this to nonuniformities in the SiO_x layer due to nano-roughness on the pyramid face. Our EBIC measurements further show that even the pyramidal morphology consisting of pyramid tips, faces, edges and valleys causes SiO_x related non-uniformities. This results in the SiO_x layer near the pyramid valleys to become more conducting than the pyramid tips or faces. The preferential conduction of the SiO_x layer near pyramid valleys is an interesting result since it shows that by controlling the surface morphology one can engineer the eventual pinhole formation process in the SiO_x layer in such contacts, which is otherwise a random process.

4.6. Acknowledgements and Funding

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CHAPTER 5

MODIFICATIONS OF TEXTURED SILICON SURFACE MORPHOLOGY AND ITS EFFECT ON *Poly*-Si/SiO_x CONTACT PASSIVATION

Modified from a future paper

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In Chapter 4, we speculated that the microscopic random pyramidal textured Si surface morphology with its sharp tips and valleys, and the nanoscale roughness over the pyramidal faces are the reasons for the poorer passivation on a textured surface using *poly*-Si/SiO_x contacts. We further showed that a simplistic reoptimization of the contact processing conditions does not lead to a more efficient solar cell on a textured surface. Hence, modification of the pyramid morphology is needed to improve passivation, and has been demonstrated by etching of a textured Si surface with isotropic etching solutions, such as HF:HNO_3 [151-154, 167]. However, details regarding the interdependence of etching conditions and resulting surface morphology are lacking. Here, we investigate the effect of HF:HNO_3 solution etching paramaters on the etch-rate and surface morphology of a textured Si surface. We further show that etching affects the microscopic pyramidal shape, dominant crystallographic orientation, and the nanoscale roughness of the surface. These surface changes improve the *poly*-Si/SiO_x contact passivation.

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5.1. Abstract

High-efficiency crystalline silicon (*c*-Si) solar cells require textured surfaces for efficient light trapping. However, passivation of a textured pyramidal surface to reduce carrier recombination is challenging due to the presence of sharp tips, edges, and valleys. Using electrical and surface microscopies combined with lifetime measurements, we report on the effect of $HF:HNO_3$ etching on the pyramidal textured Si surface morphology, and on *poly*-Si/SiO_x contact performance. Preferential rounding of either the valleys between pyramids, or the pyramid tips is obtained depending on the $HF:HNO_3$ solution temperature. Both these morphologies make the pyramid shape irregular, with the pyramid faces no longer being predominantly a Si(111) surface. Our atomic force microscopy measurements further show that the nanoscale roughness over the pyramid face also reduces after $HF:HNO_3$ etching. Thus, etching affects the microscopic pyramidal shape, dominant crystallographic orientation, and the nanoscale roughness of the surface. We speculate that these three surface effects result in improvement of surface passivation via *poly*-Si/SiO_x contacts. However, this improved passivation is accompanied by increased reflectance of the $HF:HNO_3$-etched textured surface. Finally, our electron-beam-induced current measurements reveal SiO_x thickness nonuniformities on the $HF:HNO_3$-etched textured Si surface: SiO_x is thicker near the pyramid tips, edges, and faces as compared to near the valleys between pyramids. This nonuniformity in the SiO_x layer may explain the poorer passivation obtained on a KOH-textured and $HF:HNO_3$-etched textured surface as compared to a planar surface.

5.2. Introduction

Solar energy is a prime candidate for meeting future world energy demands, and Si photovoltaics (PV) is the leading technology dominating the solar market. The Si PV technology

is constantly evolving with cheaper manufacturing processes and more efficient solar cells. Numerous cell architectures have already resulted in cell efficiencies >25% [61, 68, 137], with the current record being 26.7% [69]. These ultrahigh-efficiency Si solar cell architectures are enabled by excellent surface and contact passivation. In these architectures, the monocrystalline Si (*c*-Si) surface is passivated with either hydrogenated amorphous Si (*a*-Si:H) [58], or polycrystalline silicon (*poly*-Si) with ultrathin, 1–2 nm, SiO_x layers [70, 74, 113, 116, 127]. In addition to surface passivation, excellent light-trapping is also crucial for the highest efficiency *c*-Si solar cells, which is usually achieved by surface texturing of a Si(100) wafer using a KOH-based wet chemical etching process [43]. The resulting surface texture has 1–10 μm wide regular equilateral square pyramids with their edges along the Si(110) direction and their faces along the Si(111) plane. This texturing process thus affects both the morphology and the crystallographic orientation of the *c*-Si surface. While enhanced light trapping in the solar cell is achieved by such a textured surface, it also leads to enhanced carrier recombination, and this effect has been observed for different Si solar cell technologies [79, 124, 151-153, 168-171].

An unavoidable reason for increased recombination on a textured surface as compared to a planar surface is the increased surface area by a factor of ~1.7 due to the pyramidal morphology. However, this alone does not explain the ~10 times increased emitter recombination current density, J_o which has been observed for *poly*-Si/SiO_x passivated contacts [79]. The increased recombination can instead be related to three other factors. First, there is a higher defect density at the SiO_x/*c*-Si interface [79-81], for a Si(111) crystallographic orientation on a textured Si surface instead of Si(100) orientation on a planar surface. Second, there is increased film stress and nonuniform growth of the passivation layers on the tips, edges, and valleys of a textured surface compared to a planar surface [151, 168, 169]. Additionally, a rarely discussed third effect is the

increased recombination due to nanoscale roughness over the pyramidal surface morphology [170, 172]. Apart from these general effects, there are certain other effects that are more specific to particular cell architectures. For cells with diffused emitters, poor passivation has been related to nonuniform dopant diffusion profiles over the textured surface [171]. For cells based on *a*-Si:H layers, the poorer passivation has been related to epitaxial growth of the *a*-Si:H layers near the pyramid valleys [152]. For cells with *poly*-Si/SiO_x passivated contacts, poor passivation has been related to increased defects at the SiO_x/Si(111) interface [79]. Therefore, processing strategies are required to improve the performance of passivated contacts on textured surfaces.

It has been shown that a polishing etch of a textured *c*-Si surface results in improved passivation irrespective of the cell architecture [151-154, 167]. The most commonly used polishing etch is based on HF:HNO_3 solution, which is known to etch Si isotropically [173, 174]. Etching occurs through the continuous oxidation of the Si surface via HNO_3, and simultaneous etching of the oxidized Si surface via HF. Subjecting pyramidal textured Si wafers to such an etch usually leads to preferential rounding of the pyramid tips [152, 154, 167]. However, in certain cases, preferential rounding of the valleys between pyramids has also been observed [151]. The reason for two different morphological changes obtained using similar etching solutions is however not clear and, therefore, controlled experiments are needed on a textured surface to understand the role of other parameters during etching, such as etching temperature, and the extent of solution agitation.

Here, we show that based on the temperature of HF:HNO_3 solution, we can preferentially round either the valleys between pyramids, or the pyramid tips. Both these morphologies make the pyramidal shape irregular with the pyramid faces no longer being predominantly a Si(111) surface. Our atomic force microscopy (AFM) measurements further show that the nanoscale roughness

over the pyramid face also reduces after etching the textured surface with $HF:HNO_3$ solution. Using *poly*-Si/SiO_x contacts, we demonstrate improved passivation on pyramidal morphologies with either rounded tips or rounded valleys as compared to a KOH-textured Si surface. However, this improved passivation is accompanied by increased reflectance of the polished textured surface. Finally, electron-beam-induced current (EBIC) measurements show that irrespective of the surface morphology, the SiO_x layer within a *poly*-Si/SiO_x contact is thicker near the pyramid tips, edges, and faces as compared to that near the valleys between pyramids.

5.3. Experimental Details

Experimental details of sample processing and characterization are described below.

5.3.1. Etching conditions to modify Si surface and characterization using SEM and AFM

Etching experiments were performed on double-side-polished (DSP), phosphorous-doped, ~280 μm thick, float zone Si(100) and Si(111) wafers with resistivities of 3.8 and 3.4 Ω·cm, respectively. Additional experiments were also performed on ~170 μm thick double side textured (DST) wafers. The DST wafers were prepared by a KOH-based texturing etch of as-sawn, phosphorous-doped, ~195 μm thick, *n*-type Czochralski (*n*-Cz) Si(100) wafers with a resistivity of 3 Ω·cm. All the DST wafers used in this study were etched in the same solution, and showed very similar surface morphology. These wafers were then further etched with different chemistries. For alkaline-based etching, the wafers were etched in 25% tetramethylammonium hydroxide (TMAH) solution at a temperature of 75 °C for 30–180 s. The solution was agitated using a magnetic stirrer, which was set to a speed of 600 rpm. For acid-based etching, the wafers were etched in 1:20 $HF:HNO_3$ solution. Etching was performed for 10–360 s, at stirring speeds of 50–400 rpm, and over the temperature ranges of 2–6 and 40–42 °C. Temperature was measured via a

thermocouple, and was controlled by placing the Teflon beaker containing the $HF:HNO_3$ solution either in an ice bath or a water bath at the appropriate temperature. Etch rates were then determined by measuring the change in weight of a 2.5×2.5 cm *c*-Si piece after etching.

Scanning electron microscopy (SEM) of the etched wafers was performed using a JEOL 7000F SEM at an accelerating voltage of 2 kV. AFM measurements were performed in the tapping mode using an Asylum Research MFP-3D atmospheric AFM with an Al-coated Si tip (BudgetSensors Tap190-G). Phase maps were also acquired during the topography measurement. The samples were mounted on a stage at an angle of 55° with respect to the AFM stage to ensure that the pyramid face was perpendicular to the AFM tip. The AFM measurements were performed a few micrometers from the top edge of the sample.

5.3.2. Fabrication of symmetric test structures with *poly*-Si/1.5 nm SiO_x layers

The DST wafers were cleaned using standard wafer cleaning procedures of piranha, Radio Corporation of America (RCA)-1, and RCA-2 [128, 129] after etching with the $HF:HNO_3$ solution. The wafers were then subjected to dry thermal oxidation at nearly atmospheric pressure in a quartz tube furnace at a N_2-to-O_2 gas flow ratio of 6:1 at 700 °C for 5 min. The SiO_x thickness measured with spectroscopic ellipsometry on a reference polished Si(100) wafer was ~1.5±0.05 nm, but could not be measured on the textured surface. Boron-doped *a*-Si:H was then deposited on both sides of the oxidized *c*-Si wafers using a SiH_4/H_2 capacitively-coupled, radio-frequency plasma powered at 13.56 MHz. The flow rates of SiH_4, H_2, and B_2H_6 (2.6% in H_2) were 2, 100 and 1 standard cm^3/min (sccm), respectively. The *c*-Si wafer was placed on the grounded substrate holder at a temperature of 250–350 °C with an input power to the plasma source of 8 W to grow a ~50 nm thick *a*-Si:H layer. The resulting samples were then annealed at 850 °C for 30 min in a quartz

tube furnace under N_2 atmosphere to convert *a*-Si:H to a *poly*-Si layer via solid-phase crystallization. This was followed by atomic layer deposition of Al_2O_3 using trimethylaluminium and H_2O as precursors at a substrate temperature of 200 °C followed by annealing in forming gas (1:9 H_2:N_2 mixture) at 400 °C for 60 min. Quasi-steady-state photoconductance decay measurements were then performed using a Sinton lifetime instrument (WCT-120) to extract the implied open circuit voltage (i-V_{oc}) [106]. Reflectance measurements were performed on the symmetric *poly*-Si/SiO_x/*c*-Si samples using a Variant Cary 6000i UV-Vis-NIR spectrophotometer with a DRA-1800 diffused reflectance accessory.

5.3.3. Fabrication of test structures with *poly*-Si/2.2. nm SiO_x layers on front and rear sides and their characterization with EBIC

The DST wafers subjected to different acid-based etches were cleaned using standard wafer cleaning procedures of piranha, Radio Corporation of America (RCA)-1, and RCA-2 [128, 129]. The wafers were then subjected to dry thermal oxidation at nearly atmospheric pressure in a quartz tube furnace at a N_2-to-O_2 gas flow ratio of 6:1 at 800 °C for 10 min. The SiO_x thickness measured with spectroscopic ellipsometry on a reference polished Si(100) wafer was ~2.2±0.05 nm, but again could not be directly measured on the textured surface. A ~40 nm thick intrinsic (*i*) *a*-Si:H film was then plasma deposited on both sides of the oxidized wafer using similar conditions as in Section 5.3.2, and the samples annealed at 1050 °C for 30 min in N_2. Following a treatment with 10% aqueous HF solution, doped *a*-Si:H films were then deposited on either side to form a n^+ *a*-Si:H/*i* *poly*-Si/SiO_x/*n*-Si/SiO_x/*i* *poly*-Si/p^+ *a*-Si:H structure. For deposition of p^+ *a*-Si:H the plasma deposition conditions were the same as in Section 5.3.2, whereas for phosphorous doped n^+ *a*-Si:H layer, 1 sccm of PH_3 (3% in H_2) was introduced into the plasma deposition chamber instead of B_2H_6. The samples were then annealed in N_2 at 850 °C for 30 min to form a

n^+ *poly*-Si/SiO_x/*c*-Si/SiO_x/p^+ *poly*-Si structure. Subsequent processing steps of Al_2O_3 deposition and forming gas anneal were similar to those described in Section 5.3.2. The samples were then treated with 1% aqueous HF solution to remove the Al_2O_3 layer. Metallization was performed by thermally evaporating Ag at a base pressure of ~10^{-7} Torr in a Temescal FC-1800 metallization tool. Metal contacts consisting of a ~4 nm thick Ti adhesion layer followed by ~1 μm thick Ag layer were formed on both sides of the test structure for EBIC measurements. EBIC measurements were performed on the n^+ *poly*-Si side of these test structures using a JEOL JSM-7600 FESEM and Mighty EBIC quantitative EBIC setup. An electron-beam accelerating voltage of 5 kV and ~5 nA beam current were used for the EBIC measurements.

5.4. Results and Discussion

Experimental results regarding changes in textured Si surface morphology due to etching and its effects of contact performance are provided and discussed below.

5.4.1. Effect of TMAH etching on pyramidal surface morphology

We first investigated how the pyramid morphology is affected by etching in a basic medium [175]. In basic solutions such as KOH and TMAH, Si etches anisotrpically, and this type of etching is used to texture the surface of a Si(100) wafer. However, under certain etching conditions basic solutions can also be used to planarize the *c*-Si surface. Figure 5.1 shows the SEM images of a KOH-etched textured Si surface, before and after etching in a 25% TMAH solution at 75 °C for different durations. Under these condtions we have determined that we can planarize a pyramidal Si surface. In Fig. 5.1a, prior to TMAH etching, the pyramid (100) tips, and valleys, (110) edges, and (111) faces are clearly visible. Figs. 5.1b–1e show that the surface morphology is modified quite significantly after etching the textured wafer with TMAH solution, and this

surface no longer resembles the one in Fig. 5.1a. Many sharp features are also visible which seems consistent with anisotropic etching with TMAH soluion. However, this etch process modifies the crystallographic orientation of the pyramidal features exposing surfaces other than the Si(111) faces obtained after KOH texturing [175]. While we can see in the SEM images in Fig. 5.1 that after 180 s the surface indeed becomes more planar with wider valleys, we can also see that this etch process does not round off the pyramid tips. Since these pyramid tips may be responsible for the poor passivation of the surface *poly*-Si/SiO_x contacts, this strategy was not considered ideal for improving the contact performance.

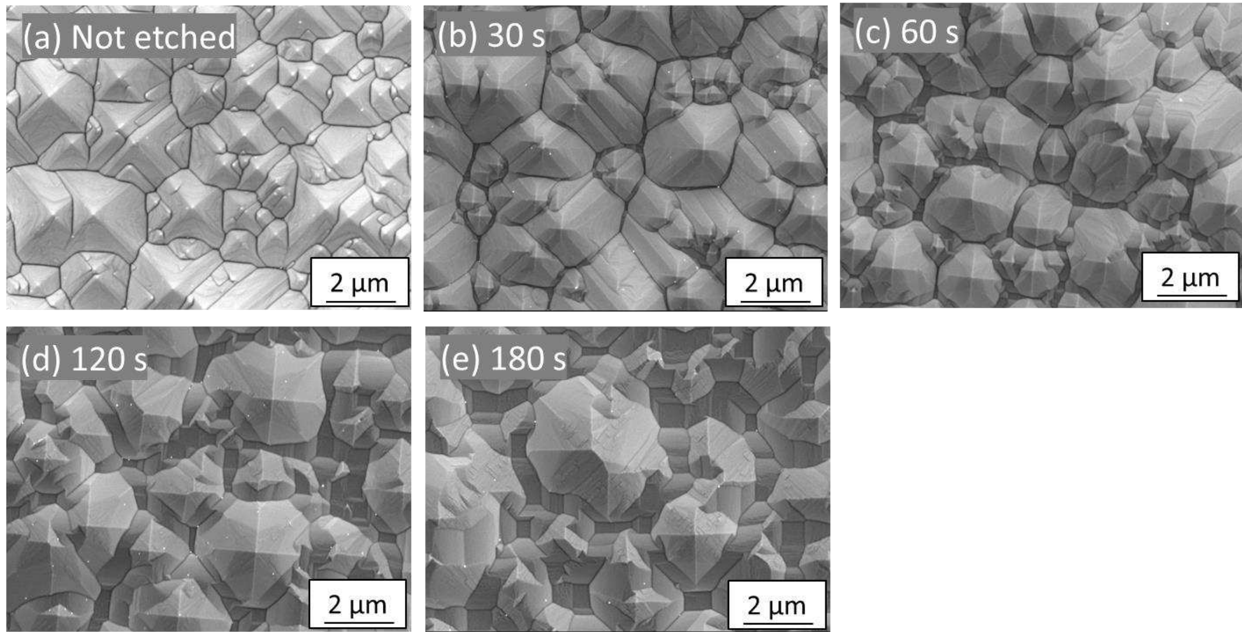

Figure 5.1 Plan-view SEM images of (a) a KOH-textured Si wafer, and after the textured wafer was etched with 25% TMAH at 75 °C for (b) 30, (c) 60, (d) 120, and (e) 180 s. The stirrer speed was 600 rpm.

5.4.2. Effect of HF:HNO_3 etching conditions on pyramidal surface morphology

Previous studies have demonstrated rounding of pyramid tips using a HF:HNO_3 solution [152, 154, 167]. Isotropic etching of Si using HF:HNO_3 based solution depends on a number of

parameters such as composition of the solution, presence of diluents (e.g., H_2O, CH_3COOH, etc), temperature, and degree of agitation of the solution [173]. However, the influence of these parameters on the etch rate and the resulting morphology of a textured silicon surface is not well studied. In Table I we list the etch rate of Si wafers with different crystallographic orientations and surface morphology etched with a 1:20 HF:HNO_3 solution. The increasing etch rate of both, DSP Si(100) and DSP Si(111) wafers with increasing stirrer speed shows that this etching reaction is limited by the transport of reactive species to the surface of the Si wafer. This is consistent with previous studies which have shown that the HF:HNO_3 etching reaction is transport limited [174]. From the data in Table 5.1, it can also be seen that the etch rate for the DSP Si(100), DSP Si(111), and DST wafers increases when the solution temperature is increased from ~2–6 to 40–42 °C. Since, the etching of Si using a HF:HNO_3 is an exothermic reaction [173], it is important to constantly monitor and control the temperature of the solution for reproducible etching. The data in Table 5.1 further shows that the etch rates of DSP Si(100), DSP Si(111), and DST wafers were similar, ~1.7 μm/min, at ~5 °C. The similar etch rates for the DSP Si(100) and Si(111) wafers are expected due to isotropic Si etching with HF:HNO_3 solution [173]. However, the similar etch rate for a DST and DSP wafer needs further discussion. It must be noted that for the data shown in Table 5.1, we calculated the etch rates based on mass change and by assuming the surface area of the textured wafer is the same as a polished wafer. This assumption was made because it is known that the surface area of a textured wafer changes with increasing etch time due to modification of the surface morphology [167], making it difficult to accurately account for the changing surface area as etching proceeds. Since, the initial pyramidal textured Si surface has ~1.7 times more surface area than a polished wafer, we are overestimating the etch rate of the textured wafer. We speculate that the apparent etch rates of the textured and polished wafers are similar at 2–6 °C

because the etching reaction is transport-limited due to the formation of a boundary layer at the wafer surface. If this boundary layer is much thicker than the 2–3 μm size range of the pyramids, the boundary layer surface area will be similar for planar and textured wafers. Lastly, when the etching solution temperature is increased to ~40 °C, the etch rate of the DST wafer is lower than the DSP wafers. Below we discuss how these different etching temperatures affect the morphology of the textured Si surface. Since, stirring speed affects etch rate, for all subsequent etching experiments, we used a stirrer speed of 400 rpm unless specified otherwise.

Table 5.1 Etch rate of silicon with different crystallographic orientation and surface morphology for different etching conditions using 1:20 HF:HNO_3 solution.

Stirrer speed	Si etch rate (1-sided) (μm/min)					
	DSP Si(100)		DSP Si(111)		DST	
	2–6 °C	40–42 °C	2–6 °C	40–42 °C	2–6 °C	40–42 °C
50	-	3.34	-	3.10	-	-
200	-	4.45	-	4.35	-	-
400	1.70	4.87	1.65	4.78	1.65	3.70

Figure 5.2 shows the SEM images of a textured Si wafer etched with HF:HNO_3 solution maintained within a temperature range of 2–6 °C for different etch times. SEM images were obtained both in the plan-view and with the sample tilted at 45° to better visualize the changes in morphology. No significant change in the pyramidal morphology is observed for the shortest etch time of 10 s (see Fig. 5.2a). While the pyramid tips and valleys still appear sharp, the edges along Si(110) direction, where two pyramidfaces intersect, seem slightly flatter. When the etching time is increased to 60 and 120 s (see Figs. 5.2b and 5.2c respectively), the tips of the pyramids seem flatter. This is referred to as rounding of the pyramid tips, and reduces the surface area in the tip reagion. The valleys between the pyramids do not seem to undergo any visual change with increasing etch time. The SEM images acquired when the sample is tilted at 45° (see Fig. 5.2d–f)

further show that it is not only the pyramid tips that are being rounded, but the entire pyramid seems to have a smaller height-to-base ratio. To quantify this, in the images where the sample was titlted by 45°, we measured the angle at the pyramid tip between two pyramidal edges, for the pyramidal face closer to the detector for the SEM (see Figs. 5.3d–f). The measured angles were ~64°, ~84°, and ~82° for etching times of 10, 60, and 120 s respectively. This clearly indicates a change in the pyramid height-to-base ratio. An important point to note from this is that these pyramids are no longer equilateral square pyramids, and hence, geomerically the pyramid faces cannot be the Si(111) crystallographic surface after HF:HNO_3 etching.

Figure 5.3 shows the SEM images of a textured Si wafer etched with HF:HNO_3 solution maintained within a temperature range of 40–42 °C for different etch times. Again, SEM images were obtained both in the plan-view and with the sample tilted at 45°. Similar to the SEM image in Fig. 5.2a, pyramid edges along Si(110), where two faces of a pyramid intersect, seem slightly wider after a short etch time of 10 s (see Fig. 5.3a). Also, the valleys between two pyramids appear slightly wider. When the etching time is increased to 30 and 60 s (see Figs. 5.3b and 5.3c, respectively), significant rounding of the valleys between pyramids is observed, again reducing the surface area. The pyramid tips remain sharp and do not become more rounded, as was observed when these samples were etched at a lower temperature range of 2–6 °C (see Figs. 5.2b and 5.2c). The SEM images acquired when the sample is tilted at 45° (see Fig. 5.3d–f) further show that the pyramid seems to have a smaller height-to-base ratio. As previously described, we quantified this by measuring the angle at the pyramid tip between two pyramidal edges, for the pyramidal face closer to the detector for the SEM. The angles are ~64°, ~64–78°, and ~78–100° for etching times of 10, 30, and 60 s respectively. Since these are no longer equilateral square pyramids, the pyramid face cannot be a Si(111) surface. Hence, due to etching of a pyramidal textured Si surface with

$HF:HNO_3$ solution, not only the pyramidal shape, but the crystallographic orientation of the surface also changes. We would like to point out that similar experiments were also performed at stirring speeds of 50–400 rpm at 40–42 °C. However, the change is surface morphology was not significant, and the pyramid valleys were preferentially rounded for all sitrring speeds.

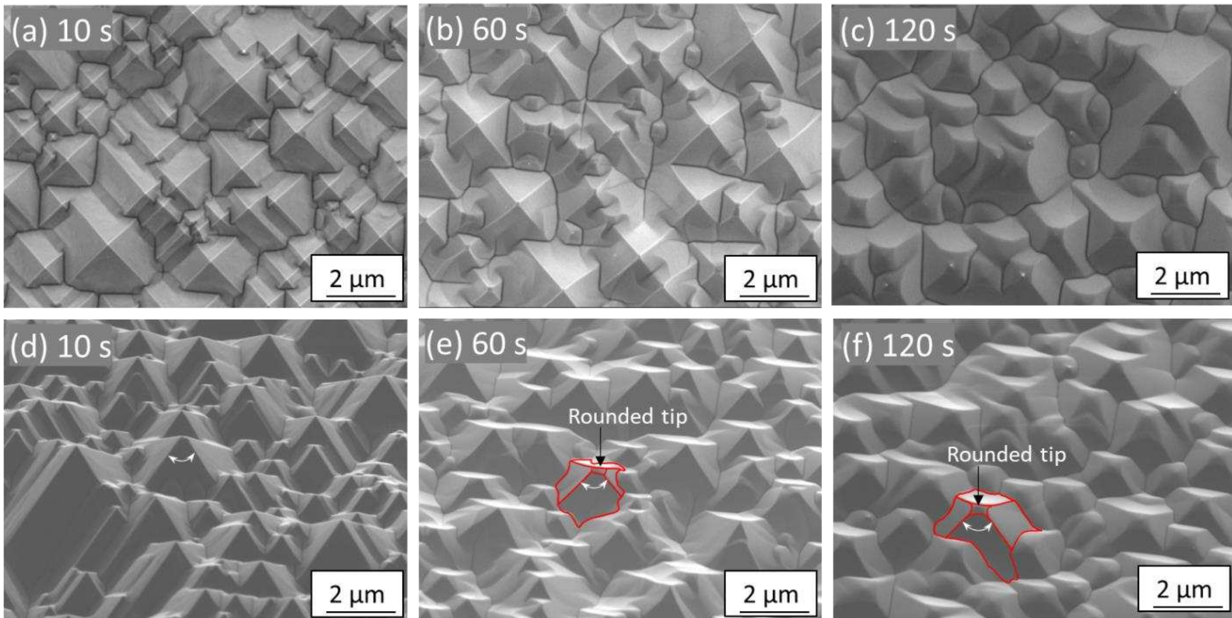

Figure 5.2 Plan-view SEM images of a textured Si wafer etched with 1:20 $HF:HNO_3$ solution maintained at 2–6 °C, and at a stirrer speed of 400 rpm for (a) 10, (b) 60, and (c) 120 s. (d–f) Corresponding SEM images of samples in "a–c" with the sample tilted at 45°. In "e" and "f", one pyramid is outlined for easier visualization of the pyramid tip and the faces. The double-arrowed curve in d-f shows the angle measured near the pyramid tip.

From Figs. 5.2 and 5.3 we have determined how etching temperature affects the microscopic pyramidal surface morphology, the crystallographic orientation of the surface, and surface area. However, it is also important to determine the nanoscale roughness of the surface, since it can affect the electronic properties of the *c*-Si/SiO_x interface [161]. In the SEM image of the KOH-etched textured surface (see Fig. 5.4a) we see numerous ridge-like features on the pyramidal Si(111) face, resulting in nanoscale roughness. These ridges are not observed after etching the wafer with $HF:HNO_3$ solution for 10 s at both ~5 and ~40 °C (see Figs. 5.4b and 5.4c,

respectively). All the SEM images were acquired at a low accelerating voltage of 2 keV for enhanced resolution of the surface morphology. To quantify the extent of the change in nanoscale roughness due to etching, we performed AFM measurements over the pyramidal Si(111) face. The textured wafers were mounted at an angle of ~55° during the measurement to align the pyramid face perpendicular to the AFM tip, as schematically shown in Fig. 5.4d. Figures 5.4e–g show the 2D rendition of the surface topography of the samples shown in Figs. 5.4a–c, respectively. It must be noted that the scanned regions in Figs. 5.4e–g, are not arbitrary regions on the pyramid surface. These regions were identified by first performing a large area (5×5 μm) scan as shown in Fig. 5.4h. A region lying entirely on the pyramid Si(111) face was then scanned, as has been illustrated by the boxed rectangle in the phase contrast image in Fig. 5.4h. From the topography maps of the pyramidal Si(111) face we can infer that the pyramid face on the samples etched with HF:HNO_3 (see Figs. 5.4f and 5.4g) become smoother compared to the surface obtained after KOH etching (see Fig. 5.4e). The surface roughness quantified by the standard deviation of the z-axis height in these maps decreases from 0.68 nm on the KOH-etched sample to 0.35 and 0.27 nm for the samples etched with HF:HNO_3 at 2–6 and 40–42 °C, respectively. To summarize, our results show that for the same concentration of HF:HNO_3 solution, by varying the etching temperature, the etch rates and the resulting surface morphology of a textured Si surface is affected to obtain either preferential rounding of pyramid tips or valleys. The etching also affects the crystallographic orientation, nanoscale roughness, and area of the surface. Below we discuss how these different morphologies affect passivation with and carrier-conduction through *poly*-Si/SiO_x passivated contacts.

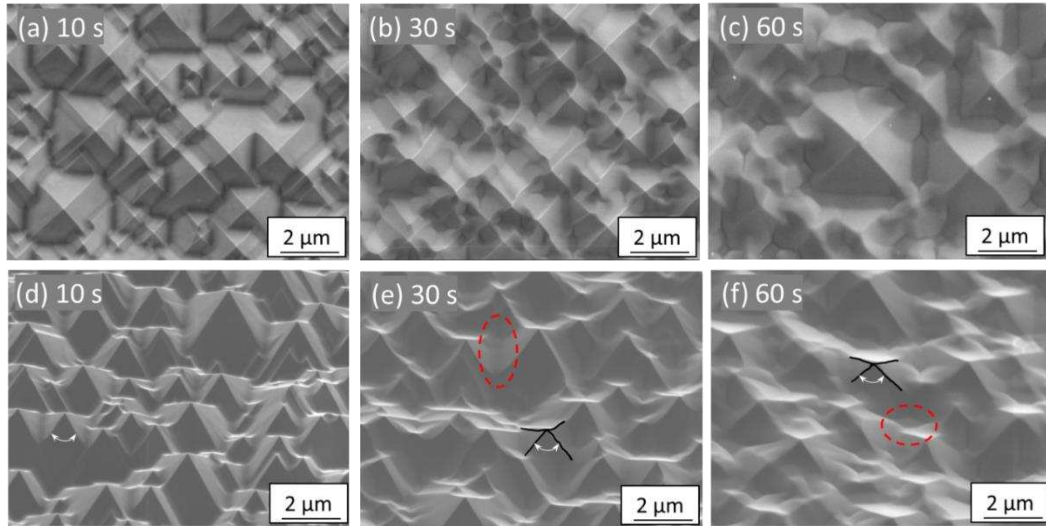

Figure 5.3 Plan-view SEM images of a textured Si wafer etched with 1:20 HF:HNO_3 solution maintained at 40–42 °C, and at a stirrer speed of 400 rpm for (a) 10, (b) 30, and (c) 60 s. (d–f) Corresponding SEM images of samples in “a–c” with the sample tilted at 45°. In e and f, the edges of one pyramid (black color) and a rounded valley (red color) are outlined for easier visualization. The double-arrowed curve in d-f shows the angle measured near the pyramid tip.

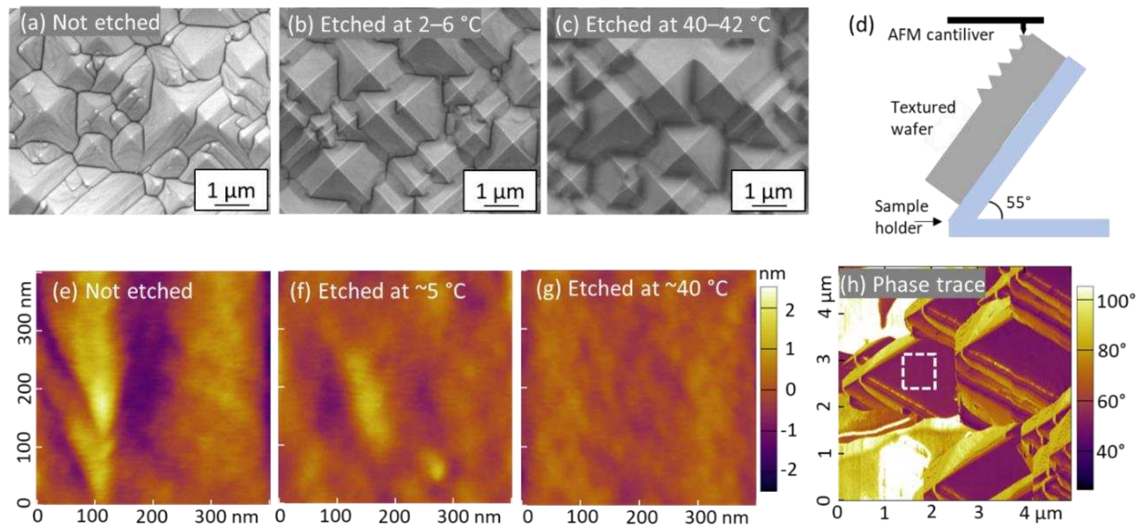

Figure 5.4 Plan-view SEM image of (a) a KOH-textured Si surface, and after the textured wafer was etched in a 1:20 HF:HNO_3 solution for 10 s at (b) 2–6 and (c) 40–42 °C. (d) Schematic of sample mounting for the AFM measurement. (e–g) 2D rendition of the AFM topography image of the pyramidal Si(111) facet corresponding to the samples shown in “a–c”. The standard deviation of the height (z-axis of each image) in figures “e–g” was 0.68, 0.35, and 0.27 nm, respectively. (h) Phase map of the pyramidal textured Si wafer measured with the Si wafer mounted at an angle of ~55° with respect to the AFM stage. The box illustrates an example of a scanned region on a pyramidal face for determining the nanoscale roughness.

5.4.3. Effect of surface morphology on *poly*-Si/SiO_x contact passivation

We studied the effect of surface morphology with either rounded tips or valleys on *poly*-Si/SiO_x contact passivation on HF:HNO_3-etched textured wafers, which were etched for 5–60 s at either 2–6 or 40–42 °C. As a control, test structures were also made on the KOH-textured wafers. Figure 5.5a shows the relation between i-V_{oc} and reflectance at 600 nm of symmetric p^+ *poly*-Si/SiO_x test structures on these wafers for different etch times. The i-V_{oc} increases as the reflectance of the wafer increases, since the surface becomes more planar. Similar i-V_{oc} and reflectance values were obtained irrespective of preferential rounding of pyramid tips or valleys. Therefore, we can conclude that rounding of pyramid tips or valleys has a very similar effect on the quality of passivation obtained for *poly*-Si/SiO_x contacts. However, the improvement in passivation cannot be strictly attributed to the rounding of pyramid tips or valleys because the pyramid shape, surface orientation, surface area, and nanoscale surface roughness change simultaneously due to etching with HF:HNO_3 solution, as described in Section 5.4.2. Additionally, we speculate that passivation might be different for contacts with *a*-Si:H layers due to epitaxial growth near the pyramid valleys [152]. Hence, changing the area fraction of pyramid valleys might affect passivation from *a*-Si:H layers differently. Figure 5.5b shows the reflectance spectra of the samples in Fig. 5.5a. As reference, we also show the reflectance spectra of a test structure on a planar Si surface. The reflectance at 600 nm increases quite significantly, from ~12% for a KOH-etched textrued wafer, to ~16% for a textured wafer etched with HF:HNO_3 solution at 40–42 °C for 5 s. This increased reflectance makes the HF:HNO_3-etched surface morphology unsuitable for light-trapping at the front side of a Si solar cell. However, the lower reflectance of the HF:HNO_3-etched morphology as compared to that of a planar Si surface over the 1000–1200 nm range might make the HF:HNO_3-etched morphology suitable for the rear side of Si solar cells.

More detailed work, as described in McIntosh et al. [176], needs to be performed to evaluate the benefits of a HF:HNO_3-etched textured surface as a back surface for Si solar cells.

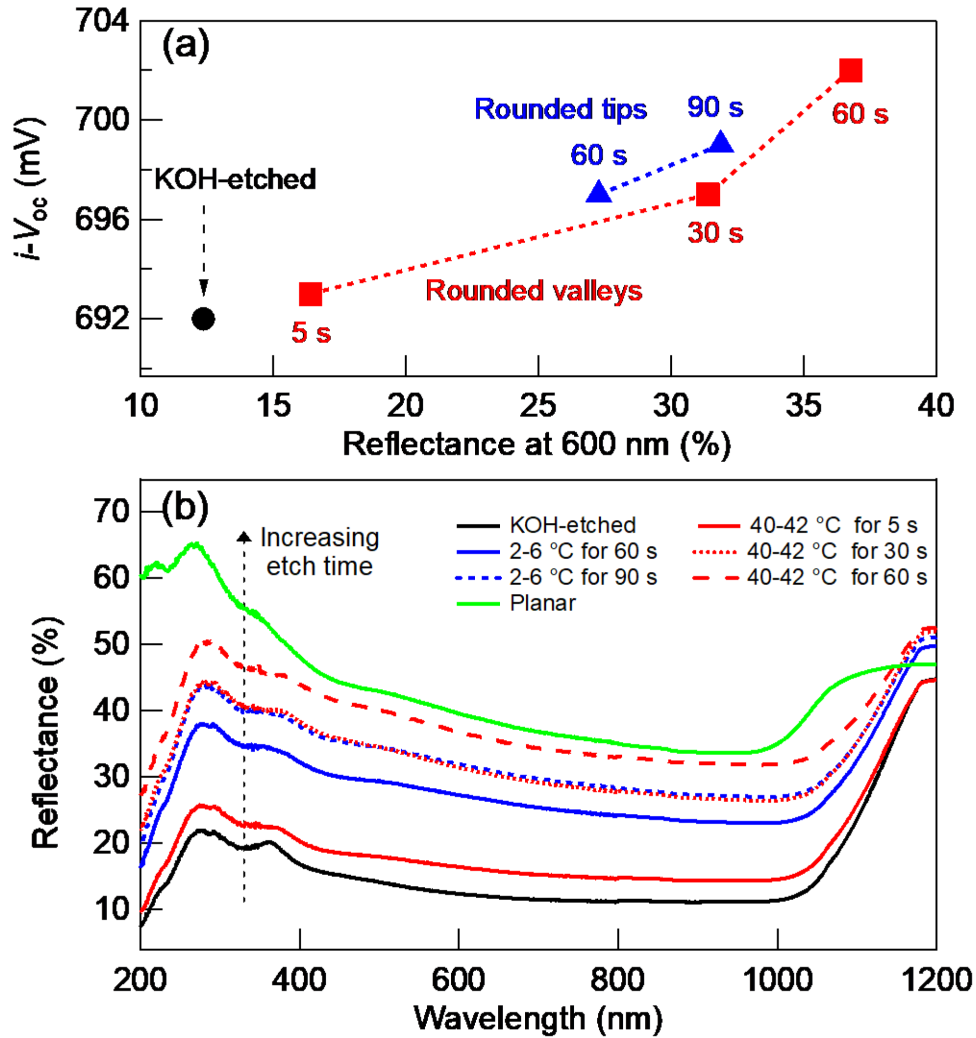

Figure 5.5 (a) *i*-V_{oc} for symmetric p^+ *poly*-Si/1.5 nm SiO_x/*n*-Cz structures on textured Si wafers with different reflectance. Textured Si wafers were etched in 1:20 HF:HNO_3 solution for different times of 60 and 90 s at 2–6 °C (▲) or 5, 30, and 60 s at 40–42 °C (■) resulting in varying reflectance. (b) Reflectance spectra of the samples in “a”. Reflectance spectra of a symmetric p^+ *poly*-Si/1.5 nm SiO_x/*n*-Cz sample on a planarized Si surface is also shown as a reference in green.

5.4.4. Effect of surface morphology on uniformity of SiO_x layer thickness

To investigate the effect of surface modifications on the uniformity of the SiO_x layer, we performed EBIC measurements of *poly*-Si/SiO_x contacts. The oxidation conditions used to grow the SiO_x layer within the *poly*-Si/SiO_x/*c*-Si structure resulted in a ~2.2 nm thick SiO_x layer on polished Si(100) wafer, but could not be determined via ellipsometry on the textured and HF:HNO_3-etched samples. *Poly*-Si/SiO_x contacts with a ~2.2 nm thick SiO_x layer are non-conductive [113], but become conductive after annealing the *poly*-Si/SiO_x contact to temperatures >1000 °C. The high temperature causes the SiO_x layer to locally thin down and/or break-up [125], forming what are sometimes referred to as "pinholes" [64, 75]. These pinholes enable conduction between the *poly*-Si layer and the underlying *c*-Si wafer, and can be characterized using EBIC. The signal intensity in EBIC images results from the separation of electron-hole pairs generated by the electron beam within a SEM and subsequent collection of these excited carriers, which results in a current that is mapped over the scanned region [112]. Since the EBIC collection efficiency is significantly higher near a conduction-enabling pinhole than near a region with an insulating, pinhole-free SiO_x layer, these pinholes can be accurately mapped with EBIC [64]. Furthermore, we have previously shown in Section 4.4.4 that the pinholes preferentially form near the valleys between pyramids on a textured Si surface for *poly*-Si/SiO_x contacts with the ~2.2 nm SiO_x layer. *Poly*-Si/SiO_x contacts with the tunnelling ~1.5 nm SiO_x layer do not show any SiO_x related EBIC features due to the uniform tunnelling nature of the ~1.5 nm thick SiO_x layer. Thus, pinhole type *poly*-Si/SiO_x contacts, with >1.7 nm thick SiO_x layer, combined with EBIC measurements are a valuable tool to investigate conduction, and indirectly the thickness nonuniformities in the SiO_x layer. After comparison of EBIC maps with the

corresponding SEM image, we can relate these nonuniformities to morphological features on a textured Si surface.

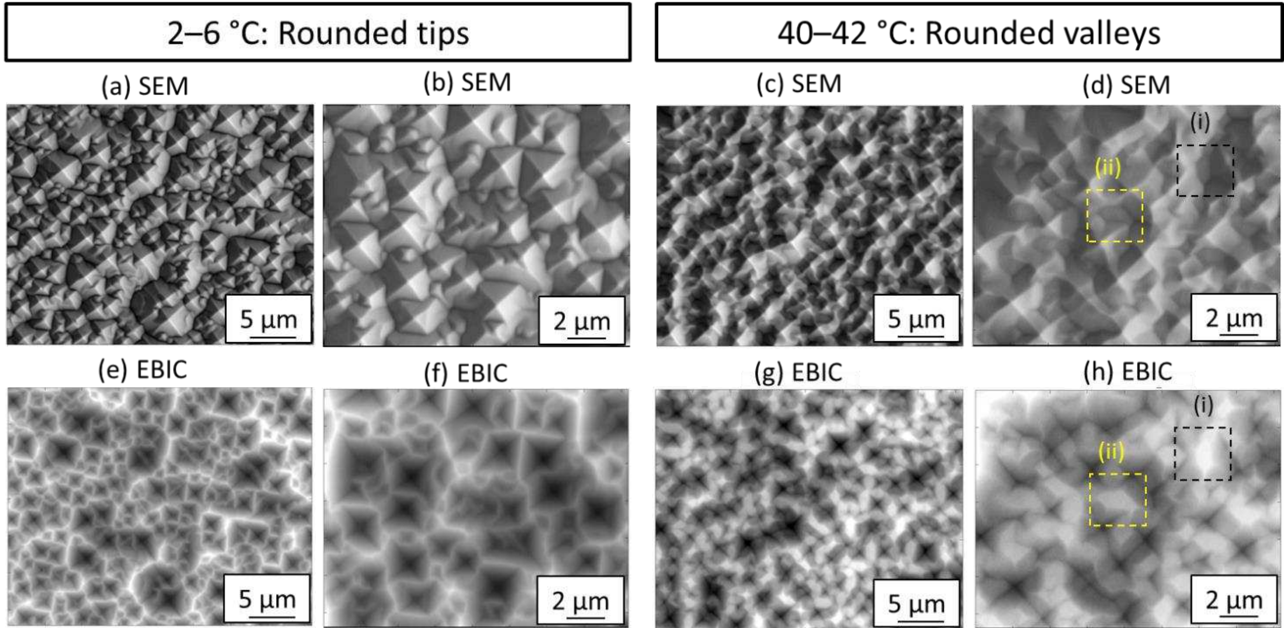

Figure 5.6 Plan-view SEM images of a n^+ *poly*-Si/2.2 nm SiO_x contact on textured Si surface originally etched with 1:20 HF:HNO_3 solution for 60 s at (a, b) 2–6 and (c, d) 40–42 °C. (e–h) EBIC images corresponding to the regions shown in SEM images "a–d", respectively. The measurements were performed on test structures with *poly*-Si/SiO_x layers on the front and the back sides. Boxed regions "i" and "ii" in both "d" and "h" show regions with a rounded pyramid valley.

Figures 5.6a–b, and 5.6c–d show the SEM images of the surface of test structures with *poly*-Si/SiO_x contacts with preferentially rounded pyramid tips and valleys, respectively. Figures 5.6e–h show the corresponding EBIC images of the regions shown in Figs. 5.6a–d, respectively. In Figs. 5.6e and 5.6f, which correspond to the EBIC images of the sample with the rounded pyramid tips, only a few valleys between pyramids appear bright, while the pyramid faces, edges, and rounded tips appear significantly darker. These locations were unambiguously identified by comparing the EBIC maps (Figs. 5.6e and 5.6f) with their corresponding SEM images (Figs. 5.6a and 5.6b). Since, we have previously established that bright spots in EBIC correspond

to conducting, and hence thinner SiO_x regions (see Section 3.4.3), we can conclude that the SiO_x layer near the pyramid valleys is thinner as compared to that near the pyramid faces, edges and rounded tips. Furthermore, since not all valleys are equally bright (see Fig. 5.6e), we can infer that the SiO_x is not uniformly thin in the valleys. Similar to Figs. 5.6e and 5.6f, in Figs. 5.6g and 5.6h, which correspond to the EBIC images of the sample with the rounded valleys, some of the rounded valleys between pyramids appear bright, while the pyramid faces, edges, and tips are significantly darker. For easier visualization we have marked regions "i" and "ii" in both Figs. 5.6d and 5.6h, which correspond to two different regions where the valley is rounded. The EBIC image for region "i" in Fig. 5.6h is much brighter than that for region "ii", indicating that the SiO_x layer in region "i" is more conducting and hence thinner than that in region "ii". While there may be local variations in SiO_x thickness in the valleys, our EBIC measurements show that SiO_x near the pyramid valleys is on an average always preferentially thinner than near other pyramidal facets for both tip- and valley-rounded surfaces. Finally, we speculate that the SiO_x layer near the pyramid valleys either grows thinner during dry thermal oxidation, or forms pinholes more easily during the 1050 °C annealing step of a *poly*-Si/SiO_x/*c*-Si structure.

5.5. Summary and Conclusions

In conclusion, we have studied the effect of HF:HNO_3-etching parameters on the etch rates and surface morphology of polished and textured Si wafers. The etch rate depends on the extent of agitation of the etching solution, and hence, is an important parameter to consider for reproducible etching. Depending on the etching temperature, preferential rounding of pyramid tips or valleys of a pyramidal textured Si wafer can be achieved, which also reduces the surface area. Such a modification of the surface also makes the pyramid shape irregular, and hence, geometrically, the pyramid face is no longer a Si(111) surface. Apart from the microscopic

modifications to the pyramidal shape, the nanoscale roughness of the pyramids also decreases due to etching. We further show that while HF:HNO_3-etching of a textured surface results in improved passivation with *poly*-Si/SiO_x contact layers, it also results in increased reflectance. We observe a very similar passivation quality for a textured surface with rounded pyramid tips versus rounded pyramid valleys. Since, etching of a textured Si surface with HF:HNO_3 solution leads to simultaneous changes in pyramid morphology, surface area, surface orientation, and nanoscale surface roughness, it is difficult to isolate the reasons for the improved surface passivation with *poly*-Si/SiO_x contacts. Finally, our EBIC results show that the SiO_x layer grown on a textured Si surface has nonuniform thickness, with the SiO_x near the pyramid tips, edges and faces being thicker than that near the pyramid valleys. Since passivation from *poly*-Si/SiO_x contacts depends on SiO_x thickness, the increased rounding of pyramid valleys might result in a more uniformly SiO_x layer, thus leading to improved surface passivation. In the future, it would also be interesting to study how these different surface morphologies affect passivation with *a*-Si:H layers for Si heterojunction cells, since poor passivation from *a*-Si:H layers has been related to epitaxial growth near the pyramid valleys.

5.6. Acknowledgements and Funding

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CHAPTER 6

THERMAL STABILITY OF COPPER-NICKEL BASED CONTACTS FOR CRYSTALLINE SILICON SOLAR CELLS

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In Chapters 2–5, we invesitgated *poly*-Si/SiO_x contacts to enable high-efficiency next-generation Si solar cells. The improvement in efficiency may result in lower $/kWh cost of the final cell. However, another way to reduce the $/kWh of cells is to reduce the material costs. Current solar cell metallization relies on the Ag-paste firing process [177-180] [181, 182]. Ag is expensive and hence alternative metallization schemes involving the use of cheaper Cu metal have been proposed and evaluated [182-185]. However Cu is know to diffuse into Si, creating defects which are detrimental to solar cell efficiency [186-188]. Hence, Cu diffusion barrier interlayes between Si and Cu are needed [189]. In this chapter, we evaluate the potential of Ni and NiSi as Cu diffusion barrier layers [190, 191]. We demonstrate a simple one-step annealing process to form high-quality NiSi films on *c*-Si, and show that NiSi is a superior and thermally more stable barrier layer to Cu than Ni.

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6.1. Abstract

Electrodeposited Cu is a low-cost, low-damage alternative to Ag paste for front-side metallization of crystalline Si (*c*-Si) solar cells, but requires conductive diffusion barriers like Ni or NiSi. Thermal stability of these barriers during post-metallization anneal is critical for performance. In this study, we address the structural and chemical stability of Cu contacts with both Ni and NiSi barrier layers, identifying interfacial reactions responsible for their degradation. Superior thermal and chemical stability of single-phase NiSi barrier as compared to Ni is evidenced by XRD, Auger, and Raman spectroscopies. Moreover, the commonly used Cu-Ni-Si contact stack does not convert to more stable Cu-NiSi-Si stack upon thermal treatment. Instead, Cu readily alloys with the Ni layer and reacts with the underlying *c*-Si to form Cu_3Si, with no evidence for the formation of Ni_xSi phases. Also, even the superior NiSi barrier slowly dissolves into Cu at elevated temperatures.

6.2. Introduction

The current method for front-side metallization of crystalline Si (*c*-Si) solar cells is based on screen-printed Ag paste, which is subsequently fired at high temperatures, ~800 °C, to create a metal contact to the *c*-Si emitter that penetrates through the SiN_x anti-reflection coating and the Al_2O_3 passivation layer [47, 48]. However, Ag is expensive, the paste contains glass frit, organic binders, and solvents, and high-temperature firing results in performance losses [177-180]. The low metal density due to the presence of other constituents in the paste results in lower conductivity than that of pure Ag. Also, the morphology of the paste combined with the screen printing technique necessitates wider gridlines ≥ 50 µm, which result in more shadowing [181, 182], and the glass frit components result in recombination losses at the front of the cell [179]. An

industrially-attractive alternative to Ag paste is electroplated Cu, which allows for much finer, ~15 µm, and more conductive gridlines using a cheaper and more abundant metal [182-185]. Geissbuhler *et al.* have shown a 0.4% increase in absolute efficiency for a silicon heterojunction solar cell achieved via replacing the Ag paste front contacts with a transparent conductive oxide (TCO) and Cu plated contacts, primarily due to improvements in the fill-factor and the short-circuit current [182]. However, in standard *c*-Si solar cells such as the Al back surface field and the passivated emitter rear contact (PERC) cells, the metal grid is in direct contact with the Si wafer. Therefore, Cu contacts necessitate the use of a conductive diffusion barrier between Cu and the underlying *c*-Si absorber since Cu is known to diffuse into *c*-Si even at ambient temperatures, and forms recombination-active precipitates [186-188]. To address a similar issue in the microelectronics industry, metal silicides such as NiSi, Pd_2Si, $MoSi_2$, WSi_2, $TiSi_2$, $CoSi_2$ and PtSi have been used as interconnects and diffusion barriers [189]. For most of the above transition metals the desired metal silicide phase can be obtained by annealing a metal film deposited on *c*-Si over a specific temperature range. Amongst the various metal silicides, nickel monosilicide (NiSi) is preferred as it forms at a relatively lower temperature, consumes less Si, has lower resistivity, and grows most uniformly [190, 191].

Similar to all other transition metal silicides, nickel silicide also has many different phases which form depending on the annealing temperature of Ni films deposited on HF-cleaned *c*-Si wafers [192-194]. Generally, the Ni_2Si phase forms between 200–350 °C, NiSi between 400–550 °C, and $NiSi_2$ above 650 °C. Amongst these phases, NiSi has the lowest resistivity and therefore is the preferred phase for contact formation [192]. NiSi is usually formed using a two-step annealing process, which involves low-temperature annealing of a Ni film on *c*-Si to form Ni_2Si, followed by a piranha etch to remove the unreacted Ni, and a high-temperature annealing step to

convert Ni_2Si to NiSi. While this two-step methodology provides good control over the film thickness and results in single-phase NiSi films, the large number of steps involved make the processing of such contacts unattractive for solar cell production at an industrial scale. The NiSi process can be significantly simplified by direct annealing of Ni films on *c*-Si under NiSi formation conditions thus eliminating the need for the highly corrosive Piranha process and the lower temperature annealing step. This is referred to as the one-step annealing process [195], and has been investigated in this study.

The effectiveness of NiSi and Ni as a Cu diffusion barrier in *c*-Si solar cells has been studied using techniques such as Suns-open circuit voltage [196], current-voltage measurements [197, 198], and photoluminescence imaging [108, 199, 200]. The results from some of these studies that use solution-based Ni deposition are contradictory. While Bartsch *et al*. have shown that the Ni is an effective barrier for Cu [196], Flynn *et al*. have shown that Cu readily diffuses through the Ni layer and forms Cu_3Si precipitates [200]. These studies involve the use of solution-based Ni plating processes where certain impurities can be incorporated, which can lead to erroneous results [201, 202]. We further speculate that the above mentioned contradictory results have been obtained most likely due to the test devices being subjected to high-temperature thermal stress conditions for accelerated reliability determination, which affects film integrity. However, high-temperature thermal processing steps may be required in actual cell manufacturing, and this can be a serious reliability issue if these steps affect the integrity of Cu/Ni based contacts. For example, *p*-type, *c*-Si based, PERC cells have to be annealed to 100–200 °C to regenerate the cell efficiency loss that occurs due to light-induced degradation [203]. Another example is localized heating that occurs during soldering of contacts in *c*-Si based solar cells. Therefore, it is important

to understand the thermal stability of Cu/Ni and Cu/NiSi based contacts to access their feasibility in different *c*-Si based devices.

In this paper, we first report on the synthesis of NiSi using a two-step and a one-step annealing process. To ensure high film uniformity and purity, in our experiments we have used electron beam (*e*-beam) deposited Ni instead of Ni deposited via the electroless process. Using X-ray diffraction (XRD) and Raman spectroscopy we show that NiSi films grown using either a two-step or a one-step annealing method are structurally very similar. Second, we have compared the thermal stability of both the Cu/Ni/Si and Cu/NiSi/Si contacts over 200–500 °C, and determined that the Cu/NiSi stack has much better Cu diffusion barrier properties than Cu/Ni stack. We have also shown that both Ni and NiSi barrier layers dissolve into Cu at elevated temperatures.

6.3. Experimental Details

The experimental details regarding sample processing are described below.

6.3.1. NiSi formation in two- and one-step process

Single-side-polished, 300 μm thick, *n*-type Czochralski (Cz) Si(100) wafers (WRS Materials) with a resistivity of 1–5 Ω·cm were used as substrates. The wafers were cleaned using standard piranha and RCA cleaning processes [128]. Subsequently, the wafers were immersed into 1% HF aqueous solution to remove any native oxide prior to Ni deposition. Nearly 50 nm of Ni was deposited at room temperature on the polished side of these wafers in an *e*-beam deposition tool, which had a base pressure of ~10^{-7} Torr. The samples were then annealed in a rapid thermal annealing chamber (MILA 3000) in N_2 atmosphere for NiSi formation. Figure 6.1a shows the processing sequence for the formation of NiSi via the two-step and one-step annealing processes. For the two-step process the Ni coated *c*-Si wafers were first annealed at 250 °C for 5 min, the

unreacted Ni was then removed using a piranha solution, which was followed by a second annealing step at 450 °C for 5 min. In the one-step process, the Ni-coated *c*-Si wafers were annealed directly at 450 °C for 2–8 min. The films were characterized at different stages of annealing using XRD [Rigaku DMax with a Cu K_α source (λ = 0.154 nm)] in the Bragg-Brentano θ-2θ configuration to determine the crystalline phases. The XRD measurements were complimented with Raman spectroscopy (Renishaw InVia) in a backscatter geometry using a 532 nm excitation wavelength. The diffraction peaks were indexed using powder diffraction file number 00-048-1339 for Ni_2Si, 00-038-0844 for NiSi, 00-004-0836 for Cu, and 00-051-0916 for Cu_3Si.

6.3.2. Thermal stability of Cu/Ni/Si and Cu/NiSi/Si contacts

To evaluate thermal stability of the Cu/Ni/Si and Cu/NiSi/Si contacts, we generated test structures as described below. After the *c*-Si wafers were cleaned using the process described in Section 6.3.1, we created three types of structures: (a) with no metal film, (b) with ~50 nm Ni film, and (c) with ~110 nm NiSi film formed via the one-step annealing process. Subsequently, these structures were immersed into 1% aqueous HF. After this, ~200 nm of Cu was deposited on top of these layers in a thermal evaporation tool, which had a base pressure of ~10^{-7} Torr. The samples were then annealed in a tube furnace in N_2 atmosphere at 200–500 °C for 10 min to 70 hr. The thermal stability of the contacts was evaluated by determining the crystallographic phases formed after annealing using XRD, and with elemental depth profiling using Auger electron spectroscopy (AES). AES was performed using a 5 kV, 20 nA primary beam defocused such that a 50 μm diameter region was probed. Raw data were acquired, numerically differentiated, and worked up as described previously using PHI MultiPak v9.6.1.7. and Wavemetrics Igor [204]. A peak interference between a minor copper AES transition and the main nickel line at 849 eV was

removed using a linear least squares fitting routine [205]. Sputter profiling was performed with the sample rotating at 1 rpm using 3 kV Ar^+ at a current density of 20 μA/cm^2.

6.3.3. NiSi as a Cu diffusion barrier

To study Cu diffusion into *c*-Si across the NiSi barrier layer, we used *c*-Si(100) wafers similar to the ones described in Section 2.1. Hydrogenated amorphous Si (*a*-Si:H) was deposited on the polished side of the *c*-Si wafer from a SiH_4/H_2 capacitively-coupled, radio-frequency plasma powered at 13.56 MHz. The flow rates of SiH_4 and H_2 were 1 and 100 standard cm^3/min, respectively. The *c*-Si wafer was placed on the grounded substrate holder at a temperature of 300 °C with an input power to the plasma source of 10 W for 10 min to grow a ~50-nm-thick hydrogenated amorphous Si (*a*-Si:H) layer as described in Section 2.3. This *a*-Si:H film was subsequently annealed in a quartz tube furnace at 850 °C for 30 min in N_2 atmosphere to convert *a*-Si:H to a polycrystalline Si (*poly*-Si) layer. The samples were then immersed into 1% aqueous HF, and Ni was then deposited on the opposite side of the wafer and converted to 30–40 nm thick NiSi by annealing at 500 °C for 90 s, followed by a piranha etch to remove the excess Ni. The samples were then immersed into 1% aqueous HF, and ~200 nm thick Cu was thermally evaporated onto the NiSi layer or directly on *c*-Si. The Cu pads were restricted to an area that was smaller than the size of the *c*-Si wafer to ensure that Cu could not diffuse to the *poly*-Si film on the opposite side by migrating along the edge of the wafer. The test structures were then annealed at 200 °C for 65 hr in an inert N_2 atmosphere, and the Cu concentration on the *poly*-Si film side was analyzed using dynamic Secondary Ion Mass Spectrometry (SIMS) depth profiling using 1.5 keV oxygen ions.

6.4. Results and Discussion

Experimental results are provided and discussed below.

6.4.1. NiSi characterization and optimization of the one-step annealing process

Figure 6.1a shows the process flow for the formation of NiSi via the two-step and the one-step annealing process and Fig. 6.1b shows the corresponding X-ray diffractograms recorded at different stages of annealing of the Ni film on *c*-Si. Specifically, diffractogram “i” in Fig. 6.1b shows that annealing of a ~50 nm thick Ni film on *c*-Si (Ni/Si) for 5 min at 250 °C, followed by etching of excess Ni in a piranha solution results in the formation of only a polycrystalline Ni_2Si phase. Diffractogram “ii”, which was measured after further annealing of the Ni_2Si/Si structure in “i” at 450 °C for 5 min shows the formation of only a polycrystalline NiSi phase. Thus, diffractograms “i” and “ii” in Fig. 6.1b show that the processing conditions used in this study provide excellent control over the nickel silicide phase. Diffractogram “iii” in Fig. 6b shows that after process optimization, the NiSi film formed after direct annealing of a Ni film on *c*-Si at 450 °C for 5 min is very similar to the NiSi film formed via a two-step annealing process. The analysis of the diffractograms here is limited to identifying the crystallographic phases: we have not analyzed the preferred orientation of the crystallites or the stress in the nickel silicide films.

All three nickel silicide films described above were also characterized using Raman spectroscopy (see Fig. 6.1c). The peaks at ~100 and ~140 cm^{-1} observed in spectrum “i” are attributed to the Ni_2Si phase, and the peaks at ~197 and ~216 cm^{-1} observed in spectra “ii” and “iii” are attributed to the NiSi phase [206]. Based on the analysis of the XRD patterns and the Raman spectra we conclude that we can grow very similar NiSi films on *c*-Si either by the two- or one-step annealing process of Ni film on *c*-Si. The good agreement between the XRD and Raman

spectroscopy data also establishes Raman spectroscopy as a quick diagnostic tool to identify the NiSi phase and to check for phase purity. In addition to this, the absence of the Raman-active *c*-Si phonon band at 521 cm^{-1} in spectra "ii" and "iii" in Fig. 6.1c confirms that the NiSi films formed using both two- and one-step annealing approaches of *e*-beam deposited Ni on *c*-Si provide a continuous pinhole- and crack-free film that completely covers the underlying *c*-Si surface. On the other hand, it has been previously reported that NiSi films grown using electroless Ni deposition on *c*-Si often leads to the formation of pinholes or cracks that penetrate through the entire thickness of the NiSi films [202]. Complete surface coverage of *c*-Si with NiSi is vital if the NiSi film is to be used as a Cu diffusion barrier layer as the presence of any defects will allow for ready diffusion of the Cu into the *c*-Si substrate, which will deteriorate cell performance. Thus, the above results verify that the simpler one-step process for NiSi formation gives structurally similar NiSi films to those obtained via the two-step process.

While we have shown that one-step annealing of Ni films on *c*-Si can lead to NiSi formation, the process had to be optimized to ensure complete consumption of Ni and formation of a film with only the NiSi phase. The formation of NiSi from Ni on *c*-Si is a diffusion controlled process [192]. Between 200–350 °C, Ni diffuses into Si forming the Ni_2Si phase. Upon annealing at higher temperatures, 400–550 °C, Ni diffuses farther into *c*-Si forming the desired NiSi phase. The growth of a film with only the NiSi phase is important because a film with a mixture of NiSi and the high-resistivity Ni_2Si phase [192], will likely result in higher series-resistance-induced losses in the final device while also affecting its Cu diffusion barrier properties. We optimized our conditions for ~50-nm-thick Ni films on *c*-Si by fixing the annealing temperature at 450 °C, while varying the annealing time from 2 to 8 min. The inset in Fig. 6.1c shows the temporal evolution of the Raman spectra during direct annealing of Ni films on *c*-Si at 450 °C in N_2 ambient.

It can be seen that for an annealing duration of 2 min, only the Ni_2Si phase is formed, and not the NiSi phase. Only after annealing for more than 4 min we start observing peaks in the Raman spectra that are associated with the NiSi phase, while spectral features associated with the Ni_2Si phase disappear. This indicates that for complete conversion of Ni to NiSi, we need to anneal the Ni films for a certain minimum duration, which we speculate will depend on the initial thickness of the deposited Ni film. For the remainder of this study, unless mentioned otherwise, we grew the NiSi films by annealing ~50 nm thick Ni films on *c*-Si at 450 °C for 5 min in N_2 ambient.

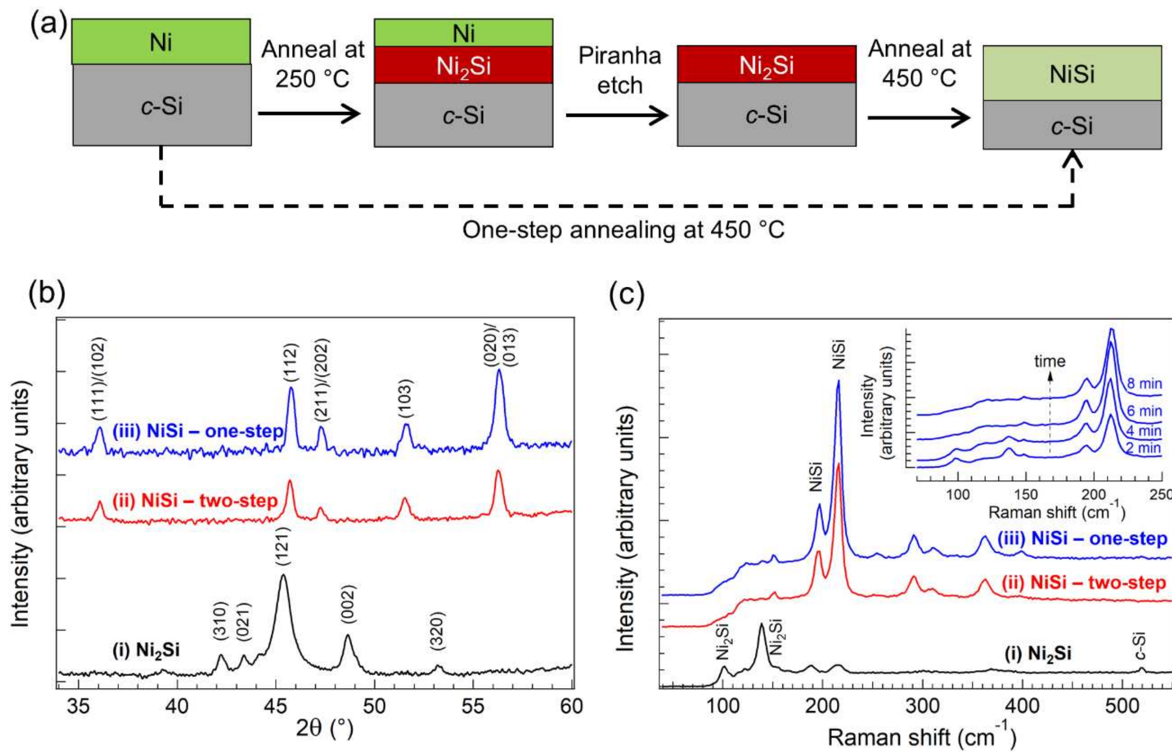

Figure 6.1 (a) Process sequence for the formation of NiSi on *c*-Si via a two-step or one-step annealing process. (b) X-ray diffractograms recorded at different stages of annealing of Ni films on *c*-Si: (i) after annealing for 300 s at 250 °C, followed by etching of excess Ni in a piranha solution; (ii) after annealing the structure in "i" for another 300 s at 450 °C; and (iii) after direct annealing for 300 s at 450 °C in a one-step process. (c) Raman spectra recorded at different stages of annealing of Ni films on *c*-Si corresponding to the conditions described in Figure 1b. The inset shows the temporal evolution of the Raman spectra during one-step annealing of Ni films on *c*-Si at 450 °C.

6.4.2. Thermal stability of Cu/Ni/Si and Cu/NiSi/Si contacts

Figure 6.2 shows the X-ray diffractograms of different Cu containing film stacks (see inset) recorded after annealing at 200 °C for 65 hr in a N_2 environment. Diffractogram "a" in Fig. 6.2 is that of a control sample with ~200 nm thick Cu film directly deposited on *c*-Si. The diffraction peaks could be indexed to Cu and Cu_3Si phases. The presence of Cu_3Si shows that under these experimental conditions, in the absence of a diffusion barrier, Cu readily diffuses and dissolves in *c*-Si. The detection of the Cu_3Si peaks also gives us a tool to determine if the Cu indeed diffuses through the Ni or NiSi barrier layers and dissolves into the underlying Si. Diffractograms "b" and "c", which are of the Cu/Ni/Si and Cu/NiSi/Si stacks, respectively, contain peaks that cannot be indexed to any Cu_xSi phases indicating that both Ni and NiSi can be effective Cu diffusion barriers at 200 °C for up to 65 hr. However, formation of the high resistivity Ni_2Si phase is evident in the Cu/Ni/Si sample shown in diffractogram "b". The NiSi layer is thermally more stable than Ni in contact with Cu because in diffractogram "c" corresponding to the Cu/NiSi/Si contact, crystallographic phases associated with only the Cu film and the underlying NiSi layer are present. Also, in both the Cu/Ni/Si and Cu/NiSi/Si contacts, after annealing, we notice a shift in the Cu diffraction peaks to a higher 2θ value (see diffractograms "b" and "c" in Fig. 6.2). This shift in peak position can be seen more clearly for the Cu(200) peak shown in the inset of Fig. 6.2. Both, Cu and Ni have the face-centered cubic structure with the Cu lattice constant being slightly larger than that of Ni. Also, these metals are positioned next to one another in the periodic table and are readily soluble in one another. The shift of the Cu peak to higher 2θ value can be explained by the alloying of the Cu lattice with the slightly smaller Ni atoms that migrate either from the Ni film or due to dissolution of NiSi. Thus, we can conclude from the analysis of the data in Fig. 6.2 that

both Ni and NiSi might be effective Cu diffusion barriers at 200 °C with the Cu/Ni contact showing poorer thermal stability due to Ni_2Si formation.

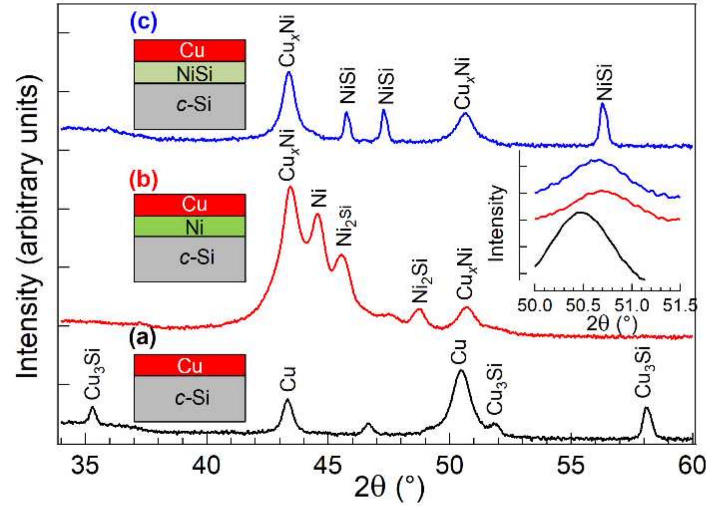

Figure 6.2 X-ray diffractograms recorded after annealing three different film stacks at 200 °C for 65 hr in N_2: (a) Cu directly on *c*-Si; (b) Cu on Ni deposited onto *c*-Si; and (c) Cu on NiSi grown on *c*-Si. For each sample, ~200 nm of Cu was thermally evaporated onto the top surface. The inset shows a magnified view of the diffractograms in the 2θ range around 50.5°, which corresponds to the Cu(200) diffraction. For clarity, only the relevant crystallographic phases are labeled.

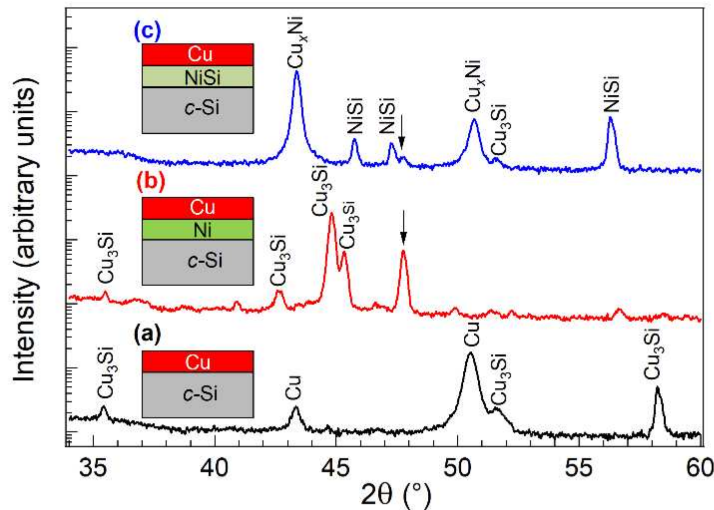

Figure 6.3 X-ray diffractograms recorded after annealing three different film stacks at 450 °C for 600 s in N_2 corresponding to the structures described in Fig. 6.2.

Figure 6.3 shows X-ray diffractograms of structures similar to those shown in the inset of Fig. 6.2, but annealed to a higher temperature of 450 °C for 10 min in N_2. These test structures are reproduced in the inset of Fig. 6.3 for clarity. One of our aims here was to determine if we can form a Cu/NiSi/Si contact by directly annealing Cu/Ni/Si contact structure at 450 °C, which was the temperature used for the one-step synthesis of NiSi (see Section 6.3.1). Similar to diffractogram "a" in Fig. 6.2, diffractogram "a" for the Cu/Si structure in Fig. 6.3 shows the presence of Cu and Cu_3Si phases due to the dissolution of Cu into the underlying *c*-Si. Diffractogram "b" in Fig. 6.3, which corresponds to the annealed Cu/Ni/Si structure shows strong evidence of Cu_3Si formation. In fact, in diffractogram "b" we can no longer identify any peaks corresponding to crystalline Cu indicating the complete conversion of Cu to other phases. Diffraction peaks corresponding to nickel silicide phases are also absent, which indicates that the formation of Cu_3Si is thermodynamically more favorable than formation of nickel silicide. We speculate that the strong unidentified peak in diffractogram "b" in Fig. 6.3 at $2\theta \approx 47.5°$ is due to a Cu-Ni or Cu-Ni-Si alloy. Finally, in diffractogram "b" in Fig. 6.3, the $Cu_3Si(012)$ diffraction peak at $2\theta \approx 44.5°$ can also be assigned to Ni(111), as some Ni may remain unreacted with both *c*-Si and Cu. Regardless of the interpretation of the diffraction peak at $2\theta \approx 44.5°$, we can conclude that the Ni film in contact with Cu and Si is unstable and not a sufficient barrier for Cu diffusion at 450 °C. Diffractogram "c" in Fig. 6.3 is very similar to diffractogram "c" in Fig. 6.2 except for a weak unassigned diffraction peak at $2\theta \approx 47.5°$ and a weak $Cu_3Si(311)$ diffraction peak at $2\theta \approx 51.8°$. Thus, we also conclude that while NiSi barrier layer is thermally more stable than Ni, at 450 °C the NiSi surface in contact with Cu starts to dissolve forming Cu_3Si. Further evidence for this from AES measurements is discussed below.

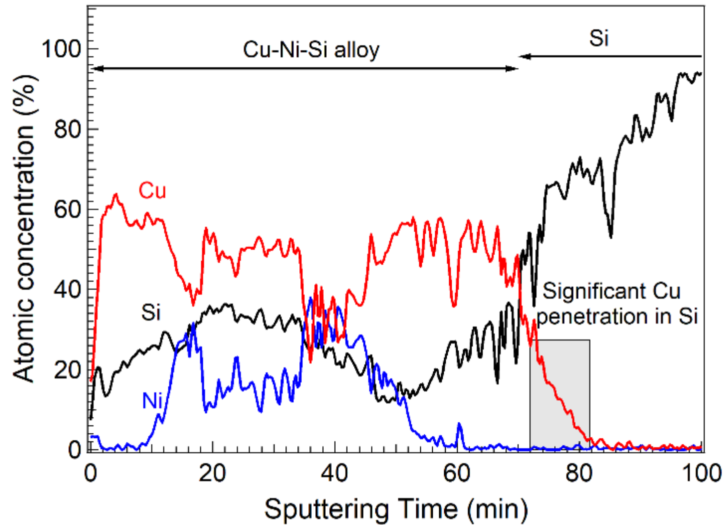

Figure 6.4 Elemental depth profiles for Cu, Ni, and Si obtained from AES for a stack consisting of ~200 nm Cu on ~50 nm Ni on *c*-Si annealed at 450 °C for 10 min in N_2. Sputtering was done on the Cu side of the sample, and thus $t = 0$ corresponds to the Cu side of the stack.

To determine the movement of Cu, Ni, and Si atoms through the Cu/Ni/Si film stack annealed at 450 °C for 600 s we measured the elemental depth profiles with AES. In Fig. 6.4, the atomic concentration of various elements measured with AES are plotted as a function of the sputtering time. From the analysis of these elemental profiles, it is clearly evident that the Cu/Ni/Si film stack has completely degraded after annealing at 450 °C to form a Cu-Ni-Si alloy. Not only is there a significant concentration of Si, ~20 atomic percent, detected at the surface, but we also find that Cu is clearly penetrating through the Ni into the *c*-Si substrate: this is evident from the tail end of the Cu concentration profile between the 70-80 min sputtering time range, which corresponds to a transition to the *c*-Si bulk. Thus, the XRD and AES results in Figs. 6.3 and 6.4, respectively, clearly establish that the Cu/NiSi/Si contact is much more thermally stable and a better diffusion barrier for Cu than the Cu/Ni/Si contact if the cell were to undergo a high-temperature annealing step after metallization.

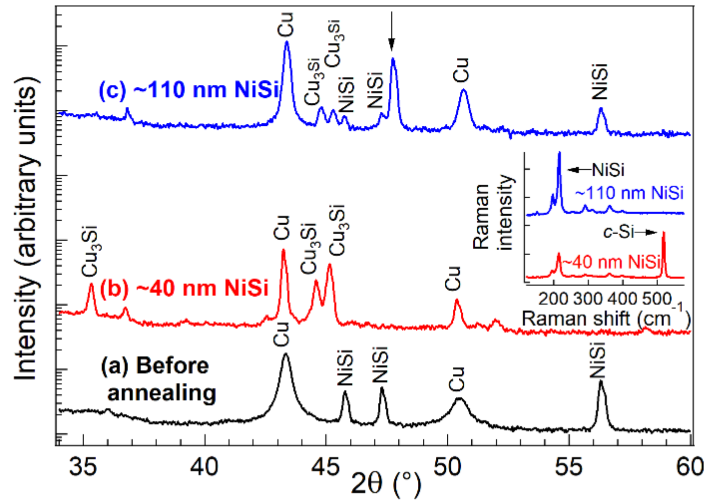

Figure 6.5 X-ray diffractograms recorded before and after annealing stacks of ~200 nm Cu evaporated onto NiSi grown on *c*-Si. (a) Cu on ~110 nm thick NiSi prior to annealing, (b) Cu on ~40 nm thick NiSi film annealed at 450 °C for 11 hr, and (c) Cu on ~110 nm thick NiSi film annealed at 500 °C for 1.5 hr. The inset shows Raman spectra of ~40 and ~110 nm thick NiSi films grown on the *c*-Si substrate prior to Cu deposition.

We also studied the effect of NiSi thickness on the thermal stability of the Cu/NiSi/Si contacts using Raman spectroscopy and XRD (see Fig. 6.5). The inset in Fig. 6.5 shows the Raman spectra for ~40 and ~110 nm thick NiSi films on a *c*-Si substrate prior to Cu deposition. In both these Raman spectra, the presence of phase-pure NiSi can be confirmed based on the characteristic vibrational features at ~197 and ~216 cm^{-1} [206]. The difference is the NiSi layer thickness can be inferred from the presence of an intense *c*-Si phonon band at ~521 cm^{-1} in the ~40 nm NiSi sample. This vibrational feature is absent for the thicker ~110 nm NiSi sample, as the thicker NiSi films prevents the collection of the backscattered photons from the underlying *c*-Si. We further note that the presence of the *c*-Si phonon band for the ~40 nm NiSi film is not due to a discontinuous film, since discontinuous NiSi films imaged through scanning electron microscopy tend to completely saturate the detector in the ~521 cm^{-1} region in our Raman spectroscopy instrument [202]. In Fig. 6.5, X-ray diffractogram "a" corresponds to the Cu/~110 nm NiSi/Si structure prior to thermal

annealing. The XRD pattern clearly shows the presence of Cu and NiSi diffraction peaks, and serves as a reference measurement for the annealed samples. In diffractogram “b” in Fig. 6.5, which was recorded after annealing the Cu/~40 nm NiSi/Si stack structure at 450 °C for 11 hr, we observe strong diffraction peaks associated with the Cu and Cu_3Si, and diffraction peaks corresponding to any nickel silicide phase are absent indicating the complete degradation of the NiSi barrier layer. We repeated this measurement with a thicker ~110 nm NiSi film, which was annealed at 500 °C for 90 min (see diffractogram “c” in Fig. 6.5). For the ~110 nm NiSi film, we observe some low intensity features that are associated with the Cu_3Si phase. Additionally, comparing diffractogram “a” and “c” in Fig. 6.5, i.e., before and after annealing, we notice a reduction in the intensity of the NiSi peaks as well as the presence of the unassigned peak at $2\theta \approx 47.5°$, which was previously also observed in diffractograms “b” and “c” in Fig. 6.3, and tentatively assigned to a Cu-Ni or Cu-Ni-Si alloy.

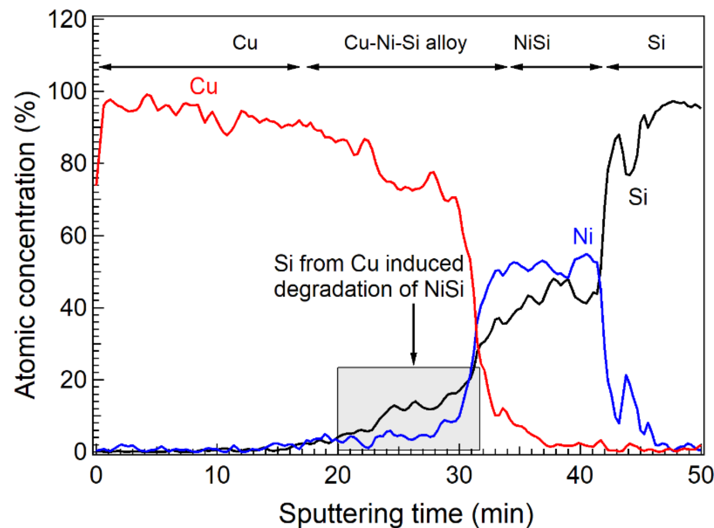

Figure 6.6 Elemental depth profiles for Cu, Ni, and Si obtained from AES for a stack consisting of ~200 nm Cu on ~110 nm NiSi on *c*-Si annealed at 500 °C for 90 min in N_2. Sputtering was done on the Cu side of the sample, and thus $t = 0$ corresponds to the Cu side of the stack.

To understand the reason for the changes in NiSi film due to extended high-temperature annealing of the Cu/NiSi/Si stack, using AES, we measured the depth profiles of the Cu/~110 nm NiSi/Si stack that was annealed at 500 °C for 90 min. The elemental profiles in Fig. 6.6 are again shown as a function of sputtering time. For times greater than 43 min, we start to detect the *c*-Si substrate with some diffused Ni and negligible amounts of Cu, which shows that NiSi is an effective Cu diffusion barrier even at higher temperatures. For sputtering times between 37 and 43 min we observe Ni and Si with atomic fraction of ~1:1 indicating the presence of the NiSi phase, while the atomic fraction of Cu is small. This is consistent with the NiSi peaks observed in XRD pattern "c" in Fig. 6.5. However, between 31–37 min sputtering time, Ni and Si are not present in a ~1:1 ratio, which suggests the original NiSi film has partially degraded and some Cu has also diffused in this region. Also, between a sputtering time of 20–32 min some of the Si and Ni have diffused into the Cu film due to the degradation of the NiSi film. Thus, the composition of the region between sputtering time of 20–37 min is consistent with the Cu_3Si and the Cu-Ni-Si XRD pattern "c" in Fig. 6.5. Based on these results we can infer that Cu induces the degradation of NiSi, forming Cu_3Si. At annealing temperatures ≤ 200 °C, we speculate that this degradation of NiSi is slow, and the integrity of the NiSi layer for preventing Cu diffusion can be prolonged by using a thicker NiSi film.

6.4.3. Evaluation of NiSi as a Cu diffusion barrier

To evaluate the Cu diffusion barrier properties of the NiSi layer via SIMS, we used test structures shown in the inset in Fig. 6.7. In these structures, one side of the double-side polished *c*-Si wafer has either a (a) Cu film on *c*-Si, (b) a Cu/NiSi/Si stack, or (c) NiSi film on *c*-Si. The other side of the test structure is a ~50 nm thick poly-Si layer, the purpose of which is to provide a sink for the Cu atoms diffusing from the Cu film through the thickness of the *c*-Si wafer. Cu is

unlikely to be directly detected in bulk *c*-Si using common elemental characterization tools such as SIMS due to a very low solubility in *c*-Si [186]. However, the grain boundaries in *poly*-Si film deposited on one side of the *c*-Si are expected to act as gettering centers for Cu. In previous work [202], we showed that for gettering Cu into the *poly*-Si layer such that the Cu concentration is detectable with SIMS (~10^{17} cm^{-3}), the structure in inset (a) in Fig. 6.7 had to be annealed at ≥300 °C for 11 hr. However, since we have established that the Cu/NiSi/Si contact is unstable at these temperatures (see Section 6.4.2), we were limited to annealing the above structure at a much lower temperature of 100 °C for 70 hr. We measured the Cu concentration profiles in a Cu/NiSi/*c*-Si/*poly*-Si stack (structure "b" in Fig. 6.7). For comparison, we also measured the Cu concentration profiles in the Cu/*c*-Si/*poly*-Si sample (structure "a" in Fig. 6.7), and the Cu-free NiSi/*c*-Si/*poly*-Si control sample (structure "c" in Fig. 6.7), which went through all the processing steps as the previous two except the actual Cu deposition step. The SIMS depth profile for the three samples in the *poly*-Si region is very similar even for the control sample with no deposited Cu. We can infer from this that the adventitious Cu introduced in the *poly*-Si layer during sample processing is much more than the Cu diffusing from the other side of the wafer and, hence, we conclude that measurements are not feasible due to the low Cu flux through *c*-Si at 100 °C.

6.5. Summary and Conclusions

We have shown using XRD and Raman spectroscopy that NiSi films grown using the industrially relevant, piranha-free, one-step annealing process are very similar to the films grown via the conventional two-step NiSi annealing process. For the one-step process, we optimized the processing conditions for NiSi formation to ensure complete Ni consumption and formation of a pure, continuous, low-resistivity NiSi film.

The thermal stability and effectiveness towards mitigating Cu diffusion of the Cu/Ni/Si and Cu/NiSi/Si contacts was studied over a temperature range of 200–500 °C using XRD and AES. It was shown that the Cu/NiSi/Si contact is a much more thermally stable, and a better diffusion barrier to Cu than the Cu/Ni/Si contact. The two main drawbacks of the Cu/Ni/Si contact are: (a) the formation of the less desirable Ni_2Si phase upon annealing to 200 °C for extended durations; and (b) rapid diffusion of Cu though the Ni layer at 450 °C with the absence of any Ni_xSi phase formation. The presence of Cu deteriorates barrier properties of NiSi film by slowly dissolving it at elevated temperatures. We also show that a thicker NiSi film is thermally more stable while mitigating Cu diffusion. Finally, we have shown that experiments for evaluating the effectiveness of NiSi as a Cu diffusion barrier using elemental detection techniques such as SIMS is challenging due to the low solubility of Cu in *c*-Si.

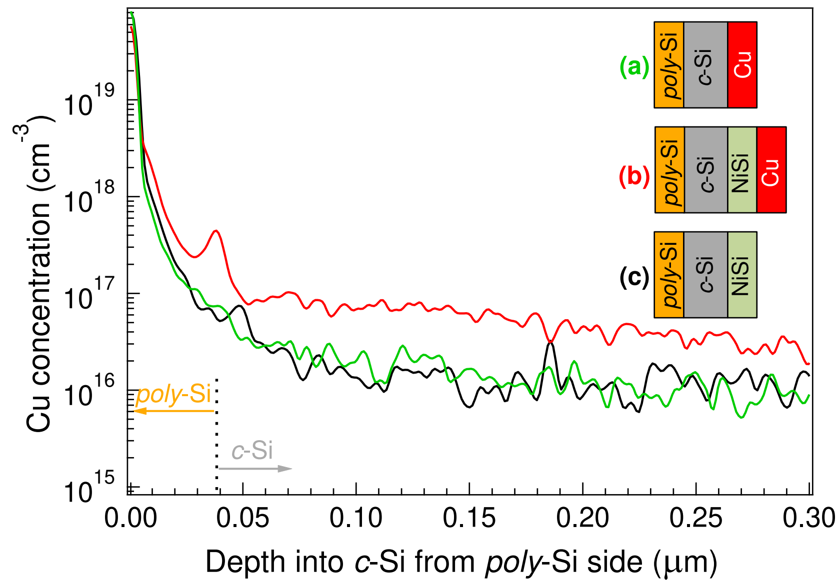

Figure 6.7 Dynamic SIMS depth profile of Cu within the *poly*-Si film and the underlying *c*-Si substrate for the structures shown in the inset annealed at 100 °C for 70 hr in N_2 environment: (a) ~200 nm of Cu directly evaporated on *c*-Si (—); (b) ~200 nm of Cu evaporated on ~40 nm of NiSi grown on *c*-Si (—); and (c) ~40 nm of NiSi grown on *c*-Si (—).

6.6. Acknowledgements

The authors thank Tonio Buonassisi and David Fenning for fruitful discussions, Robert Reedy for the SIMS measurement, Vincenzo LaSalvia and Teresa Barnes for providing access to the annealing furnaces. Funding for this work was provided by US DOE EERE contract SETP DE-EE00025783, SETP DE-EE00030301 (SuNLaMP) and under Contract No. DE-AC36-08GO28308. The publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

APPENDIX A

FACILITIES AT NATIONAL RENEWABLE ENERGY LABORATORY

A significant part of this thesis work was performed at the National Renewable Energy Laboratory (NREL), Golden, CO, USA. Below some of the facilities associated with the "High-efficiency Crystalline PV" group at NREL are listed and described.

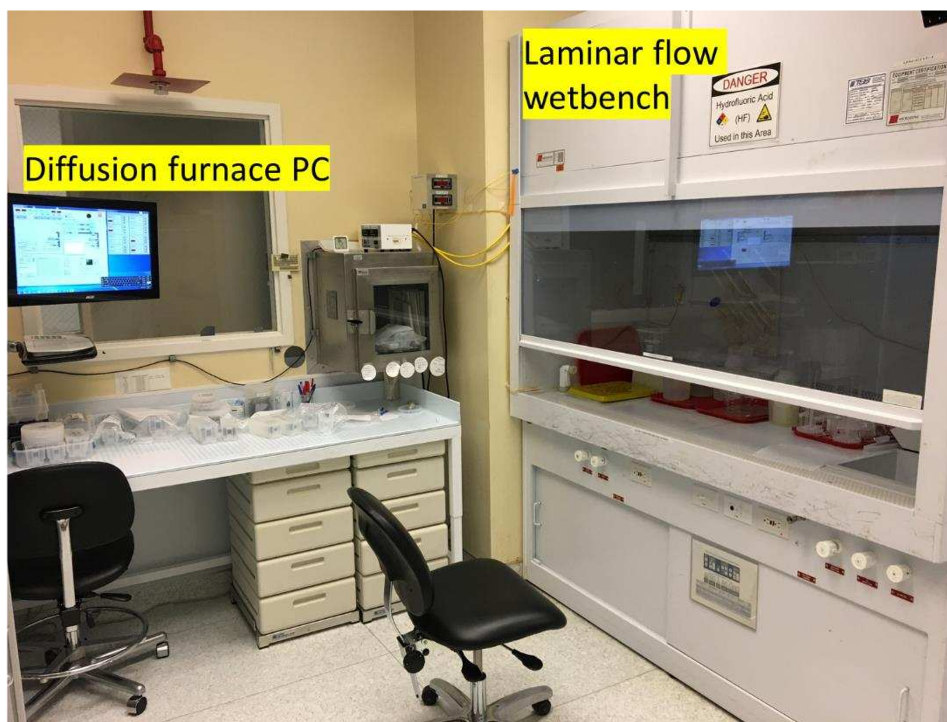

Figure A.1 Cleanroom showing the laminar flow wet-bench and diffusion furnace computer.

The Si dedicated cleanroom at NREL is a class 1000 cleanroom (see Fig. A.1), with facilities for wet-chemistries involving HF, H_2O_2, HCl, NH_4OH, H_2SO_4. Chemistries involving HNO_3, KOH, $N(CH_3)_4OH$ (TMAH), H_3PO_4, CH_3COOH are performed in a separate lab. A furnace bank consisting of dedicated furnaces for dry oxidation, annealing in N_2, H_2 and D_2, B-diffusion, and P-diffusion is also present in the same cleanroom (see Fig. A.2). Transfer elephants as shown

in Fig. A.2, are used for loading/unloading samples between the furnaces and the wet bench. Loading/unlading of the samples within the laminar fume hood gives conditions equivalent to a class 100 cleanroom. The same cleanroom also houses a Samco reactive-ion etcher with SF_6, CF_4 and O_2 gases plumbed to it (see Fig. A.3a). Characterization equipments such as a WCT-120 Sinton lifetime tester (see Fig. A.3b), 4-point probe, etc. are also present in the same cleanroom.

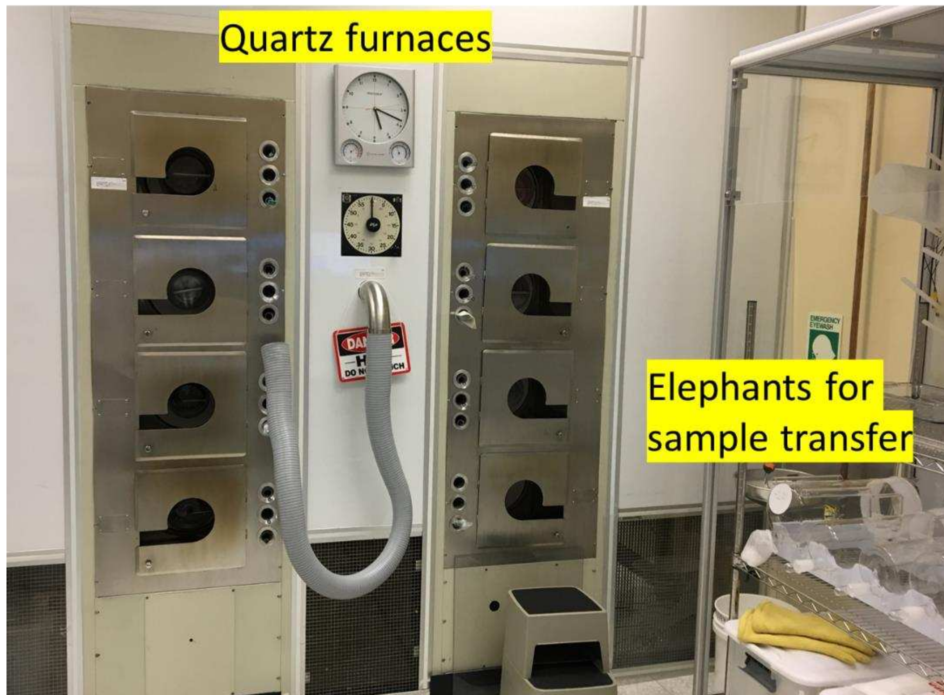

Figure A.2 Cleanroom showing the tube furnace bank and quartz elephants used for loading/unloading samples from the furnace

A Temescal FC-1800 metallization tool is present in an adjacent, but directly connected cleanroom to minimize metal contamination in the cleanroom housing the diffusion furnaces. Thermally evaporated Al, Ag, and Ti can be deposited using the FC-1800 at pressures as low as a 10^{-6} Torr using a cryogenic pump. The cleanroom adjacent to the metallization room is dedicated for photolithography and electroplating (see Fig. A.5).

Figure A.3 Samco reactive-ion etching tool (a), and Sinton WCT-120 lifetime tester (b) in cleanroom.

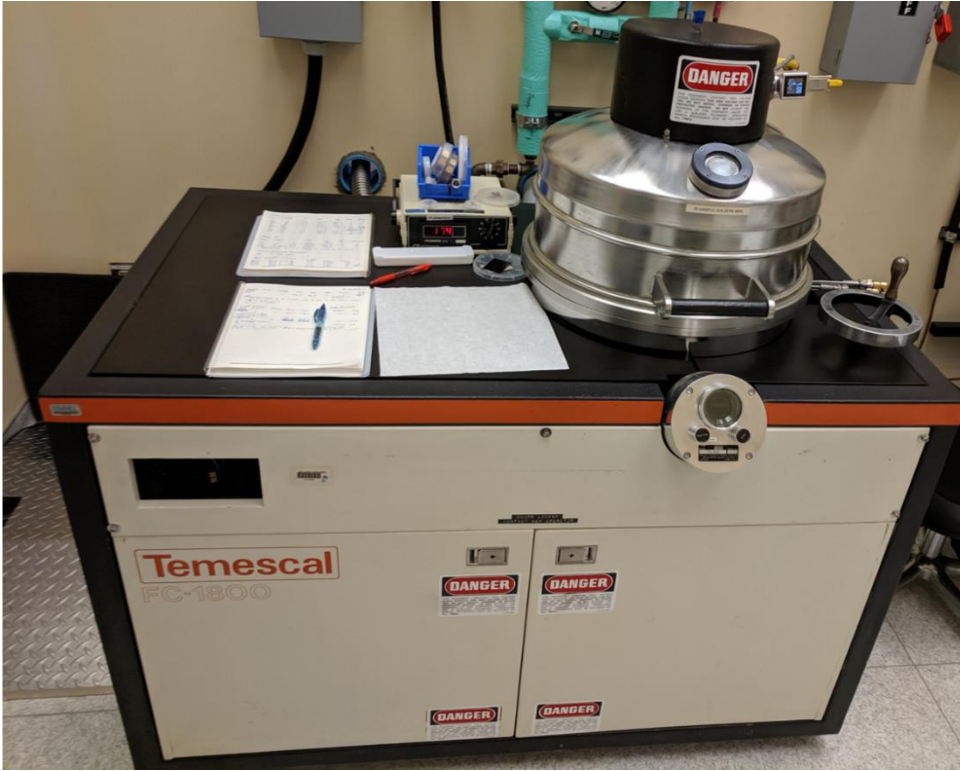

Figure A.4 Temescal FC-1800 thermally evaporated metallization tool in cleanroom.

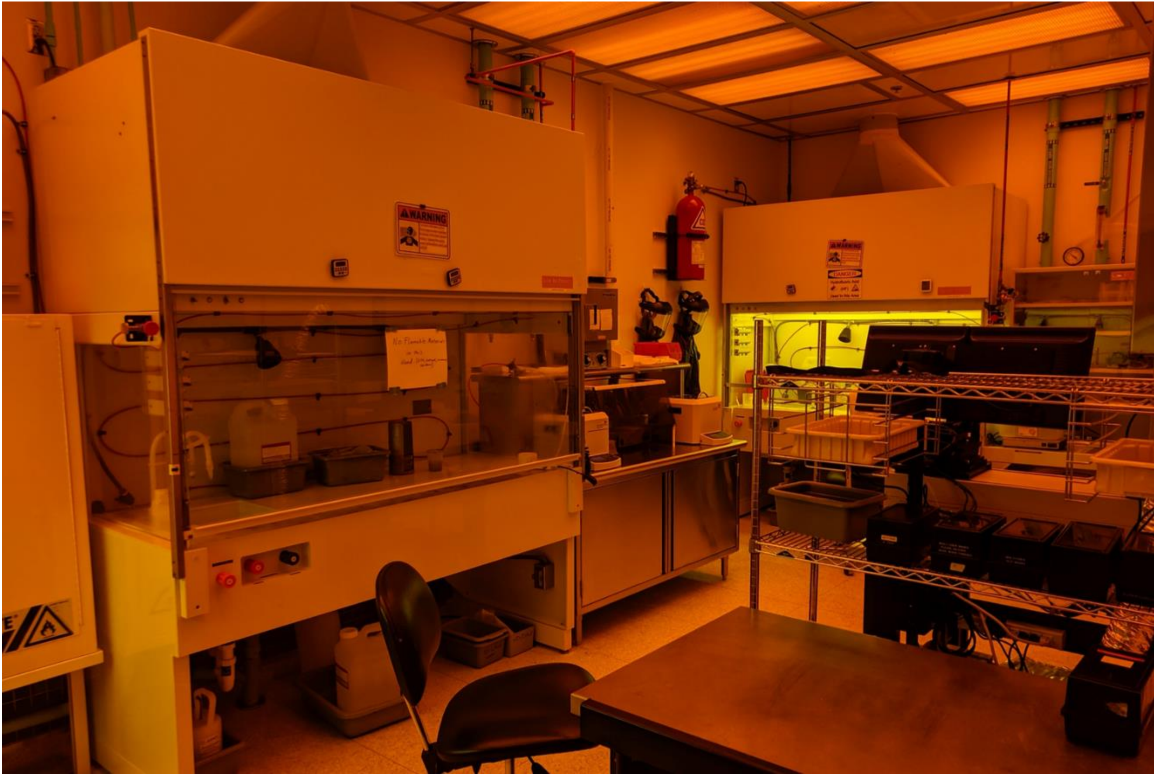

Figure A.5 Photolithography part of the cleanroom.

Another equipment used significantly for sample processing is the plasma-enhanced chemical vapor deposition (PECVD) cluster tool (see Fig. A.6a) manufactured by MVSystems Inc. (Arvada, CO). It is present in a separate building than the previous cleanroom, but connected via a skybridge. The cluster tool has numerous dedicated chambers, connected through a central chamber, thus allowing for different films to be deposited without breaking vacuum, as schematically shown in Fig. A.6b. A robot arm is used to move samples within the different chambers. The cluster tool can deposit films using plasmas, hot-wire CVD, and sputtering. A few deposited films are intrinsic and doped *a*-Si:H, *a*-SiGe:H, *a*-SiN_x:H, *a*-SiC_x:H, nanocrystalline Si, and transparent conductive oxides. Samples are loaded/unloaded from the cluster tool load-lock chamber while working in a laminar flow hood to minimize particulate contamination (see

Fig. A.7). The same hood is also connected to a benchtop Arradiance GEMStar-8XT atomic layer deposition (ALD) system which currently is used to deposit Al_2O_3 films via thermal ALD.

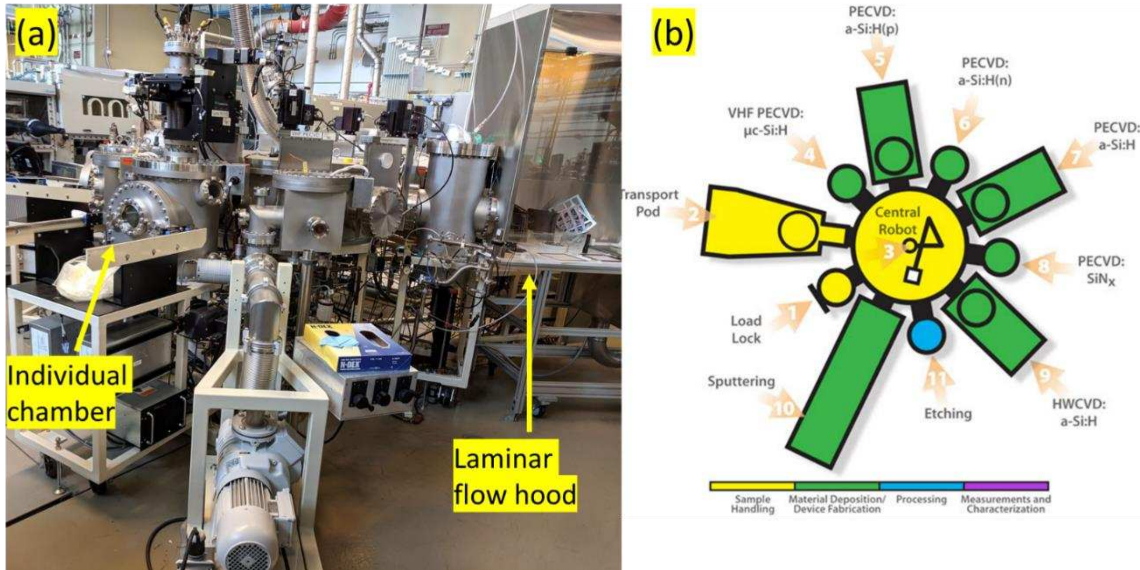

Figure A.6 Picture (a) and schematic (b) of the PECVD cluster tool.

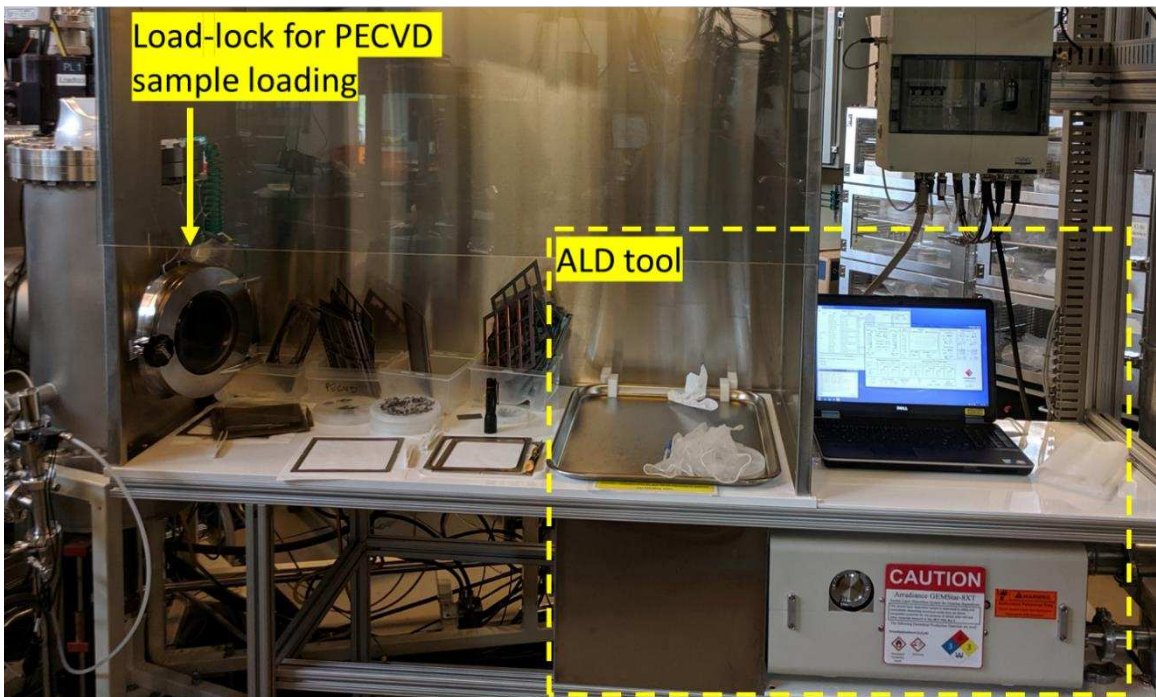

Figure A.7 PECVD load-lock for samples loading and the Arradiance GEMStar-8XT atomic layer deposition tool.

APPENDIX B

DISCUSSION OF EXPERIMENT ACCURACY

In this thesis, several figures have been shown without error bars, and hence it is important to discuss the measurement accuracy of the instruments used. SiO_x thickness was measured using spectroscopic ellipsometry using a SiO_2 model for fitting. SiO_x thicknesses <5 nm, were fitted using the same model. For SiO_x thickness >5 nm a different model was used. It must be noted that the measured SiO_x thickness depends on the model used for fitting. The measurement error observed when measuring SiO_x thickness at different locations on a *c*-Si wafer was less than ±0.05 nm. Due to the manual loading and unloading of samples from the tube furnace, we observed higher errors, ±0.1 nm, when two different samples were oxidized separately, under similar oxidation conditions. Hence, whenever a saw-damaged removed or textured wafer was oxidized, a sister-polished wafer was also oxidized, and the SiO_x thickness on the polished sample measured. For each figure, other processing steps, such as *a*-Si:H deposition, contact annealing, Al_2O_3 deposition, forming gas anneal were performed more or less in a batch manner to reduce processing variabilities. Observed measurement errors associated with measuring i-V_{oc} using Sinton lifetime spectroscopy were ±2 mV. In addition, the uniformity of the passivation was confirmed by photoluminescence imaging, and samples with nonuniformity were either discarded, or the reported measurements were performed on the largest area with uniform passivation. These photoluminescence images have not been shown in the thesis, unless required for scientific purposes. Furthermore, each data point shown in the figures was an average of 2–3 samples. The symbol size is large enough to represent the associated measurement error.

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