AN ISOLATED HIGH EFFICIENCY MULTIPLIER CELL-BASED PV SYSTEM DC-DC CONVERTER FOR RESIDENTIAL APPLICATIONS

by

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ABSTRACT

The global increase in PV installations has driven researchers to find more efficient integration techniques for interfacing PVs with the grid. More innovative converter structures are required to overcome the challenges that face conventional converters. This research presents a high voltage gain isolated DC-DC converter that is suitable for PV applications. The novel converter utilizes a high frequency transformer with 1:1 turns' ratio and multiplier cells that are also utilizing a 1:1 high frequency transformer. This new approach in topology fabrication allows for a reduced component rating and a very low normalized switch voltage ratio. That means very high voltage gain converters can be realized by using very low voltage switches and diodes. In addition, 1:1 turns' ratio transformers are easier to design and simpler to manufacture and cut the required duty cycle to half if used in half or full bridge configuration. This research also presents the designed non isolated DC-DC converters that led to the realization of the isolated DC-DC converter. A 450 W prototype is presented and tested to validate the concept and an efficiency study for the converter is also presented.

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NOMENCLATURE

PV	Photo voltaic
V_{dc}	DC link voltage
N	Turns' ratio
L_{in}	Input inductor
V_o	Output voltage
$MOSFET$	Metal–oxide–semiconductor field-effect transistor
$IGBT$	Insulated gate bipolar transistor
PWM	Pulse width modulation
$SEPIC$	Single ended primary inductance converter
φ	Magnetic flux
ZVS	Zero voltage switching
ZCS	Zero current switching
ΔB	Change in flux density
H	Magnetic field intensity

CHAPTER 1

INTRODUCTION

Renewable energy systems have gained an increased interest in the past decade due to the need for clean power without consuming fossil fuels or emitting any type of greenhouse gases. The solar PV installations have increased significantly in the United States and across the world in the past few years [1]. However, the intermittency of PV power generation makes it challenging to increase the number of installations due to their effect on the performance of the public utility grid [2]. To efficiently integrate PV installations into the grid, a high voltage gain converter with high efficiency must be used. PV Panels produce a low DC voltage that needs to be increased and inverted back to AC to inject power to the grid. There are different ways to do so. PV panels can be connected in series to produce a high voltage and then connected to a central inverter directly without using any boosting stage (Fig. 1.1) and thus reducing the system's size and components number. However, the maximum current in this case would be the current of the cell with lowest cell in the panels. In addition, the maximum power point tracking in this system is limited to the cell with the lowest power. The other issue is when a panel is shaded or damaged it would shut down the whole system.

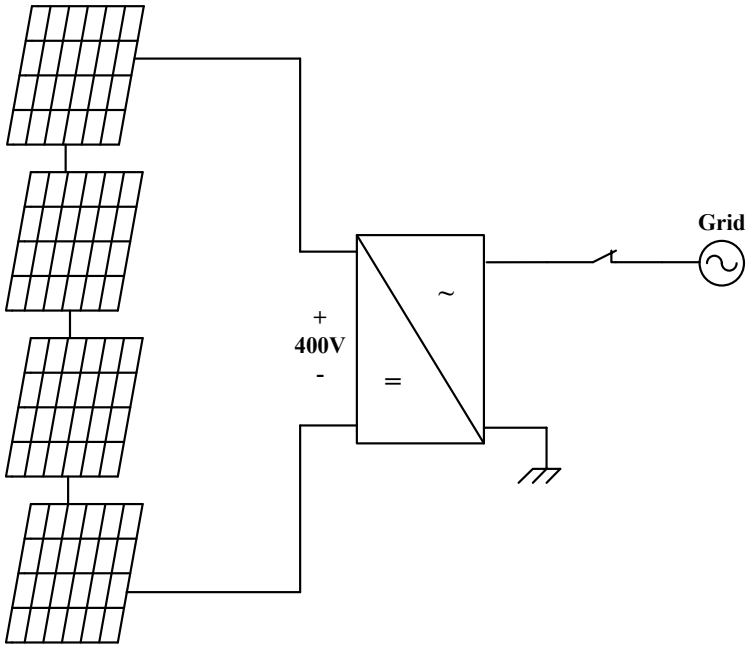


Fig. 1.1 Serious connection of PV panels connected to a central inverter

Another way is to connect PV panels individually to dedicated DC-DC converters and inverters (Fig. 1.2). This would give the system an increased reliability and maximum power point tracking. The issue of this approach is the increased number of components, the increased size (for the same frequency) and the increased cost. In addition, the efficiency of such systems needs to be addressed due to the increased power processing stages.

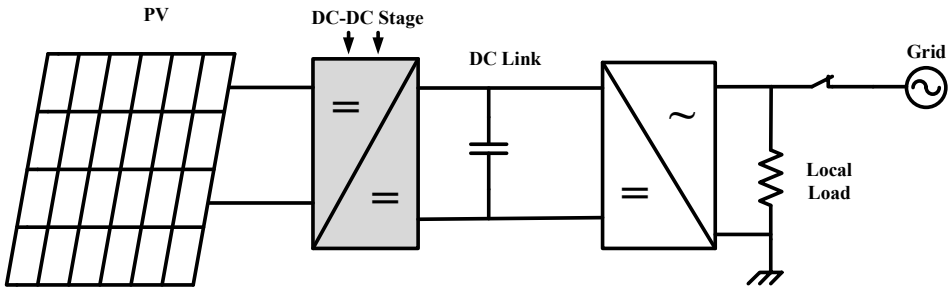


Fig. 1.2 Dedicated power conversion stages for each panels.

The desired system in that application should be developed in such a manner that it reduces the cost and does not compromise efficiency while maintaining the same reliability and functionality. Therefore, the focus of this Dissertation is to design and model a PV DC-DC Converter that provides high efficiency, reduces the cost and maintains all the desired functionalities using a novel approach. The efficiency could be improved by incorporation of soft switching techniques. The cost of the system can be reduced by using components that are rated for lower power levels. For example, a MOSFET that is rated for 48 V applications has a lower cost than a MOSFET that is used for 400 V applications. The proposed converter can produce the desired high voltage level while incorporating very low rated components and utilizes soft switching techniques to reduce the switching losses and increase efficiency.

1.1 Background

PV panels produce energy at low voltage levels (30-45 v) and in order to integrate them to the grid, either connect a number of the panels in series or have a converter to step up the voltage level. Connecting the panels in series poses a serious reliability issue and makes the system prone to shade effects. Using a DC-DC converter to raise the voltage level is commonly used in residential applications. However, conventional boost topologies cannot raise the voltage to the required level (400v) without imposing severe efficiency degradation and high level of

voltage and current stresses. The practical implementation of the classical boost converter would yield to the efficiency and voltage gain levels that are shown in figures (1.3) and (1.4). Even with low parasitic losses the voltage gain and efficiency suffer from severe degradation after 0.7 duty cycle [3]. To counter-act this problem, many researches have emerged trying to presents DC-DC converters that provide high voltage gain at reasonable duty cycles and efficiencies. In general, most of these converters require both high stress voltage switches and high turn's ratio transformers and coupled inductors.

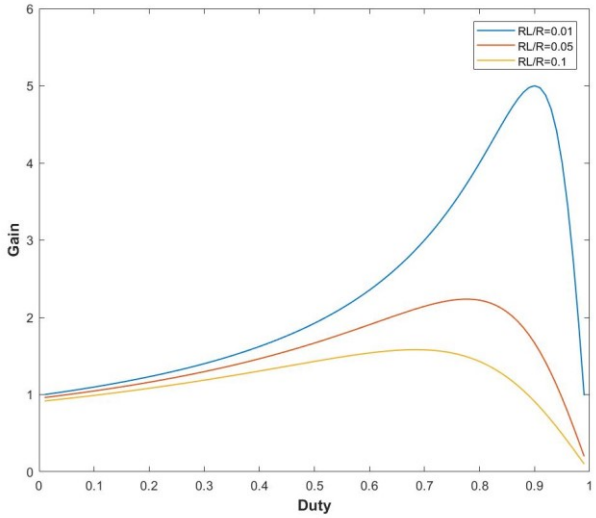


Fig. 1.3 Voltage Gain of boost converter with consideration of parasitic resistance [3]

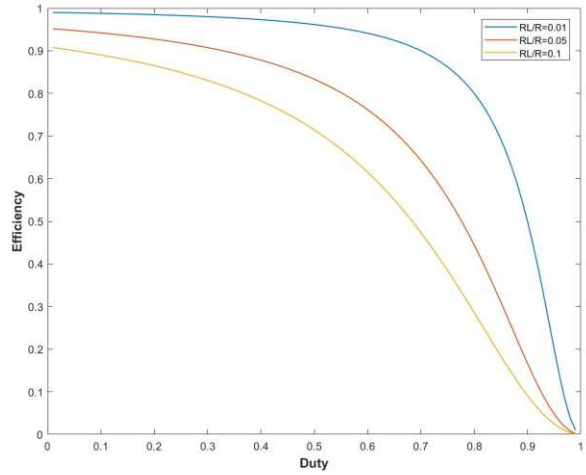


Fig. 1.4 Efficiency of boost converter with consideration of parasitic resistance [3].

These converters can be classified into two main categories, isolated and non-isolated converters. Each category will be detailed and explained and advantages and disadvantages will be mentioned in the next sections.

1.2 Isolated DC-DC Converter Topologies

Many high voltage gain approaches depend on isolated DC-DC topologies since they provide galvanic isolation which is highly desired and mostly required and mandated by regulatory institutions. The main concept of all isolated dc to dc converters depends on high frequency AC conversion with a high frequency transformer. The DC voltage is converted into high frequency AC using inverters. Then, the transformers steps up the voltage with a turn's ratio. The most commonly used topology in this kind is the dual active bridge topology [4] [5] [6]. This topology has become the industry standard for connecting battery systems into the grid or motor drives. It basically consists of two back to back inverters with a transformer in the middle. This topology provides a high gain because it utilizes the use of a transformer. It also provides a high frequency galvanic isolation between the DC source and the grid. Which means there is no need for a 60 Hz isolation transformer. However, since all the energy is transferred through the transformer, the transformer size would be designed to transfer the energy at a reasonable efficiency which would yield to an increased size and weight. In addition, this approach would require two back to back

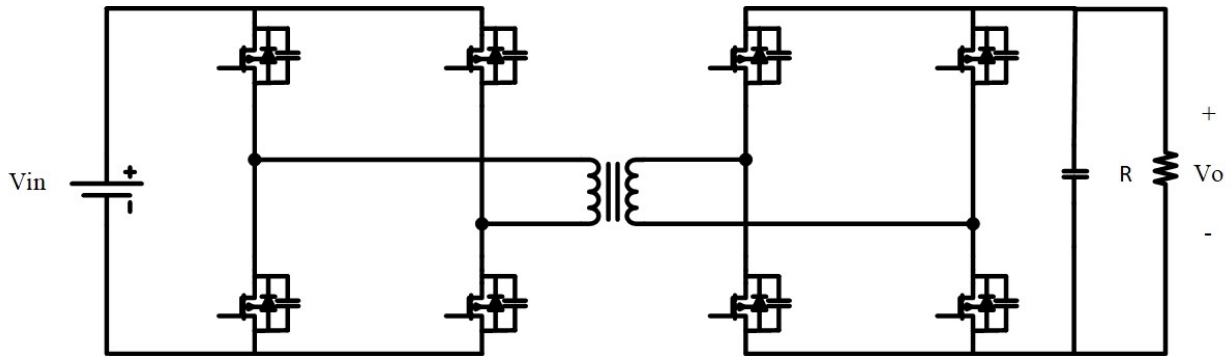


Fig. 1.5 isolated dual active bridge DC-DC converter [4].

Converters which would result in an increased number of power switches and an increased number of controls, measurements and supporting systems. The high turn's ration would yield to an increased voltage stress on the switches as well. For example, if the transformer is boosting the

voltage to 400 V, the required MOSFET or IGBT in this case must be more than 650 V if safety limits are taken into consideration. Another popular isolated topology is the resonant LLC converter which has gained an increased popularity in the recent years [7] [8] [9].

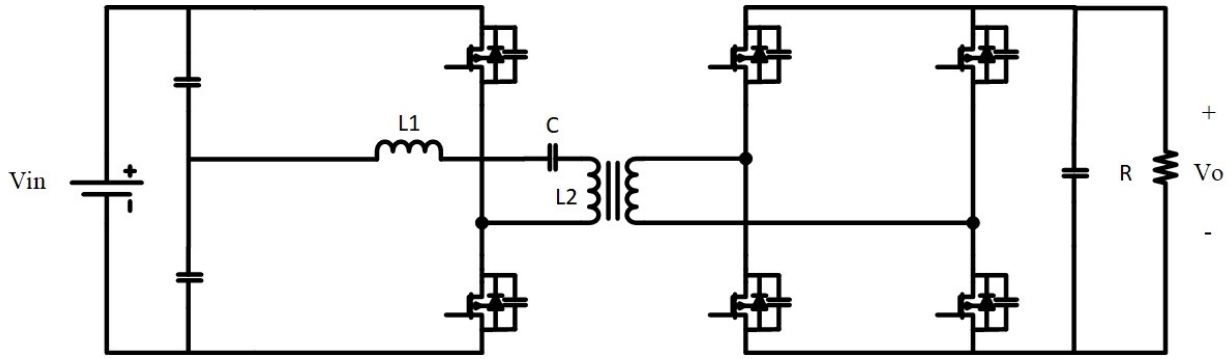


Fig. 1.6: Isolated LLC series resonant DC-DC converter [9].

The main benefit of this topology is its simplified control strategy. The voltage gain is directly coupled with the operating frequency. The higher the switching frequency the higher the output voltage is. Similar to the dual active bridge, the voltage of the transformer will reflect on the switches. That means if the transformer is designed to boost the voltage to 400 V, the switch has to endure all of it. Other topologies have been proposed in the literature that address switching losses by presenting converters that have isolation and high voltage gain and different approaches to address the voltage stress on switches [10] [11] [12]. In [10], an interleaved converter is presented that has a boosting stage before feeding the transformer with AC voltage. The two legs provide opposites boosted voltages that feed the transformer. The transformer then steps up the voltage and a rectification stage converts the voltage back to DC.

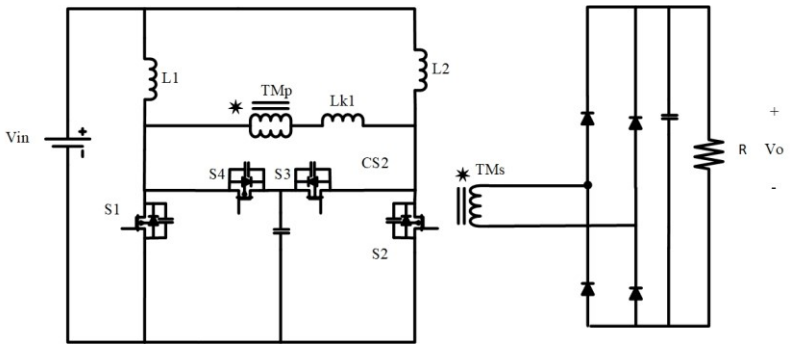


Fig. 1.7: Isolated LL type current fed DC-DC converter [10].

The main benefit of this approach is that it is PWM controlled and the required turn's ratio is cut to at least half with the boost stage. Another advantage is that the input current has very low current due to interleaving which is very desirable for PV applications. However, the output diodes still have to endure the full output voltage. In [12], the same approach used in [10] has been used here with the difference of adding a voltage doubler to each leg in the output. This will help reduce the required turn's ratio for the converter and provide different control choices. It can either controlled by PWM or phase shift control.

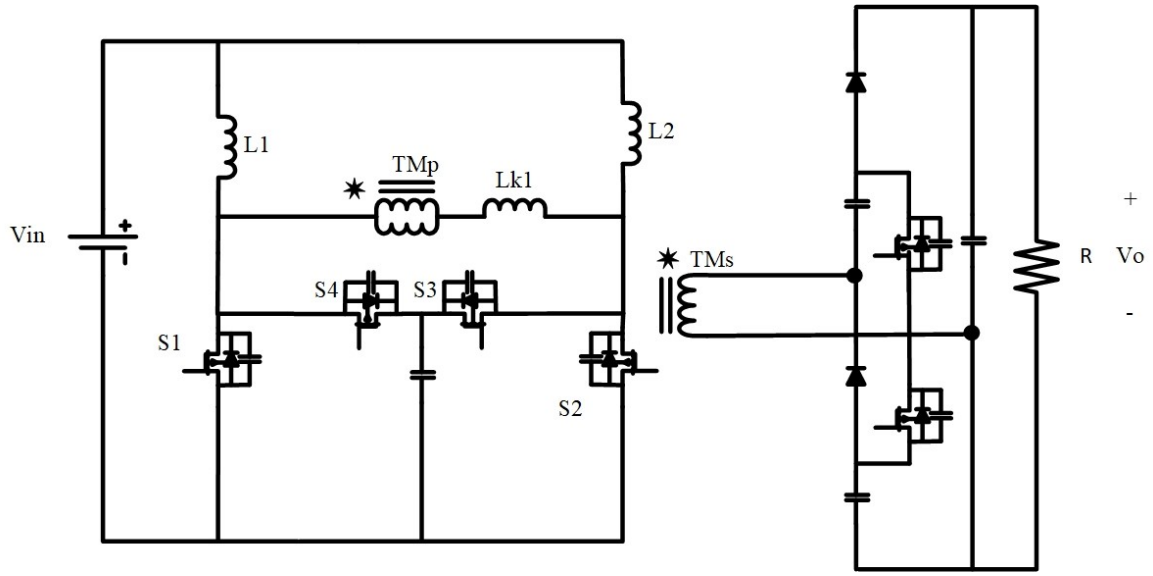


Fig. 1.8: Isolated current fed DC-DC converter with voltage quadrupled output [12].

To reduce the stress on output diodes and switches, the turn's ratio of the transformer must be reduced. To reduce the turn's ratio of the transformer, the converter must operate at a high duty cycle which would increase the voltage stress on the primary side switches. The converter must operate at a nominal duty cycle higher than 0.6 to use a 1:1 turn's ratio transformer. Otherwise, the turn's ratio must be increased and that would increase the stress on the secondary side switches and diodes.

1.3 Non-Isolated DC-DC converter Topologies

In this category, only the topologies that provide high voltage gain will be considered. Even though basic converters such as Buck, Boost, CUK, and SEPIC fall under this category, they will not be discussed due the shortcomings mentioned before. Non-isolated DC-DC

converter topologies can divided into two main sections. Switched capacitor topologies, and coupled inductor based topologies. Each one will be discussed in detail in the next subsections.

1.3.1 Switched capacitor DC-DC Converters

In this type of converters, capacitors are being charged and then switched to charge another set of Capacitors. Most of these topologies are fit for low power applications except for a few that have been proposed for high power applications. The multilevel Boost converter is one of them [13]. The configuration of the multilevel boost converter is shown as follow:

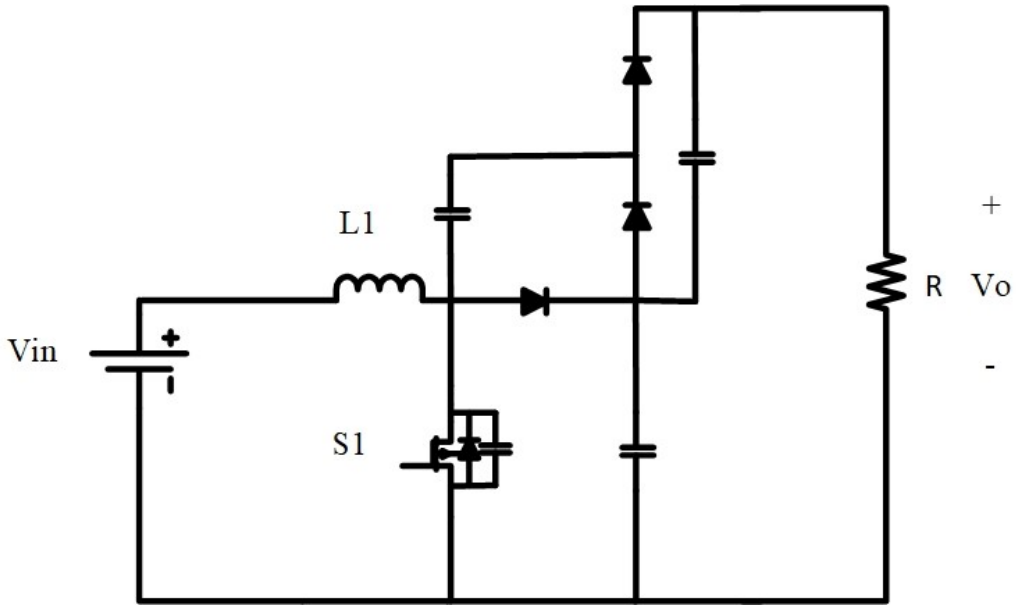


Fig. 1.9: Multilevel DC-DC Boost Converter [13].

It can be seen that when the switch is on, the inductor is charging and capacitor 1 is discharging on capacitor 4 and capacitor 5 is discharging on capacitor 3. When the switch is off, the inductor discharges on capacitor 1 and capacitor 4 discharges on capacitor 2 and capacitor 3 discharges on the load.

$$Vo = \frac{n.Vin}{1-D} \tag{1.1}$$

The main issue of this converter is that when a capacitor switches on another capacitor, it causes an instantaneous voltages change on the other capacitor which causes a severe current spike/transient. The current transient causes severe conduction and switching losses.

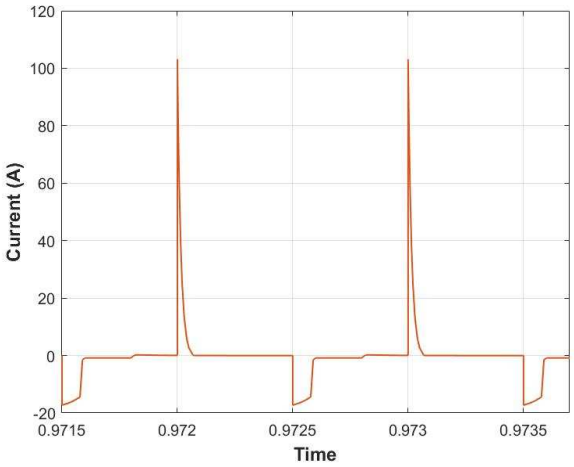


Fig. 1.10: Capacitor Current Transient Multilevel DC-DC Boost Converter [13].

The reason that this is applicable in practice is that the current transient is limited by the parasitic resistance of the capacitor. However, the losses of the converter cannot be within a reasonable range. In order to improve this topology, the current transient must be eliminated. The converter in [14] added an inductor in the path between the two capacitors. The Configuration becomes:

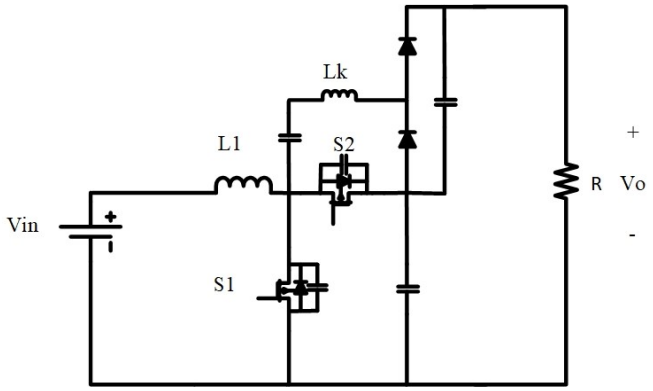


Fig. 1.11: Multilevel boost with intermediate inductor to eliminate current transients [14].

The inductor successfully eliminates the current transient and brings the efficiency within a reasonable range. However, the inductor causes a voltage drop on both the transitionary capacitor and the second output capacitor. In order to bring the voltage from 36 V to desired levels of 400 V with reasonable duty cycle switching, more than two levels are needed.

$$Vo = \frac{n.Vin}{1-D} - \Delta V \tag{1.2}$$

1.3.2 Coupled inductor Based DC-DC converters

In the literature, many topologies have been developed that incorporate coupled inductors with switched capacitor converters. A detailed overview of these topologies is shown in [15] [16] [17] [18]. In [19], a coupled inductor is used as the primary energy transfer element for the secondary capacitor.

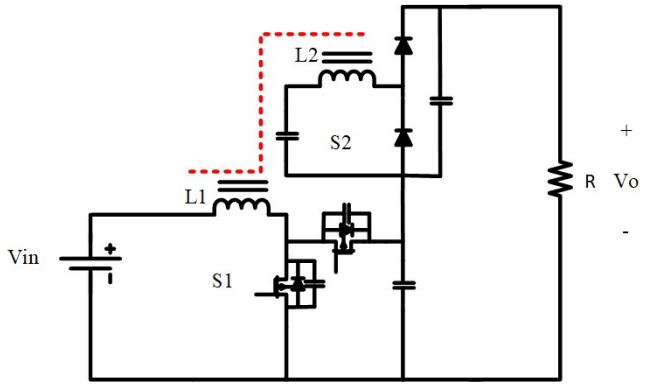


Fig. 1.12: Multilevel boost with coupled inductor rectifier cell [19].

There is no high transient current in this configuration because it operates as a voltage-doubler rectifier. However, since the coupled inductor is entirely isolated and connected to the output, it is the only energy transfer element responsible for charging the output capacitor which means that the turn's ratio requirement should be high enough to charge the capacitor to the desired level. By connecting the secondary coupled inductor to the main switch with reversed polarity, the coupled inductor and the first output capacitor are both responsible for charging the second capacitor. Which means that the second capacitor will have the added voltage value of both the coupled inductor voltage and the first capacitor's voltage allowing a smaller capacitor for the same amount of energy needed.

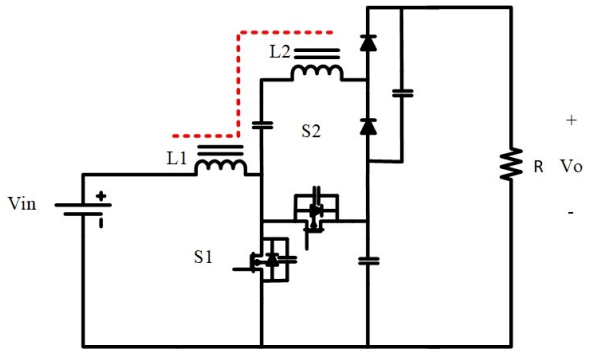


Fig. 1.13: Multilevel boost with coupled inductor cell connected to the first output capacitor.

The turn's ratio requirement will be reduced and the voltage drop in the second output capacitor will be eliminated. In fact, the second output capacitor will always have a higher voltage than the first output capacitor. This approach is achieved in [20], [21] and [22].

$$Vo = Vco1 + Vco2 = Vin\frac{KN+2}{1-D} \tag{1.3}$$

It can be seen that all these topologies use the input inductor for magnetic coupling. This will produce a high input current ripple for the coupled inductor. The high ripple will affect the lifespan of batteries. It will also make a harder MPPT tracking for PV panels.

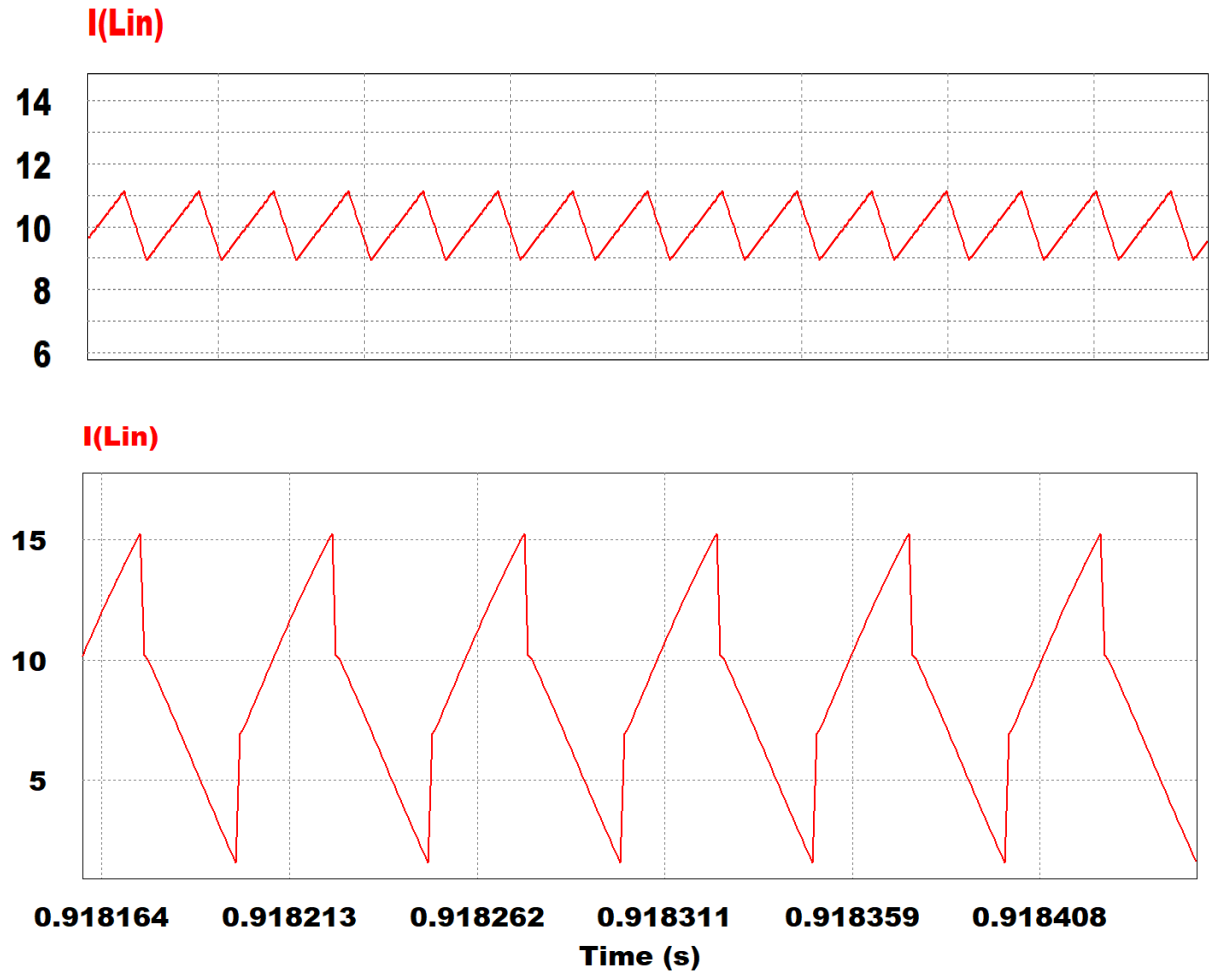


Fig. 1.14: Uncoupled vs Coupled input inductors' current ripple.

SEPIC based dc-dc converters provide two inductors and the coupling of the input inductor could be avoided providing low ripple input current. In [23], a modified SEPIC converter is presented.

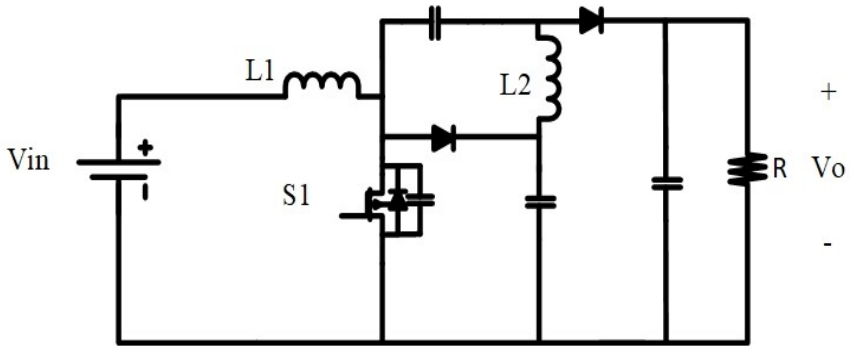


Fig. 1.15: Modified SEPIC Converter [23].

This converter provides voltage gain higher than that of the conventional boost which is highly desirable. However, the voltage gain is still needed to be higher for grid interface and high duty cycle and voltage stress would be present without using any multiplier cells.

$$Vo = \frac{1+D}{1-D} Vin \tag{1.4}$$

In [24] a multiplier cell is applied to the previous modified SEPIC. The new converter has a low ripple input and a voltage gain that is capable of stepping-up the voltage to the desired level at a reasonable duty cycle.

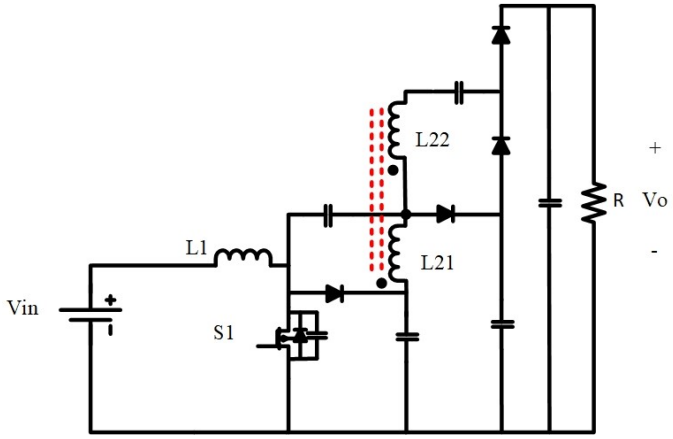


Fig. 1.16 Modified SEPIC Converter with a multiplier cell [24].

$$Vo = \frac{2+n+D}{1-D} Vin \tag{1.5}$$

Another Method to have a low ripple in the input current is using cascaded boost converter connection. Cascaded (or Quadratic) boost converters with multiplier cells have been reported in

the literature. In [25], a quadratic boost converter with a coupled inductor to increase the voltage gain is shown.

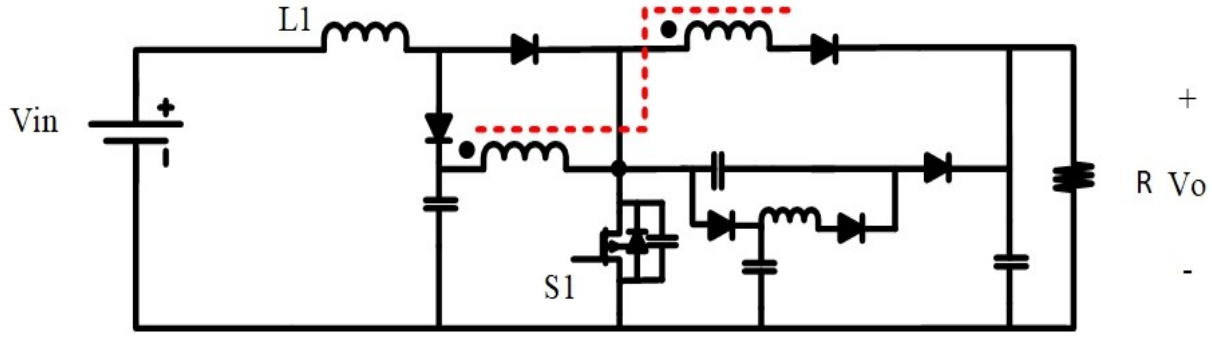


Fig. 1.17 Quadratic Boost Converter with Coupled Inductor [25].

This configuration increases the voltage gain but does not decrease the voltage stress on the switch. Therefore, a snubber cell is added to reduce the switching losses. In [26], a Quadratic boost DC-DC converter with a multiplier cell that charges two capacitors in parallel and discharges them in series.

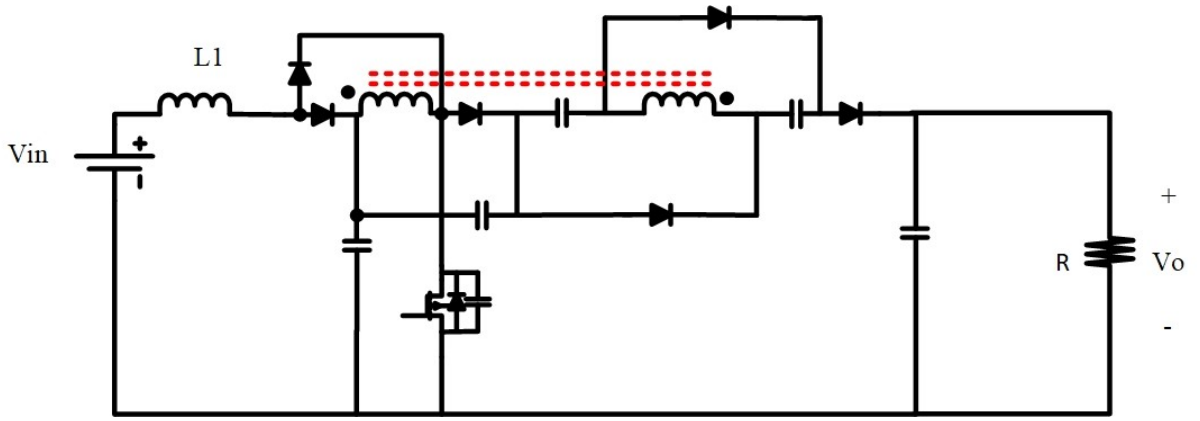


Fig. 1.18 Quadratic Boost Converter with Multiplier Cell [26].

This converter has a higher voltage gain than the previous SEPIC based converter on the expense of increased component count. In fact, all these high voltage gain converters come at the expense of high components count. In addition, the complexity of the converter increases if a low ripple input current is desired.

1.4 Problem Description

Development of PV converters that have highly efficient performance and versatile functions to extract maximum power available in an efficient manner is essential with the increased PV installation rate. In addition, utilities require galvanic isolation between the source and the grid. Most of the development and research solutions for isolated solutions present converters that require highly rated switches and diodes that are more expensive. The ones that offer reduced rating switches are not isolated. In addition, the vast majority of these High voltage DC-DC converters are not modeled for control and stability purposes. The reason for that is because of the difficulty of defining the state equations of the coupled inductor [27]. PV converters require efficient converters that are isolated and have reduced cost. The cost can be reduced by utilizing a topology that uses smaller and cheaper switches and diodes. Proper modelling and control design is vital for implementing new converters into practical use therefore any new topology should have an established model for proper control which is not the case for the vast majority of new proposed solutions in the literature.

1.5 Motivation

The motivations of this research can be summarized in these following points:

1. The need for highly efficient high voltage gain DC-DC converters for PV integration
2. The need for proper modelling and control of new and emerging high gain DC-DC converters
3. The possibility of size and cost reduction of PV systems.

1.6 Possible ways of improvement and proposed system

A possible way to improve on previously discussed topologies is to increase the output voltage and reduce the input current. This can be done by integrating multiplier cells to SEPIC-based DC-DC converters. The SEPIC converter has an input inductor that when sized properly, can effectively reduce the input ripple. This concept has been implemented in our research in [31]. The main idea in this converter is that the multiplier cell is optimized to charge two capacitors instead of one. This multiplier cell can be

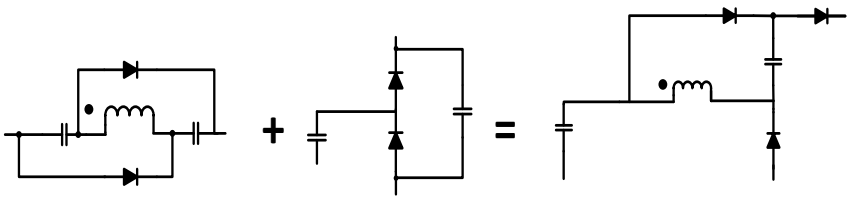


Fig. 1.19 Improved multiplier cell. © 2018 IEEE

Integrated with the second inductor of the SEPIC converter to increase the voltage range of the converter. In order to get the most out of it, it could be integrated the modified SEPIC that is mentioned in [23]. The resulting converter would then be as follows:

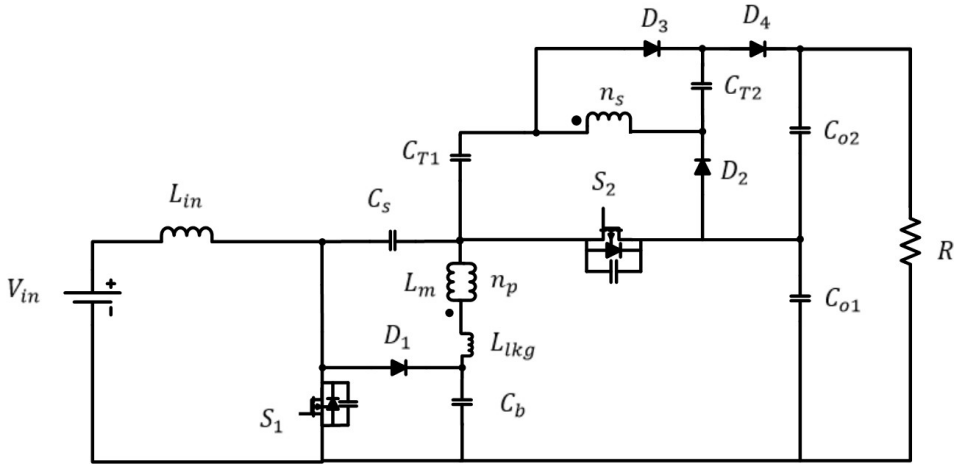


Fig. 1.20 Proposed SEPIC based converter [31]. © 2018 IEEE

The operation of the proposed converter will consist of six switching states as seen in [31]:

1. Mode 1 (t0-t1):

In this state, the main inductor is being charged, and D4 is still conducting with a decreasing rate. Similarly, secondary current of the coupled inductor is decreasing, and the leakage current is decreasing the reach the magnetizing current I Lm. Current through the capacitor is also decreasing due to the effect of capacitor Cb. The end of this switching period is when the diode D4 is off.

2. Mode 2 (t1-t2):

During this state, Capacitors Cs and CT1 are being charged and magnetizing current I Lm reverses its rate of change. During this state, the voltage loop equations are as follows:

$$V_{Lm} + V_{lkg} = V_{Cb} - V_{Cs} \tag{1.6}$$

$$V_{CT1} = V_{Co1} + V_{ns} - V_{Cs} \tag{1.7}$$

And from equations (1) and (2) we find that:

$$\frac{V_{ns}}{n} = V_{Lm} = V_{Cb} - V_{Cs} - V_{lkg} \tag{1.8}$$

3. Mode 3 (t2-t3):

When Capacitor CT1 is fully charged, diode D3 becomes forward biased, and CT2 is being charged by the secondary of the inductor. Loop equations in this case are:

$$V_{CT2} = V_{ns} = nV_{Lm} = V_{Cb} - V_{Cs} - V_{lkg} \tag{1.9}$$

4. Mode 4 (t3-t4):

During this state, S1 is turned off, and S2 is turned on. Diode d3 starts decreasing current, and the leakage current starts to decrease to equal the magnetizing current I Lm. Capacitor Co1 is being charged. The end of the switching state is when diode D3 turns off.

5. Mode 5 (t4-t5):

Diode D3 is turned off, and diode D4 is turned on, and Capacitor Co2 is being charged by Capacitor CT1, CT2, and the secondary of the coupled inductor. The end of this period is when the current of S2 reverses its direction. Voltage loop equations for this state are as follows:

$$V_{Co1} = V_{in} + V_{Lin} + V_{Cs} \tag{1.10}$$

$$V_{Co2} = V_{CT1} + V_{ns} + V_{CT2} \tag{1.11}$$

$$V_{ns} = nV_{Lm} = V_{Cs} - V_{lkg} \tag{1.12}$$

Mode 6 (t5-t6): D1 is turned on, and Cb is being charged by Lin:

$$V_{Cb} = V_{in} + V_{Lin} \tag{1.13}$$

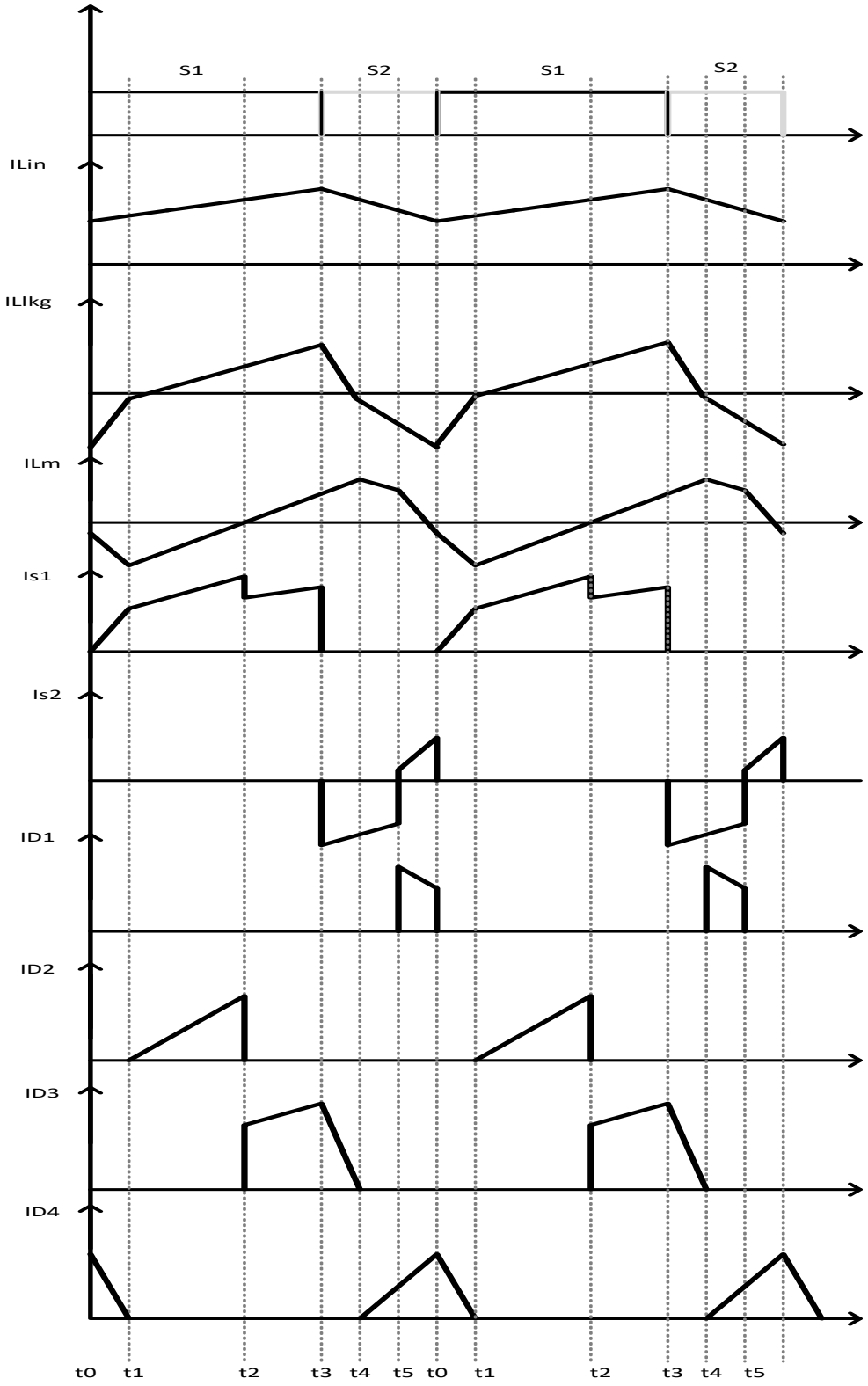


Fig. 1.21 Switching Scheme of the proposed converter.

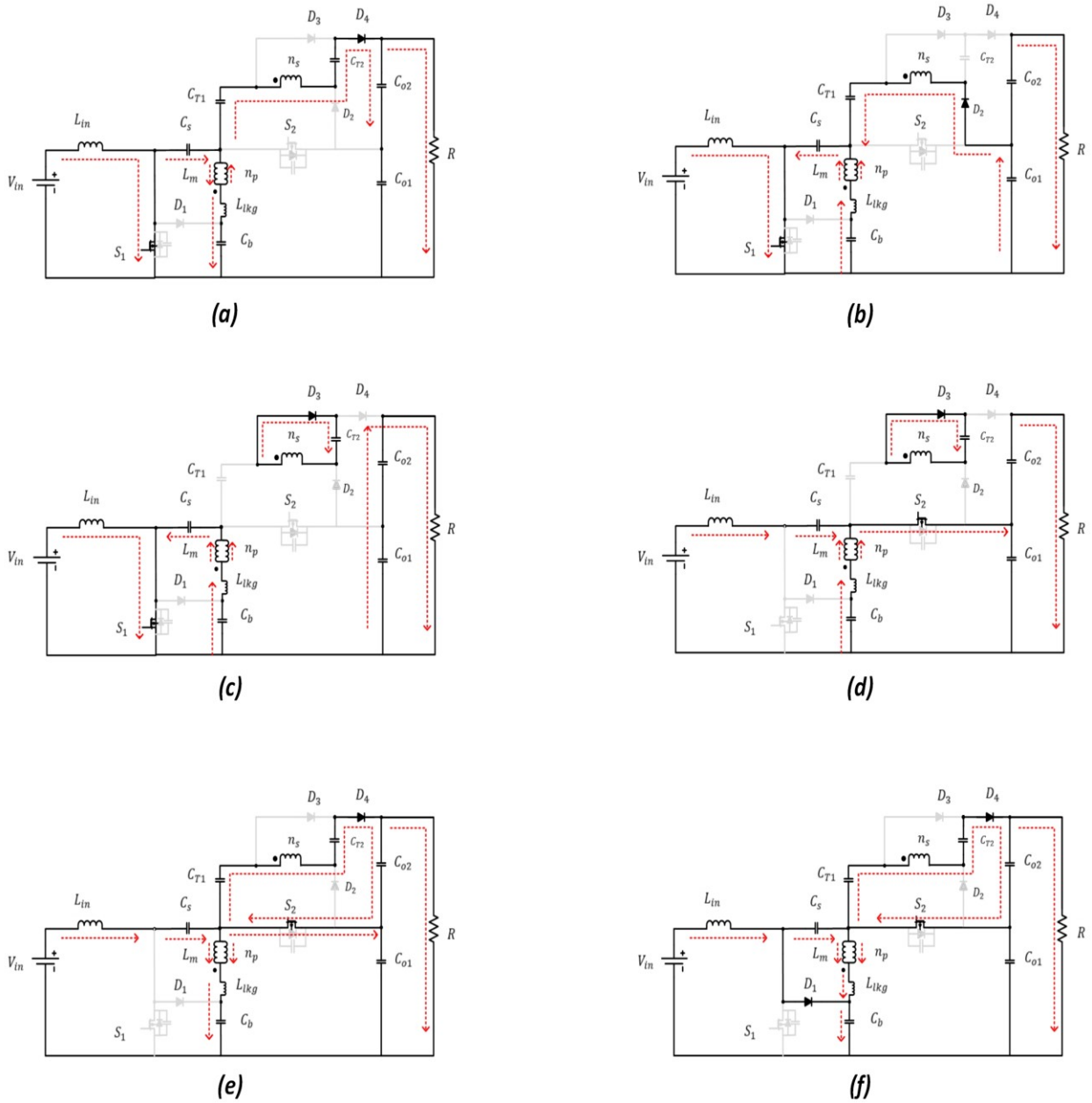


Fig. 1.22 Switching states of the proposed converter: a) mode(t0-t1). b) mode(t1-t2). c) mode(t2-t3). d) mode(t3-t4). e) mode(t4-t5). f) mode(t5-t0).

The output voltage of the converter is

$$V_o = V_{Co1} + V_{Co2} = \frac{2(1+D) + 2kn(1-D)}{1-D} V_{in} \tag{1.14}$$

Where k is the coupling factor and n is the turns' ratio. The next figure will show how this converter's voltage gain will compare to other presented topologies

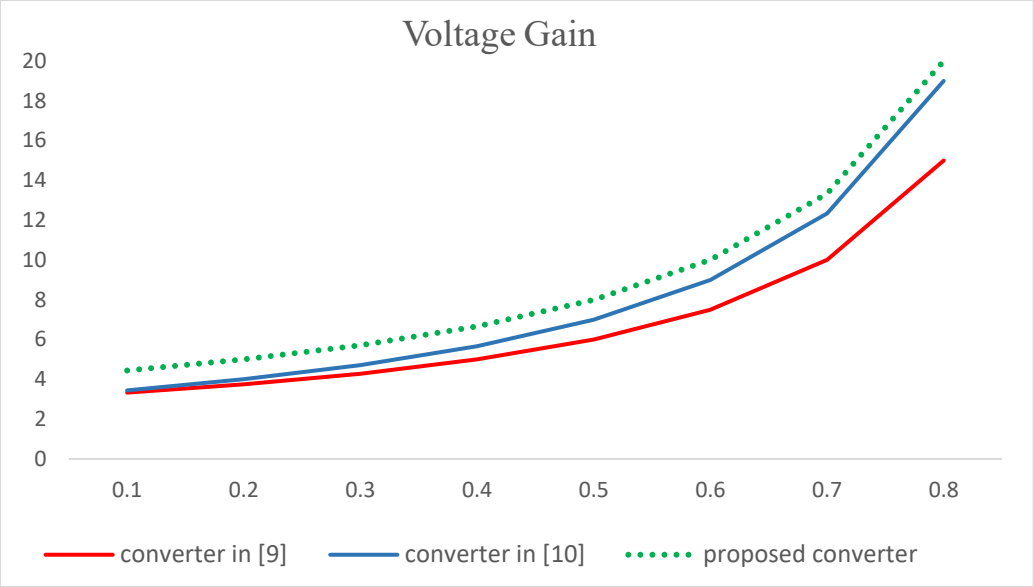


Fig. 1.23 Voltage gain Comparison [32].

It can be seen that this proposed topology improves the voltage gain significantly. However there two issues facing this topology. The first thing is that the main switch is hard switched. The second issue it that there is no improvement in the duty cycle. That means in order to get a 400 V output, the duty cycle has to be at least 0.7. In order to counteract the hard switching in the proposed topology, the converter is modified to have synchronous switch operation in the SEPIC cell. A series inductor is added to extend the soft switching range. The resulting converter would be as follows [32]:

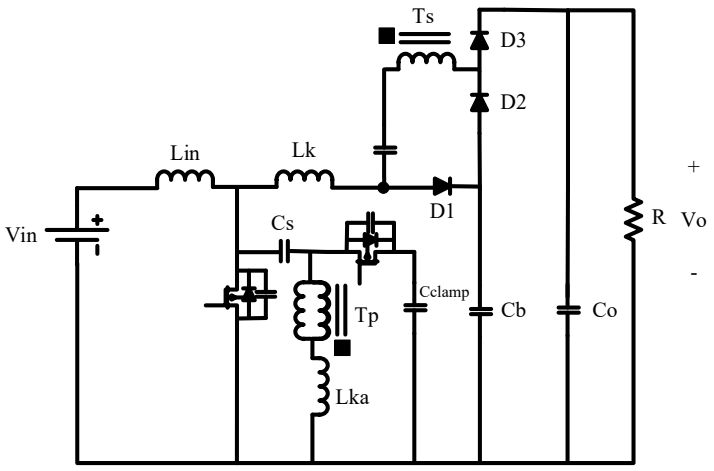


Fig. 1.24 Proposed DC-DC converter with extended soft switching operation [32].

By doing so, the number of components is reduced and the active switches would have soft switching operation. The converter has five operating modes. The switches combine the operation of the conventional boost cell with a transformer-based multiplier cell that will reflect the voltage of another boost cell to the output voltage as shown in figure 1. In addition, the switched capacitor is softened using the leakage inductance of the transformer. The additional inductor L_k introduces zero-voltage-switching to the main switches.

1. First switching period (mode 1):

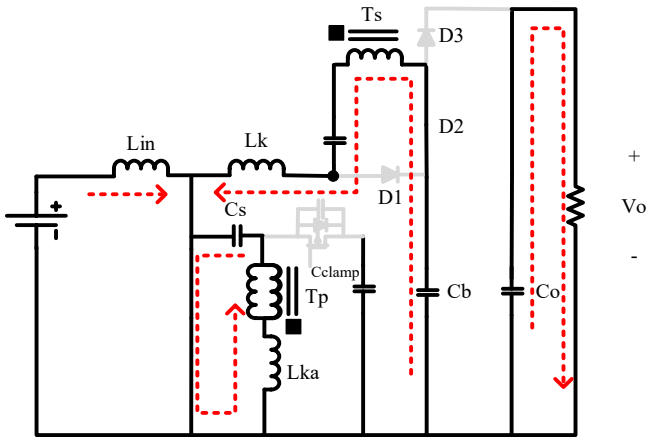


Fig. 1.25 First switching period [32].

In this mode, switch 1 is on and switch 2 is off as shown in figure 2. At the same time, D2 is on and the other two diodes are off. The Capacitor C_s starts to excite the transformer. Capacitor C_b and the transformer cell start to charge the capacitor softly due to the existence of the leakage inductance L_{ka} and the additional inductorL_k. The input inductor is also being excited, and the output capacitor is discharging on the load. KVL and KCL equations describing this mode are:

$$V_{Lin} = V_{in} \tag{1.15}$$

$$V_{Lm} = V_{Cs} * k \tag{1.16}$$

$$V_{Lk} + V_{Lka} = \frac{V_{Cb}+V_{Cs}*k-V_{CT}}{L_K+L_{Ka}} \tag{1.17}$$

$$I_{Cs} = -I_{Lk} + I_{Lm} \tag{1.18}$$

$$I_{Cb} = -I_{Lk} \tag{1.19}$$

$$I_{CT} = I_{Lk} \tag{1.20}$$

$$I_{Co} = -\frac{V_{Co}}{R} \tag{1.21}$$

$$I_{Cclamp} = 0 \tag{1.22}$$

2. Second switching period (mode 2):

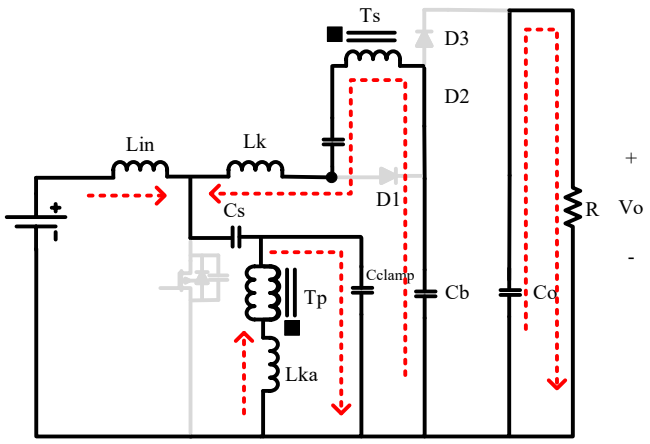


Fig. 1.26 Second switching period [32].

At the beginning of this state, switch 1 is turned off. Capacitor C_{clamp} will clamp I_{Lka} and the current will start decreasing. Diode D2 will continue conducting until the current reaches zero at the end of this period. KVL and KCL equations describing this mode are:

$$V_{Lin} = V_{in} - V_{Cs} - V_{Cclamp} \tag{1.23}$$

$$V_{Lm} = -V_{Cclamp} * k \tag{1.24}$$

$$V_{Lk} + V_{Lka} = \frac{V_{Cb} - V_{Cs} - V_{Cclamp} * (k+1) - V_{CT}}{L_K + L_{Ka}} \tag{1.25}$$

$$I_{Cs} = I_{Lin} + I_{Lk} \tag{1.26}$$

$$I_{Cclamp} = I_{Lin} + 2 * I_{Lka} + I_{Lm} \tag{1.27}$$

$$I_{Cb} = -I_{Lk} \tag{1.28}$$

$$I_{CT} = I_{Lk} \tag{1.29}$$

$$I_{Co} = -\frac{V_{Co}}{R} \tag{1.30}$$

3. Third switching period (mode 3):

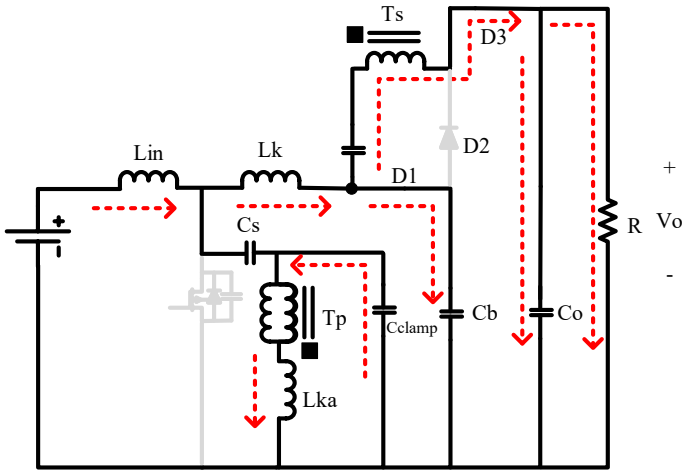


Fig. 1.27 Third switching period [32].

In this switching mode, the current in diode 2 reaches zero and it turns off. Diodes 1 and 3 turns on. The output capacitor is being charged softly by CT and the transformer cell due to the existence of L_{ka} in the path of charging. KVL and KCL equations describing this mode are:

$$V_{Lin} = V_{in} - V_{Cs} - V_{Cclamp} \tag{1.31}$$

$$V_{Lm} = -V_{Cclamp} * k \tag{1.32}$$

$$V_{Lka} = \frac{V_{Cb}+V_{CT}+V_{Cclamp}*(k)-V_{Co}}{L_{Ka}} \tag{1.33}$$

$$V_{Lk} = \frac{V_{Cs}+V_{Cclamp}-V_{Cb}}{L_K} \tag{1.34}$$

$$I_{Cs} = I_{Lin} + I_{Lk} \tag{1.35}$$

$$I_{Cclamp} = I_{Lin} + I_{Lk} + I_{Lka} + I_{Lm} \tag{1.36}$$

$$I_{Cb} = -I_{Lk} + I_{Lka} \tag{1.37}$$

$$I_{CT} = I_{Lka} \tag{1.38}$$

$$I_{Co} = -I_{Lka} - \frac{V_{Co}}{R} \tag{1.39}$$

4. Fourth switching period (mode 4):

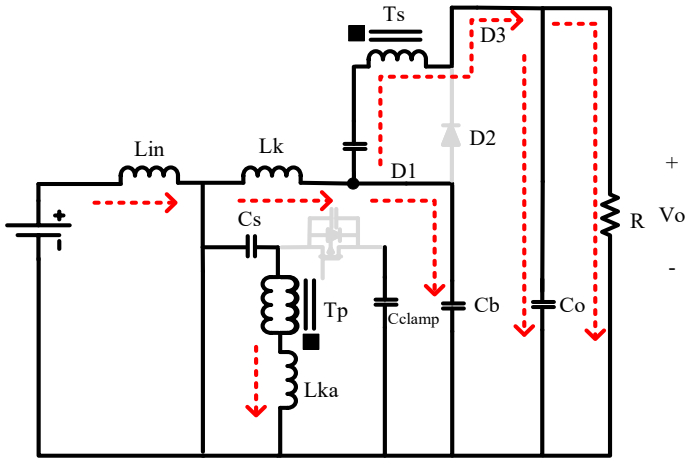


Fig. 1.28 Fourth switching period [32].

In this switching state, switch 1 is turned on and switch 2 is turned off. Diodes 1 and 3, however, are still conducting and their currents are decreasing until they reach zero at the end of this period. KVL and KCL equations describing this mode are:

$$V_{Lin} = V_{in} \tag{1.40}$$

$$V_{Lm} = V_{Cs} * k \tag{1.41}$$

$$V_{Lka} = \frac{V_{Cb} + V_{CT} - V_{Cs}*(k) - V_{Co}}{L_{Ka}} \tag{1.42}$$

$$V_{Lk} = \frac{-V_{Cb}}{L_K} \tag{1.43}$$

$$I_{Cs} = -I_{Lka} \tag{1.44}$$

$$I_{Cclamp} = 0 \tag{1.45}$$

$$I_{Cb} = -I_{Lk} + I_{Lka} \tag{1.46}$$

$$I_{CT} = I_{Lka} \tag{1.47}$$

$$I_{Co} = -I_{Lka} - \frac{V_{Co}}{R} \tag{1.48}$$

5. Fifth switching period (mode 5):

In this state, D3 current reaches zero and it turns off and diode 1 is still conducting. Capacitor C_b takes the energy in L_k and the output capacitor C_o discharges its energy on the load.

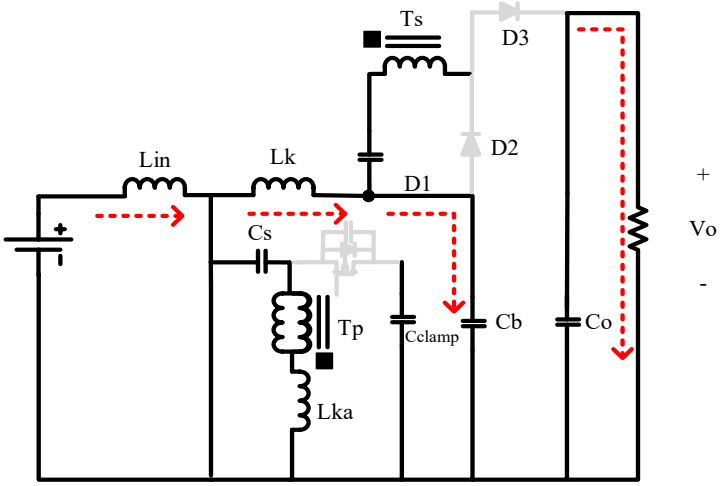


Fig 1.29 Fifth switching period [32].

KVL and KCL equations describing this mode are:

$$V_{Lin} = V_{in} \tag{1.49}$$

$$V_{Lm} = V_{Cs} * k \tag{1.50}$$

$$V_{Lka} = 0 \tag{1.51}$$

$$V_{Lk} = \frac{-V_{Cb}}{L_K} \tag{1.52}$$

$$I_{Cs} = 0 \tag{1.53}$$

$$I_{Cclamp} = 0 \tag{1.54}$$

$$I_{Cb} = -I_{Lk} \tag{1.55}$$

$$I_{CT} = 0 \tag{1.56}$$

$$I_{Co} = -\frac{V_{Co}}{R} \tag{1.57}$$

Waveforms of the converter variables can be seen in figure 1.28.

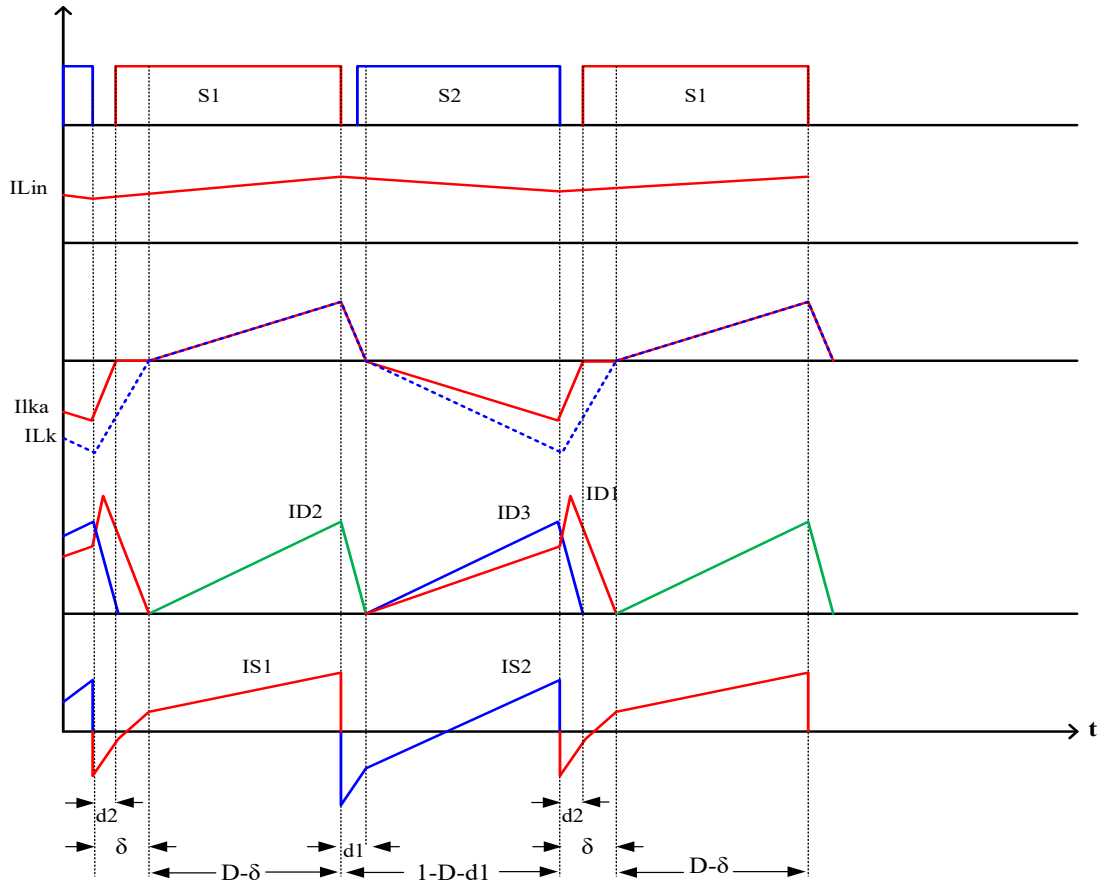
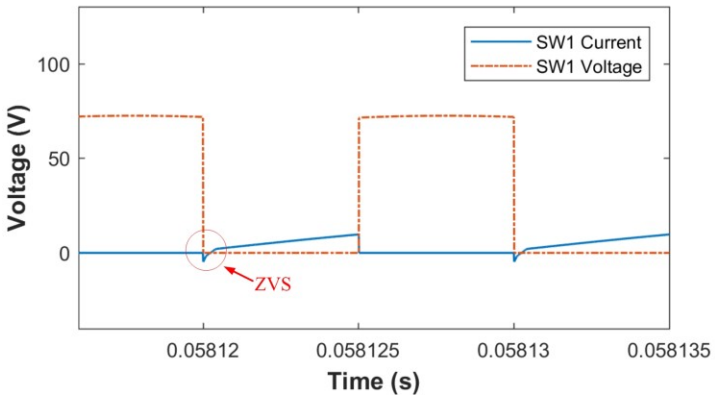


Fig 1.30 Waveforms of the converter [32].

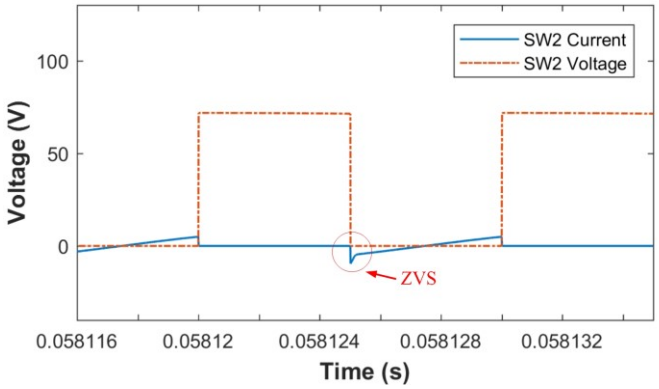
An examination of the converter's performance is presented to show the expected advantages and how switch operation is improved by the series inductor. The parameters used are as follows in Table I. The simulation test examines the ZVS operation of the switches and the ZCS operation of the diodes.

Table 1.1: converter parameters

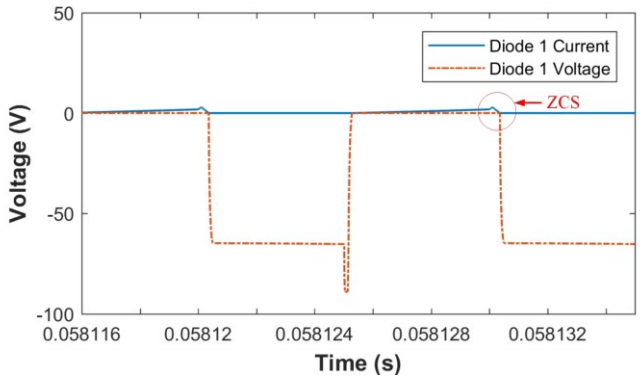
Parameter	***Value***
V_{in}	36 V
L_{in}	47uH
L_m	500uH
L_k	6uH
L_{ka}	3uH
$Capacitors$	14.1uF
D	0.5
f	100kHz
R	420Ω



(a)



(b)



(c)

Fig 1.31 (a) ZVS of active switch 1. (b) ZVS of active switch 2. (c) ZCS of diode 1 [32].

It can be seen that the second proposed option provides ZVS for all the active switches and the inductor Lk extends the soft switching range based on its chosen value. However, the extension of the soft switching range comes at the cost of the output voltage gain reduction. Due to the

delay of the diode turn off, the output voltage gain of the converter is reduced. Therefore, there is a tradeoff that needs to be considered if this approach is to be used. Another issue is the duty cycle. In order to reduce the conduction loss, the duty cycle has to be reduced as well. In both approaches, there is no galvanic isolation in the DC stage. Therefore, in order to be connected to the grid, a 60 Hz isolation transformer is required. A novel approach can be developed by integrating multiplier cells to isolated DC-DC topologies. In order to simplify the design and reduce the rated component size, a 1:1 transformer cell can be used. This approach has never been tested before. Therefore a new isolated DC-DC converter can be implemented. The proposed system combines high voltage gain and low ripple input current along with reduction of component ratings. It also provides galvanic isolation without increasing the stress of the secondary side components. The transformer's ratio is 1:1 which eliminates the need to have different insulation levels and eliminates the need for different windings and also simplifies the winding layout for the transformer. By incorporating isolated multiplier cells, the output voltage can be increased without increasing the voltage stress on output switches.

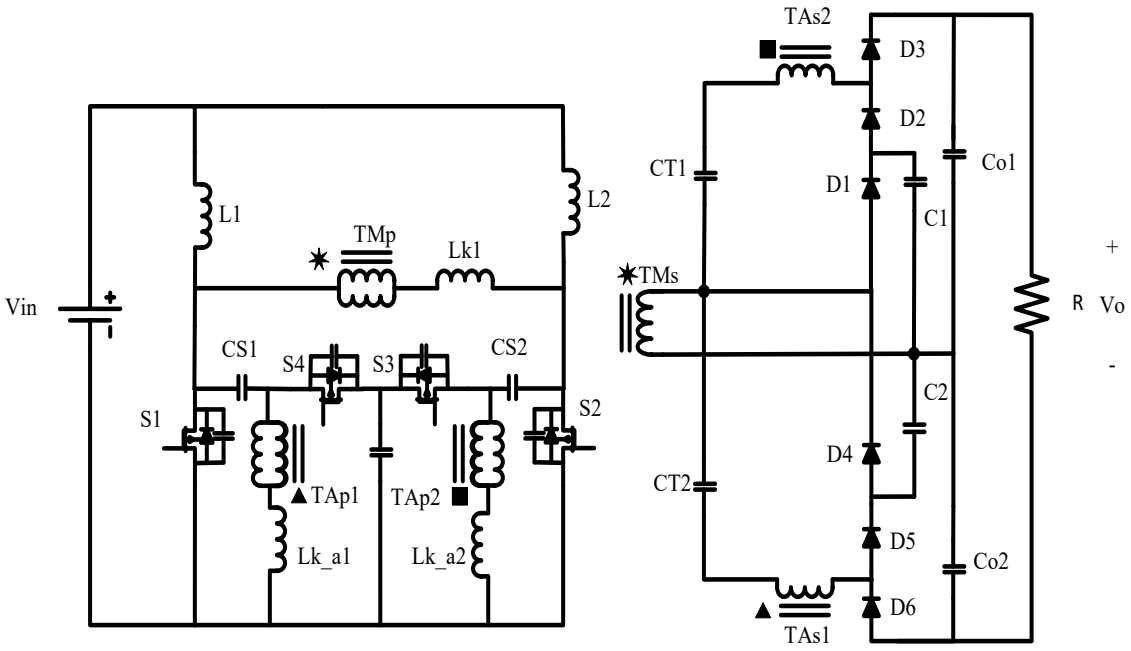


Fig. 1.32 Proposed Converter Configuration [33].

The 1:1 ratio will help minimize the voltage stress on diodes d2, d3, d5, and d6. By adopting this configuration, a very high voltage can be produced by using very low rated components [33]. In

addition, since the two cells will share the duty cycle burden, both switching and conduction losses will be reduced with the reduction of the duty cycle. The next Section will detail the theory of operation for the proposed converter. After that, the design equations and how this converter compares to other works in terms of voltage gain and switch voltage stress. Experimental results from a 450 laboratory prototype are then presented in the next section and an efficiency study is then presented. Finally, a conclusion with future work aspects and considerations will be discussed.

CHAPTER 2

THEORY OF OPERATION

The switching states of the converter and the equations describing each switching state are described next as mentioned in [33].

2.1 Switching states of the converter

A. First state; (t0-t1) S1 -> on s3 -> on s2 -> off s4 -> off:

In this case, Diodes 1, 3, and 5 are on, and Diodes 2, 4 and 6 are off. C1 is being charged by the main transformer and Co1 is being charged by the main transformer, CT1, and the auxiliary transformer. On the other hand Capacitor CT2 is being charged by the main transformer, the auxiliary transformer and by C2. Capacitor Co2 is discharging on the load.

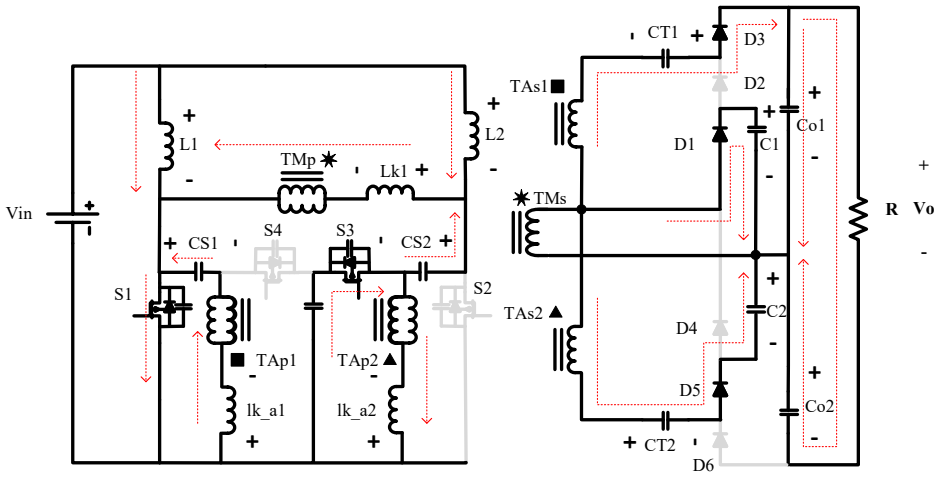


Fig. 2.1 First switching state [33].

KVL equations during this state are:

$$V_{L1} = V_{in} \tag{2.1}$$

$$V_{lk1} = V_{Cs2} + V_{Clamp} - \frac{1}{n}(V_{C1}) \tag{2.2}$$

$$V_{L2} = V_{in} - V_{Cs2} - V_{clamp} \tag{2.3}$$

$$V_{lka-1} = V_{Cs1} - \frac{1}{na}(V_{Co1} - V_{CT1} - V_{C1}) \tag{2.4}$$

$$V_{lka-2} = V_{clamp} - \frac{1}{na}(V_{CT2} - V_{C2} - V_{C1}) \quad (2.5)$$

Where na is the turn's ratio for the auxiliary transformers and the KCL equations during this state are:

$$I_{Cs1} = -I_{Lka-1} \quad (2.6)$$

$$I_{Cs2} = I_{L2} - I_{Lk1} \quad (2.7)$$

$$I_{C1} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-1} + I_{Lka-2}) \quad (2.8)$$

$$I_{CT1} = -\frac{1}{na}(I_{Lka-1}) \quad (2.9)$$

$$I_{CT2} = \frac{1}{na}(I_{LKa-2}) \quad (2.10)$$

$$I_{Co1} = -\frac{1}{na}(I_{Lka-1}) - I_o \quad (2.11)$$

$$I_{Co2} = -I_o \quad (2.12)$$

CS1 is now being discharged into the auxiliary transformer multiplier cell and the clamp capacitor, as well as CS2, are completing their charging process from the previous state. After the capacitors are charged and in the same switching state, the clamp capacitor starts feeding the auxiliary transformer and Cs2 starts discharging into the main transformer.

B. Second state; (t1-t2) S1 -> off s3 -> on s2 -> off s4 -> on:

In this case, S1 turns off and the main transformer current starts circulating through s3 and s4. The current of the auxiliary transformer 1 descends to zero and diode D3 turns off. Capacitors Cs1 and clamp capacitor are charged and the capacitor Cs2 continues to discharge in a decreasing manner. In other words, the capacitor continues discharging but at a slower rate.

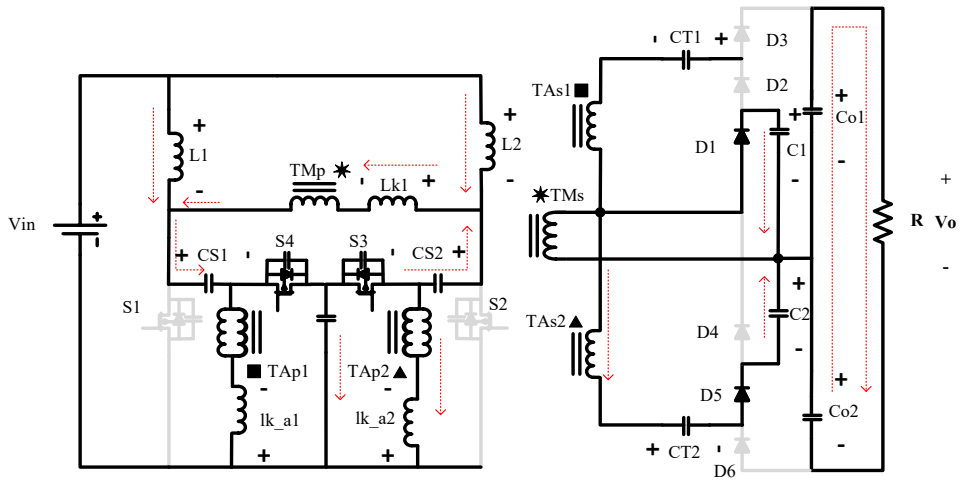


Fig. 2.2 Second switching state [33].

The capacitor CT2 continues to be charged by C2, the main transformer, and the auxiliary transformer 2. KVL equations during this switching state are:

$$V_{L1} = V_{in} - V_{Cs1} - V_{clamp} \tag{2.13}$$

$$V_{lk1} = -\frac{1}{n}(V_{C1}) \tag{2.14}$$

$$V_{L2} = V_{in} - V_{Cs2} - V_{clamp} \tag{2.15}$$

$$V_{lka-1} = 0 \tag{2.16}$$

$$V_{lka-2} = V_{clamp} - \frac{1}{na}(V_{CT2} - V_{C2} - V_{C1}) \tag{2.17}$$

And the KCL during this switching state is:

$$I_{Cs1} = I_{L1} + I_{Lk1} \tag{2.18}$$

$$I_{Cs2} = I_{L2} - I_{Lk1} \tag{2.19}$$

$$I_{C1} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-1}) \tag{2.20}$$

$$I_{CT1} = 0 \tag{2.21}$$

$$I_{CT2} = \frac{1}{na}(I_{LKa-2}) \tag{2.22}$$

$$I_{Co1} = I_{Co2} = -I_o \tag{2.23}$$

C. Third switching state; (t2-t3) S1 -> off s3 -> off s2 -> on s4 -> on:

When S3 turns off, the output of the capacitor of S3 starts charging and the capacitor of S2 starts discharging. When the capacitor of S2 is fully discharged, its body diode starts conducting providing a ZVS condition for switch S2 to be turned on at the end of this switching period.

D. Fourth Switching state; (t3-t4) S1 -> off s3 -> off s2 -> on s4 -> on:

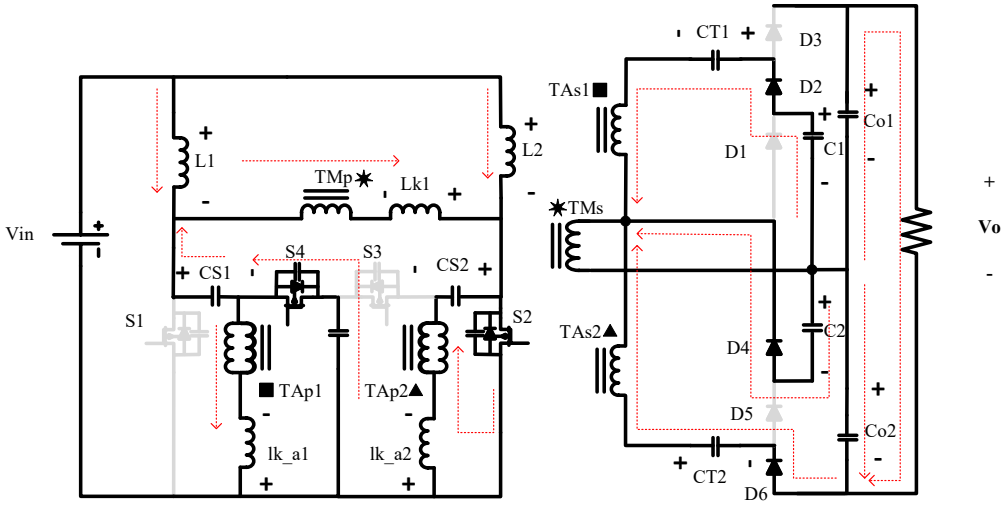


Fig. 2.3 Fourth switching state [33].

In this case, Switch two is turned on. Diode 2, 4, and 6 are on, and Diodes 1, 3 and 5 are off. C2 is being charged by the main transformer and Co2 is being charged by the main transformer, CT2, and the auxiliary transformer. On the other hand Capacitor CT1 is being charged by the main transformer, the auxiliary transformer and by C1. Capacitor Co1 is discharging on the load. KVL equations during this state are:

$$V_{L2} = V_{in} \tag{2.24}$$

$$V_{lk1} = V_{Cs1} + V_{Clamp} - \frac{1}{n}(V_{C2}) \tag{2.25}$$

$$V_{L1} = V_{in} - V_{Cs1} - V_{clamp} \tag{2.26}$$

$$V_{lka-2} = V_{Cs2} - \frac{1}{na}(V_{Co2} - V_{CT2} - V_{C2}) \tag{2.27}$$

$$V_{lka-1} = V_{clamp} - \frac{1}{na}(V_{CT1} - V_{C1} - V_{C2}) \tag{2.28}$$

And the KCL equations during this state are:

$$I_{Cs2} = -I_{Lka-2} \tag{2.29}$$

$$I_{Cs1} = I_{L1} - I_{Lk1} \tag{2.30}$$

$$I_{C2} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-1} + I_{Lka-2}) \tag{2.31}$$

$$I_{CT2} = -\frac{1}{na}(I_{Lka-2}) \tag{2.32}$$

$$I_{CT1} = \frac{1}{na}(I_{LKa-1}) \tag{2.33}$$

$$I_{Co2} = -\frac{1}{na}(I_{Lka-2}) - I_o \tag{2.34}$$

$$I_{Co1} = -I_o \tag{2.35}$$

CS2 is now being discharged into the auxiliary transformer multiplier cell and the clamp capacitor, as well as CS1, are completing their charging process from the previous state. After the capacitors are charged and in the same switching state, the clamp capacitor starts feeding the auxiliary transformer and Cs1 starts discharging into the main transformer.

E. Fifth Switching state; (t4-t5) S1 -> off s3 -> on s2 -> off s4 -> on:

In this case, S2 turns off and the main transformer current starts circulating through s3 and s4. The current of the auxiliary transformer 2 descends to zero and diode D6 turns off. Capacitors Cs2 and clamp capacitor are charged and the capacitor Cs1 continues to discharge in decreasing order. The capacitor CT1 continues to be charged by C1, main transformer, and the auxiliary transformer 1. KVL equations during this switching state are:

$$V_{L2} = V_{in} - V_{Cs2} - V_{clamp} \tag{2.36}$$

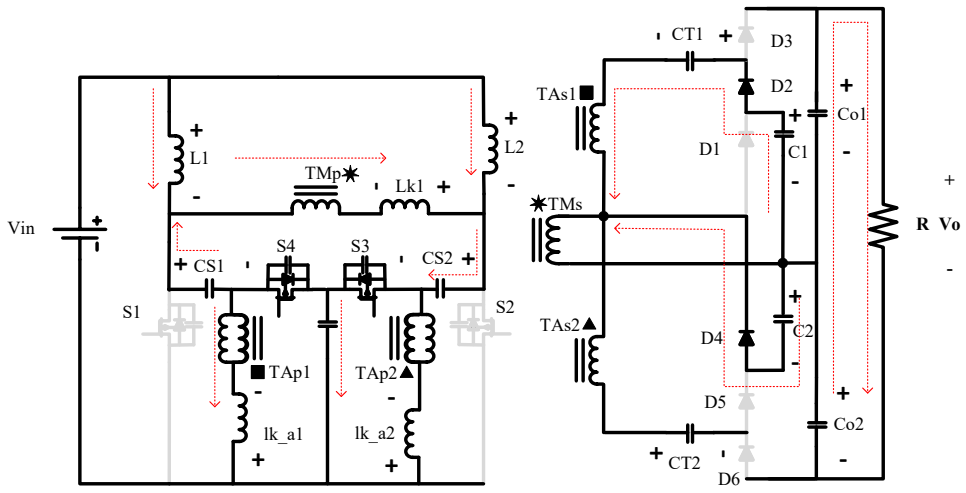


Fig. 2.4 Fifth switching state [33].

$$V_{lk1} = -\frac{1}{n}(V_{C2}) \tag{2.37}$$

$$V_{L1} = V_{in} - V_{Cs1} - V_{clamp} \tag{2.38}$$

$$V_{lka-2} = 0 \tag{2.39}$$

$$V_{lka-1} = V_{clamp} - \frac{1}{na}(V_{CT1} - V_{C1} - V_{C2}) \tag{2.40}$$

And the KCL during this switching state is:

$$I_{Cs2} = I_{L2} + I_{Lk1} \tag{2.41}$$

$$I_{Cs1} = I_{L1} - I_{Lk1} \tag{2.42}$$

$$I_{C2} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-2}) \tag{2.43}$$

$$I_{CT2} = 0 \tag{2.44}$$

$$I_{CT1} = \frac{1}{na}(I_{LKa-1}) \tag{2.45}$$

$$I_{Co1} = I_{Co2} = -I_o \tag{2.46}$$

F. Sixth switching state; (t5-t6) S1 -> on s3 -> on s2 -> off s4 -> off

When S4 turns off, the output of the capacitor of S4 starts charging and the capacitor of S1 starts discharging. When the capacitor of S1 is fully discharged, its body diode starts conducting providing a ZVS condition for switch S1 to be turned on at the end of this switching period. The waveforms that describe the operation of this converter are presented in figure 7:

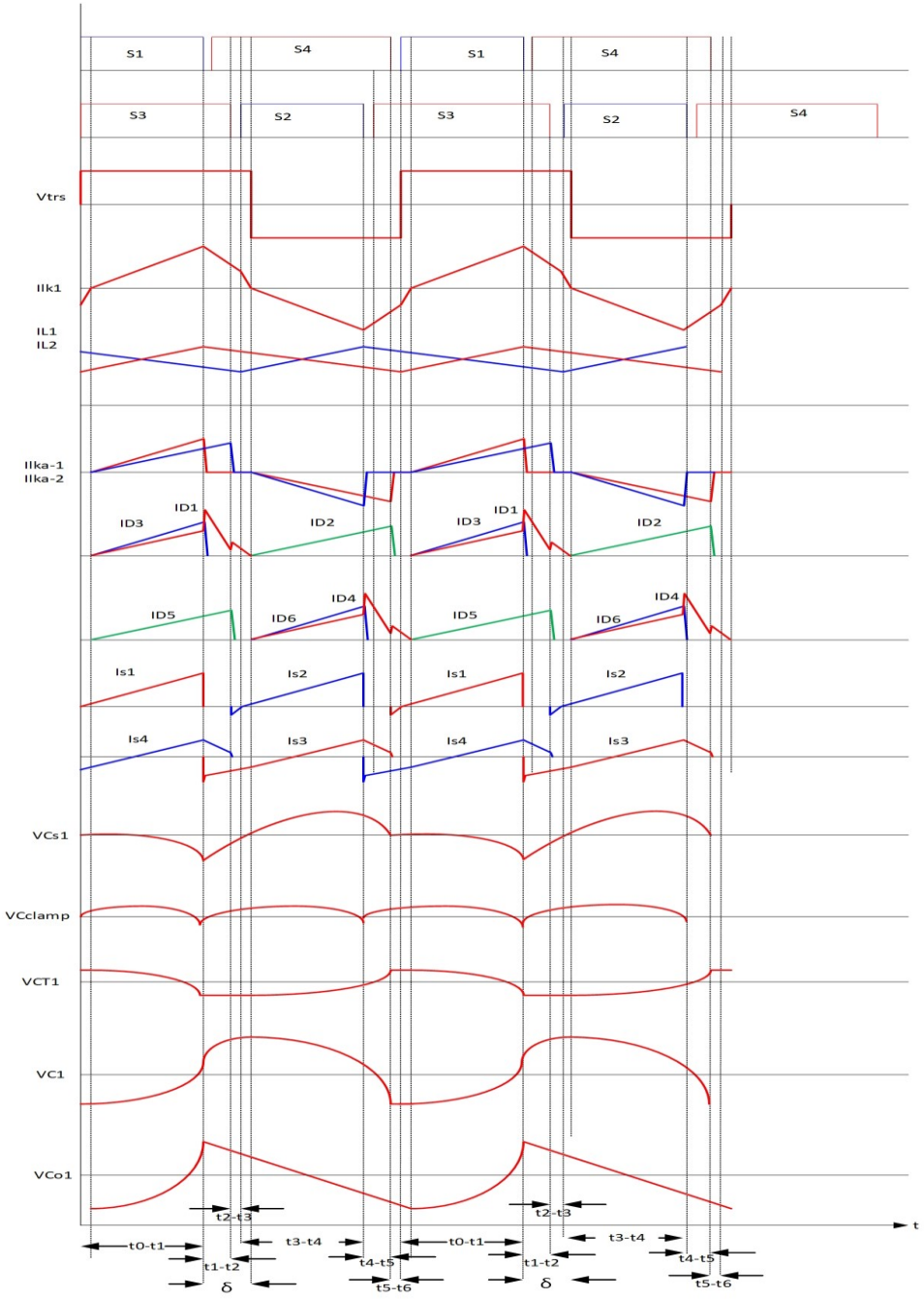


Fig. 2.5 Waveforms of the converter over a complete cycle [33].

2.2 Voltage Gain and Design Equations

From the previous set of equations, as mentioned in [33], the voltages of the capacitors and the currents of the inductors can be decided for the converter. In these following equations, the turn's ratio of the main transformer and the auxiliary transformers is considered to be 1:1 and the leakage inductances lk-a1 and lk-a2 are considered to be very small and much smaller than the magnetizing inductances of their transformers and therefore their voltage drop is neglected for the purposes of the design equations for the capacitors and also are considered equal to each other. From the Volt-Sec balance on L1 and L2 we find:

$$V_{Cs1} = V_{Cs2} = V_{in} \tag{2.47}$$

$$V_{Clamp} = V_{in}\frac{D}{1-D} \tag{2.48}$$

Similarly, from the Volt-Sec balance on Lk1 we find:

$$V_{C1} = 2V_{in}\frac{(D-2\delta)}{1-D} = V_{C2} \tag{2.49}$$

Where δ is the period where the leakage current of the main transformer reaches zero. Since the voltage drop on the leakage of auxiliary transformers is negligible:

$$V_{CT1} = V_{CT2} = V_{C1} + V_{C2} + V_{Clamp} = \frac{V_{in}}{1-D}(4(D-2\delta)+D) \tag{2.50}$$

And the output capacitors voltage is equal to:

$$V_{Co1} = V_{Co2} = V_{CT1} + V_{C1} + V_{Cs} = \frac{V_{in}}{1-D}(6(D-2\delta)+1) \tag{2.51}$$

And the output voltage of the Converter is calculated as:

$$V_o = V_{Co1} + V_{Co2} = \frac{V_{in}}{1-D}(12(D-2\delta)+2) \tag{2.52}$$

And from the conservation of energy principle:

$$\frac{V_o}{V_{in}} = \frac{I_{in}}{I_o} = \frac{1}{1-D}(12(D-2\delta)+2) \tag{2.53}$$

And since each input inductor shares half the current, the average current on each inductor is:

$$I_{L1} = I_{L2} = \frac{V_o}{R(1-D)}(6(D-2\delta)+1) \tag{2.54}$$

And from the average current on D1:

$$\frac{1}{T}\left\{\int_{\delta}^{D} I_{lk1}.dt + \int_{D}^{0.5} I_{lk1}.dt + \int_{0.5}^{0.5+\delta} I_{lk1}.dt\right\} = 3\frac{V_o}{R} \tag{2.55}$$

Solving this integration with respect to δ would lead to a long series of terms to be arranged and would finally lead to an equation defining δ as:

$$\delta^2 - \delta(D+12Q) + \left(D.(6Q-\frac{1}{4}) + \frac{D^2+2Q}{2}\right) = 0 \tag{2.56}$$

From which δ can be found and Q is defined as:

$$Q = \frac{6L_{k1}.f_{sw}}{R} \tag{2.57}$$

After finding δ, the peak current of the leakage current can be found as follows:

$$I_{lk1\_peak} = \frac{V_{in}}{1-D}(1-2(D-2\delta))\frac{D-\delta}{L_{k1}f_{sw}} \tag{2.58}$$

And the capacitor values based on the desired ripple percentage should be:

$$C_{T1,2} \geq \frac{1}{\frac{\Delta V_{CT}}{V_{CT}}.R.f_{sw}}.\frac{12(D-2\delta)+2}{4(D-2\delta)+D} \tag{2.59}$$

$$C_{o\ 1,2} \geq \frac{2(1-D+\delta)}{\frac{\Delta V_{Co}}{V_{Co}}.R.f_{sw}} \tag{2.60}$$

$$C_{\ 1,2} \geq \frac{6(D-2\delta)+1}{\frac{\Delta V_{C}}{V_{C}}.R.f_{sw}.(D-2\delta)} \tag{2.61}$$

$$C_{s\ 1,2} > \frac{24(D-2\delta)+4}{\frac{\Delta V_{Cs}}{V_{Cs}}.R.f_{sw}.(1-D)} \tag{2.62}$$

For the design of the transformer, the area product method was used. To select a core size for the transformer, the following equation was used:

$$Ap = Ae.Aw = \frac{\frac{V_{in}}{1-D}.(0.5+\delta).I_{lk1\_rms}}{B_{max}.J.K.f_{sw}} \tag{2.63}$$

Where B_{max} the maximum desired flux density in the core and J is the desired current density in the wires. From the Area product that is calculated here a proper core can be chosen if it has a higher area product that is calculated from the datasheet. After that the number of turns can be calculated by:

$$N1 = N2 = \frac{\frac{V_{in}}{1-D}.(0.5+\delta)}{2B_{max}.A_e.f_{sw}} \tag{2.64}$$

The same approach was used for the auxiliary transformers where the area product for the core selection is:

$$AP_a = Ae.Aw = \frac{V_{in}.D.I_{lka\_rms}}{B_{max}.J.K.f_{sw}} \tag{2.65}$$

And the number of turns can be found as:

$$Na1 = Na2 = \frac{V_{in}.D}{2B_{max}.A_e.f_{sw}} \tag{2.66}$$

For the leakage inductor design, a gapped core with well-known effective permeability is chosen. Then the number of turns is calculated as:

$$n = \sqrt{\frac{L.l_e}{\mu_e.A_e}} \tag{2.67}$$

The next figure (Fig. 2.6) shows the voltage gain compared to other referenced works and it shows that the voltage gain is much higher. It should also be noted that the considered voltage gain for the proposed converter is the practical voltage gain that takes into consideration the drop effect off the leakage inductance while other converters' voltage gain is the ideal one. The derivation of the previous design equations and a more detailed design procedure is explained in chapter 4 for the transformers and inductors

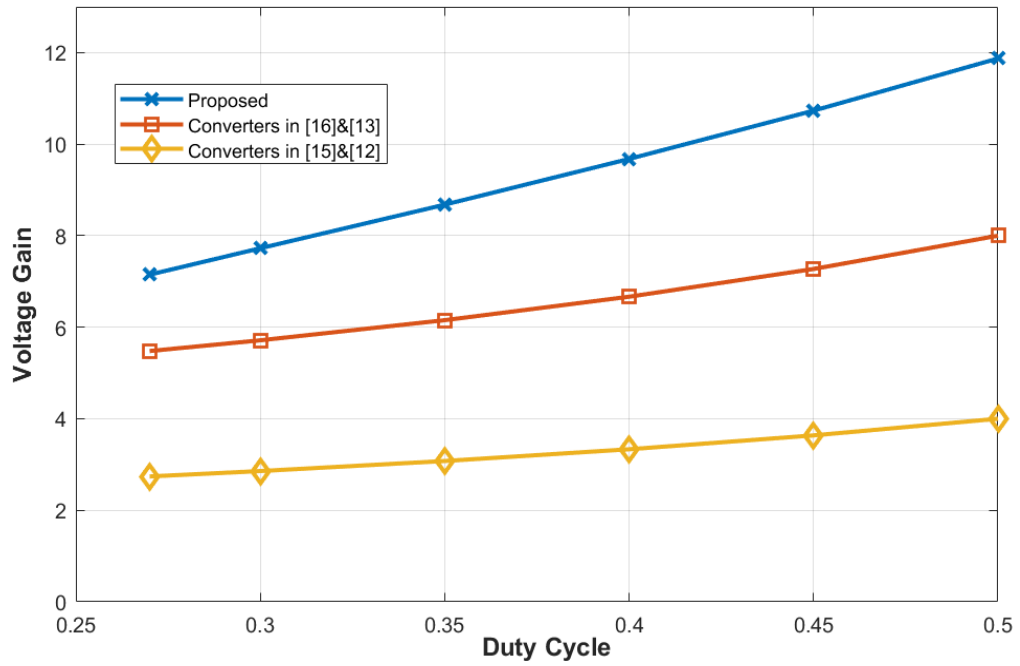


Fig. 2.6 Voltage Gain comparison for the proposed converter against other converters [33].

And the normalized switch to voltage ratio for the proposed converter compared to others is:

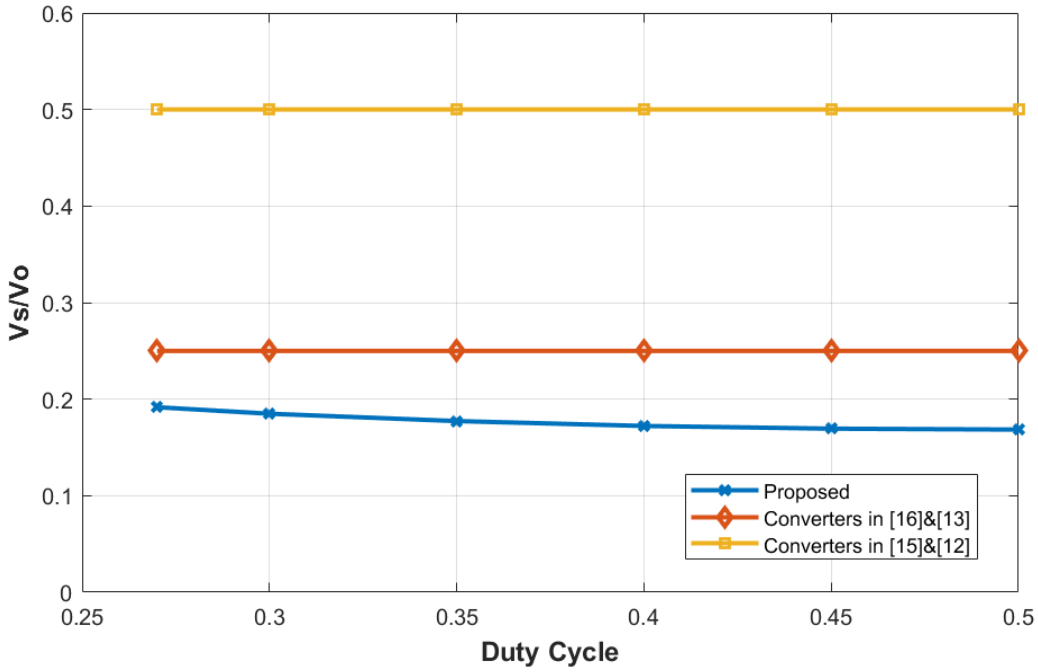


Fig. 2.7 Normalized switch voltage comparison for the proposed converter against others [33].

It can be seen that the normalized switch voltage ratio is much smaller than compared topologies which allow for the utilization of lower-rated switches. In order to verify the design equations and the presented analysis, a PSIM simulation is implemented with an input voltage of 36 V and output voltage of 380 V. Other parameters will be later discussed in chapter 3. The operating duty cycle in this case would be around 0.43. Converter is supplying a load of 450 Ω. The first waveform will be the input current waveform as seen in Fig. 2.8.

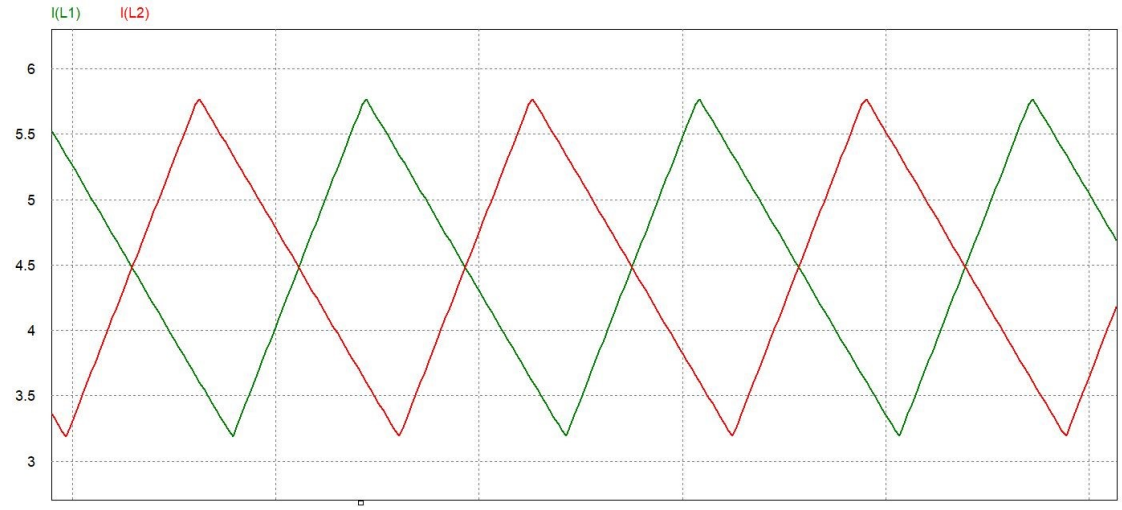


Fig. 2.8 Input currents of the converter

Fig. 2.9 shows the leakage current of the main transformer which is consistent with the analysis.

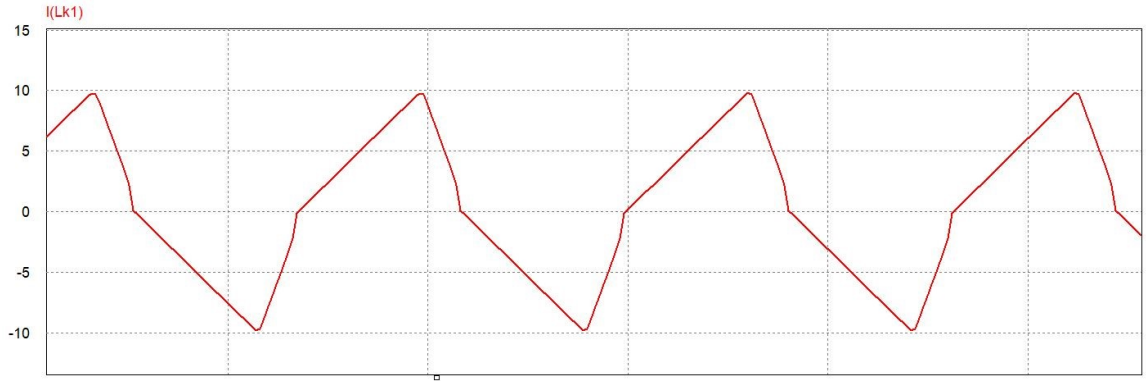


Fig 2.9 Leakage current of the main transformer

The next simulated waveforms show the voltages of D1, D2, and D3:

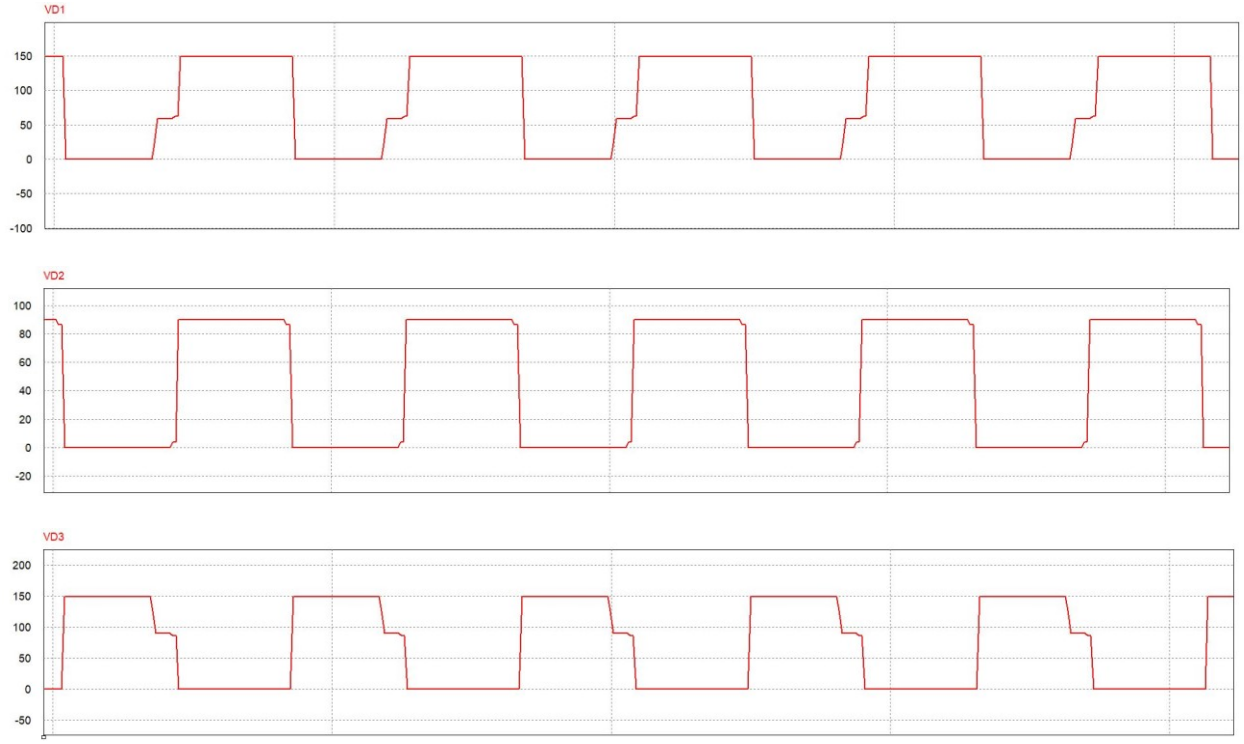


Fig 2.10 Voltages of Diodes 1, 2, and 3.

It can be seen that the waveforms from the simulation are consistent with analysis and the values are consistent with the design equations.

CHAPTER 3

MODELING THE SYSTEM AND CONTROLLER DESIGN

In this section, the average model of the converter is discussed. The averaging is performed using state-space representation and averaging. However, straight forward state-space averaging cannot be performed directly to this kind of converters. Because the state-space averaging technique usually depends on some approximations, such as the small ripple approximation, these approximations do not apply here [27]. The current in the secondary of the transformer is a pure ripple and AC. Also, the current in the primary has a large amount of ripple added to the magnetizing current. Therefore, an averaging process is required prior to the state space averaging technique. A generalized modeling technique has been proposed in [28]. The technique does not account that the average value of secondary currents is zero. The work done in [29] simply ignores the leakage inductance and it is clear from their results that there is a steady state error the value of voltage. The work in [30] confirms that the ripple of leakage inductances cannot be ignored and shows a way to average currents in inductors operating in DCM. The purpose of that is to define the average charge that is transferred from one capacitor to another and not have to use the inductor current as a state variable because its average value is zero. The current waveform and its equivalent average value are shown in figure 3.1. By doing that, as stated in [32], we avoid making I_{Lk} and I_{Lka} state variables and reduce the order of the system.

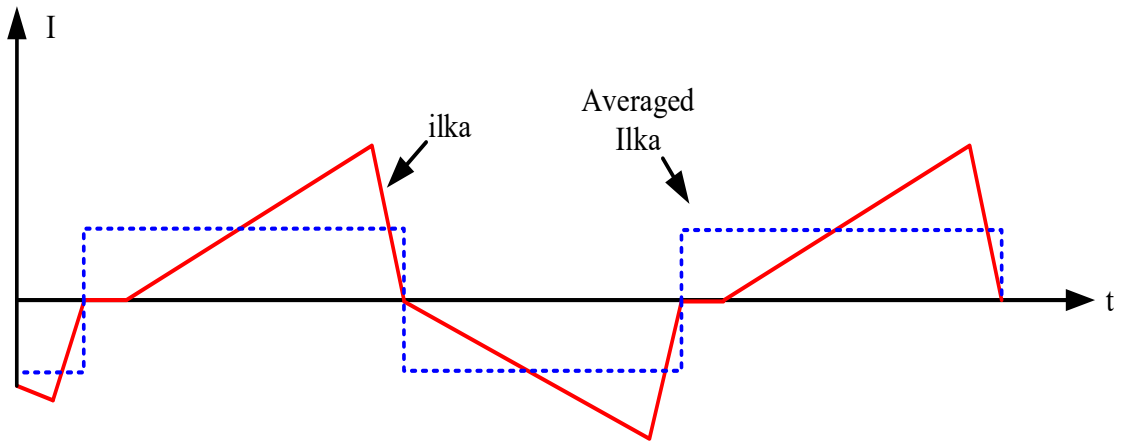


Fig 3.1 Averaged charge ripple effect [32].

Because of symmetry, the two legs of the converter have the exact same behavior except one leg is 180 degrees behind. Therefore, modeling of only one leg is needed. The symmetry of the converter also help reduce the sensory circuits and control signal circuits as the other leg is exactly the same but 180 degrees behind.

The state variables of the system, as seen in [32], can be defined as:

$$\dot{x} = \begin{bmatrix} \frac{di_{Lin}}{dt} \\ \frac{di_{Lm}}{dt} \\ \frac{dv_{Cs}}{dt} \\ \frac{dv_{Cclamp}}{dt} \\ \frac{dv_{CT}}{dt} \\ \frac{dv_{Cb}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix} \tag{3.1}$$

The average value of the current in the positive half cycle can be found to be:

$$I_{Lk+} = \frac{I_{Lk-peak+}}{2} \tag{3.2}$$

$$I_{Lka+} = \frac{I_{Lka-peak+}}{2} \tag{3.3}$$

And the average value of the current in the negative half cycle can be found to be:

$$I_{Lk-} = \frac{I_{Lk-peak-}}{2} \tag{3.4}$$

$$I_{Lka-} = \frac{I_{Lka-peak-}}{2} \tag{3.5}$$

And $I_{Lka-peak+}$can be found in (3.3) or can be defined by other state variables such as

$$I_{Lka-peak+} = \begin{bmatrix} 0 & 0 & \frac{(D-\delta)*k}{2(L_k+L_{ka})*f} & 0 & -\frac{(D-\delta)}{2(L_k+L_{ka})*f} & \frac{(D-\delta)}{2(L_k+L_{ka})*f} & 0 \end{bmatrix} \tag{3.6}$$

Which is the same current as ($I_{Lk-peak+}$). The negative peak currents can also be found from switching states 3 and 4 and are:

$$I_{Lk-peak-} = \begin{bmatrix} 0 & 0 & \frac{(1-D-d1)}{2(L_k)*f} & \frac{(1-D-d1)*k}{2(L_k)*f} & 0 & -\frac{(1-D-d1)}{2(L_k)*f} & 0 \end{bmatrix} \quad (3.7)$$

$$I_{Lka-peak-} = \begin{bmatrix} 0 & 0 & 0 & \frac{(1-D-d1)}{2(L_{ka})*f} & \frac{(1-D-d1)}{2(L_{ka})*f} & \frac{(1-D-d1)}{2(L_{ka})*f} & -\frac{(1-D-d1)}{2(L_{ka})*f} \end{bmatrix} \quad (3.8)$$

And the magnetizing current can be defined as the following vector:

$$I_{Lm} = [0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0] \quad (3.9)$$

And the input current is defined as the following vector:

$$I_{Lin} = [1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0] \quad (3.10)$$

After finding the average values of the currents, the state space representation can now be found for each switching period and the averaged model can be found. The passive parameters vector [a] is first defined as:

$$a = \begin{bmatrix} L_{in} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_m & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_s & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{clamp} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_T & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_b & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & C_o \end{bmatrix} \quad (3.11)$$

The state-space equations for the first switching period are:

$$a * \dot{x_1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & k & 0 & 0 & 0 & 0 \\ I_{Lm} - I_{Lka-peak+} & & & & & & \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ I_{Lka-peak+} & & & & & & \\ -I_{Lka-peak+} & & & & & & \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{R} \end{bmatrix} * x_1 + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * u \quad (3.12)$$

And the state-space equations for the second switching period are:

$$a * \dot{x_2} = \begin{bmatrix} 0 & 0 & -1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -k & 0 & 0 & 0 \\ I_{Lin} + I_{Lka-peak+} \\ I_{Lin} + I_{Lm} + 2 * I_{Lka-peak+} \\ I_{Lka-peak+} \\ -I_{Lka-peak+} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{R} \end{bmatrix} * x_2 + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * u \tag{3.13}$$

And the state-space equations for the second switching period are:

$$a * \dot{x_3} = \begin{bmatrix} 0 & 0 & -1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -k & 0 & 0 & 0 \\ I_{Lin} + I_{Lk-peak-} \\ I_{Lin} + I_{Lm} + I_{Lk-peak-} + I_{Lka-peak-} \\ I_{Lka-peak-} \\ -I_{Lka-peak-} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{R} \end{bmatrix} * x_3 + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * u \tag{3.14}$$

And the state-space equations for the second switching period are:

$$a * \dot{x_4} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & k & 0 & 0 & 0 & 0 \\ I_{Lm} + I_{Lka-peak-} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -I_{Lka-peak-} \\ I_{Lk-peak-} - I_{Lka-peak-} \\ I_{Lka-peak-} - \frac{1}{R} \end{bmatrix} * x_4 + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * u \tag{3.15}$$

And the state-space equations for the first switching period are:

$$a * \dot{x_5} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & k & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ I_{Lk-peak-} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{R} \end{bmatrix} * x_5 + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * u \tag{3.16}$$

After finding the state space equations of each switching period, the average state-space equations can now be found:

$$A = A_1(D - \delta) + A_2(d1) + A_3(1 - D - d1) + A_4(\delta - d2) + A_5(\delta) \tag{3.17}$$

And the steady-state values of the variables can be found by taking the derivative equal to zero which would yield to:

$$X = -(a^{-1}.A)^{-1}.B \tag{3.18}$$

This model can now be tested and compared in a simulation with a circuit-based converter in the next test. The presented test is to compare the average model steady-state gain with the circuit-based simulation. The comparison examines all capacitor voltages and the input current since it is considered as a state variable. The same conditions and parameters that are shown in table 1 are applied to both models. The steady-state gain of the input current is shown in figure 10 (a). The output capacitor gain of the circuit-based simulation and the average model is shown in figure 10 (b). The clamp capacitor voltage and V_{CT} are demonstrated in figure 10 (c) and (d) respectively. Figure 14 shows the output voltage of a step response for the average model and circuit-based model. From the results, it is clear that the average model matches the proposed circuit model of the DC-DC converter.

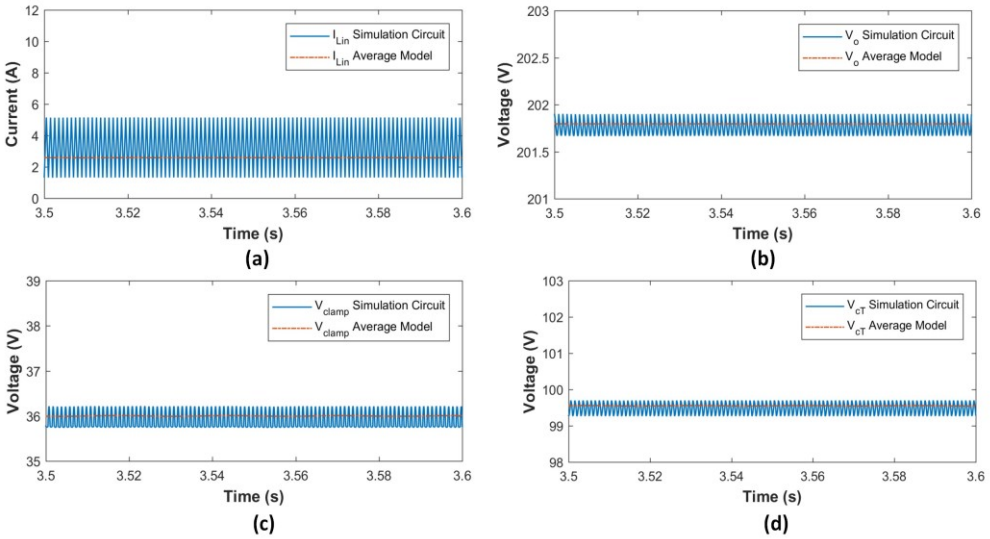


Fig. 3.2 Average model and circuit model comparison for: (a) Input inductor current. (b) Output voltage. (c) Clamp voltage. (d) V_{CT}.

Now that the model's accuracy has been verified, the Bode plot of the converter can be found. The average differential equation for the output voltage is found to be:

$$\frac{dv_o}{dt} = \alpha . v_{clamp} . k + \alpha . (v_{CT} + v_{Cb}) - \left(\alpha + \frac{1}{R.C_o}\right) . v_{Co} \tag{3.19}$$

From 143, the small signal and large signal transfer functions are found and the term α in equation ( ) is:

$$\alpha = \frac{(1-D-t_1)^2(1+\frac{t_1}{1-D-t_1})}{2L_{Ka}C_o f_{Sw}} \tag{3.20}$$

The Bode plot of the converter can be seen in Fig. (). It can be seen that the cross over frequency is 965 Hz. The phase margin is 102 degrees at the cross over frequency.

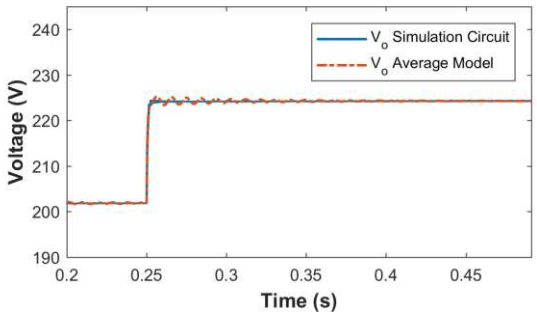


Fig. 3.3 Step response of the average model and circuit model.

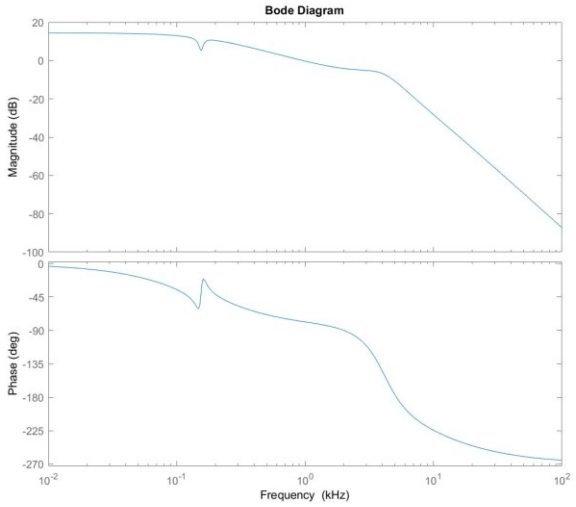


Fig. 3.4 Bode plot for the open loop model of the converter.

The regulation of the output voltage is performed using a PI feedback loop. The regulating transfer function would be:

$$G_v(s) = Kp + \frac{Ki}{s} \tag{3.21}$$

And the chosen PI parameters are:

$$Kp = 0.1 \tag{3.22}$$

$$Ki = 20 \tag{3.23}$$

The feedback control diagram would then be:

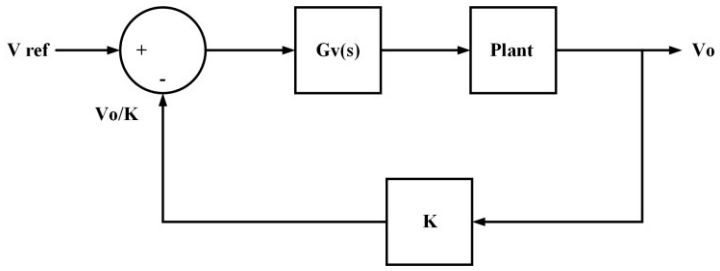


Fig. 3.5 Voltage control feedback loop.

The feedback loop is then tested in continuous time simulation using PSIM software. The first test is introducing a step in the input voltage. The response of the output voltage can be seen in Fig. (3.6):

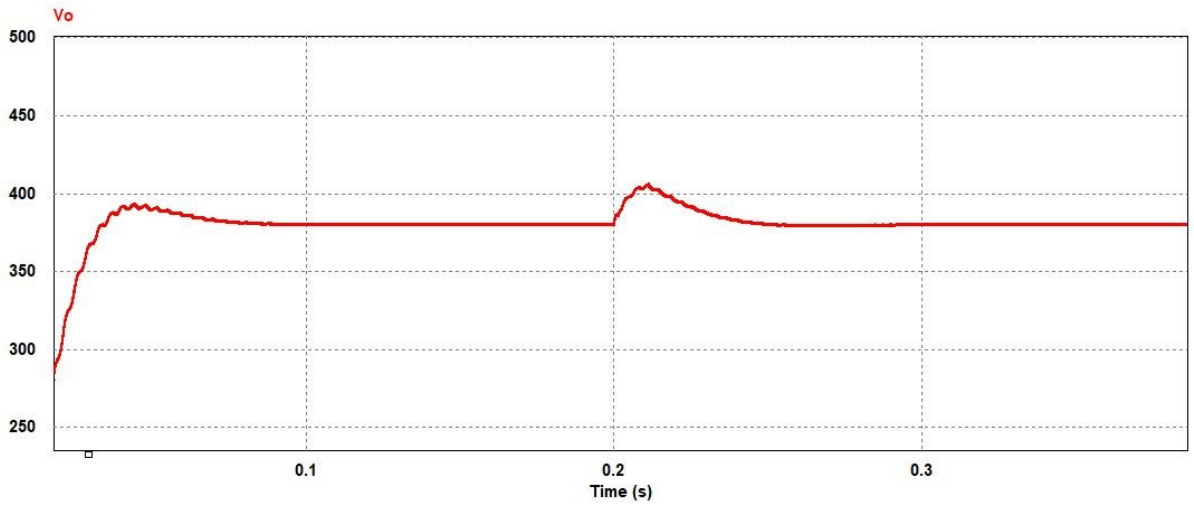


Fig. 3.6 Step response of the output voltage after increasing the input from 36 to 39 volts.

It can be seen that the voltage was regulated and stabilized at 380 volts. The duty cycle generated by the controller can also be seen in Fig. 3.7:

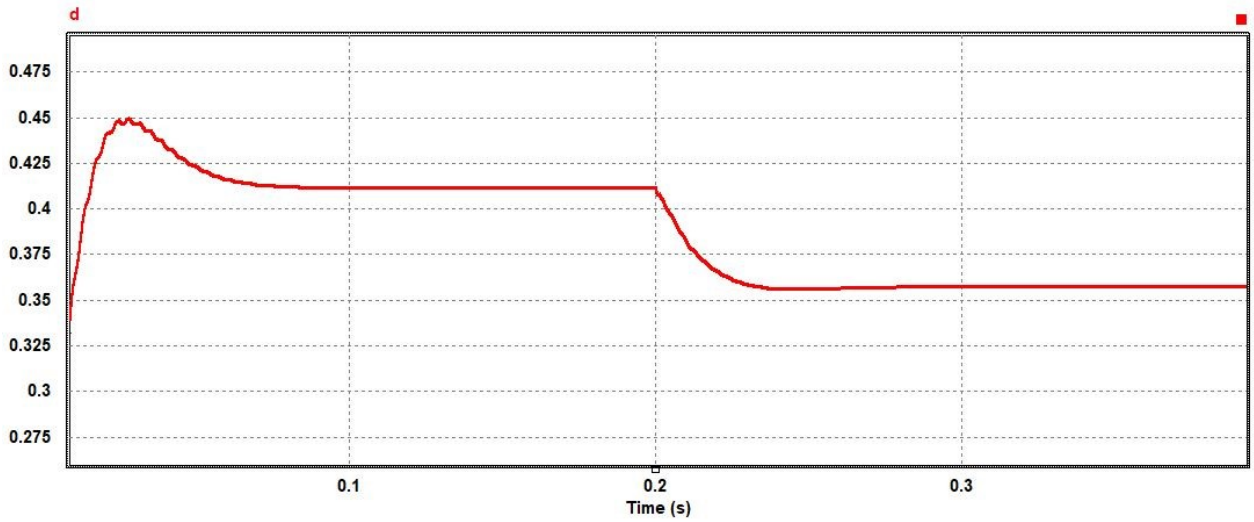


Fig 3.7 Duty cycle response after an increase in the input voltage happened.

It can be seen that the generated duty cycle has decreased from 0.413 to o.36 to stabilize the output voltage at the desired level. The next test was to introduce a step in the load. At the beginning the converter was supplying 380 volts to a 450 Ω resistor. A 1000 Ω resistor was connected in parallel to observe the response. The response of the converter under the voltage regulation loop can be seen in Fig. 3.8.

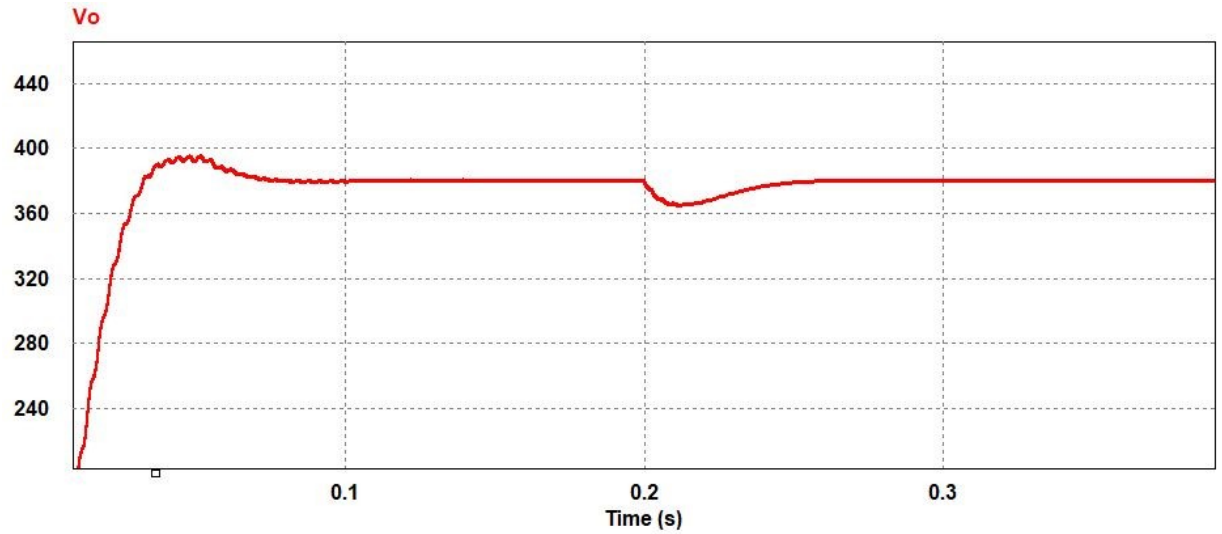


Fig 3.8 Output voltage response under a load increase.

The input currents of L1 and L2 can also be seen in Fig. 3.9:

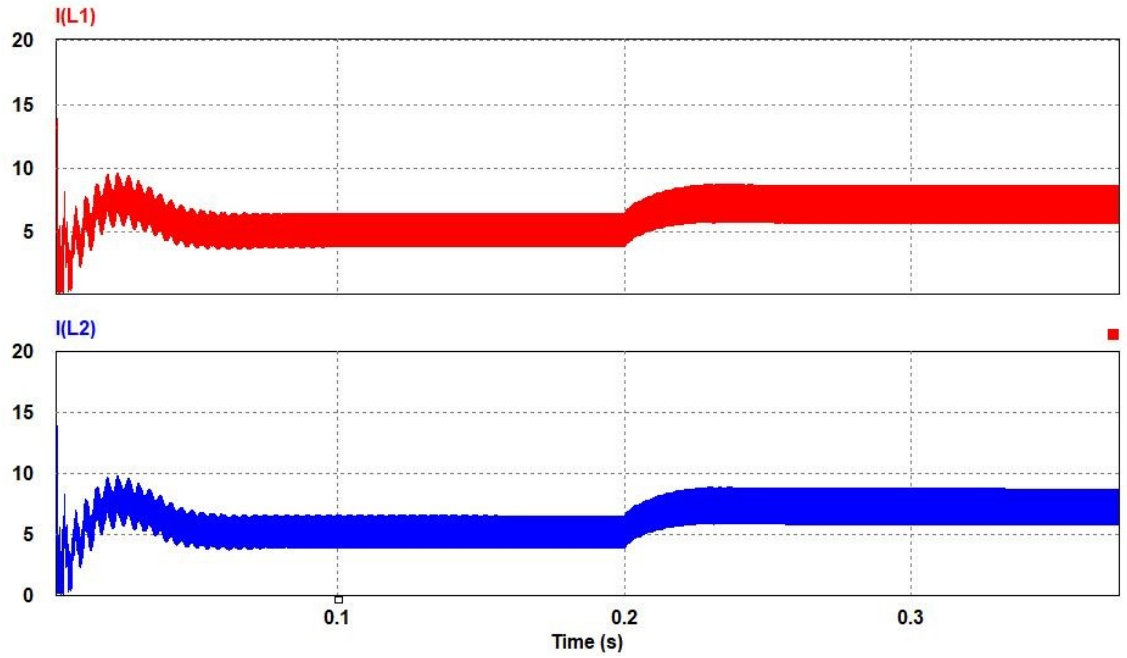


Fig 3.9 Input currents of the converter under load increase.

The currents has increased after the load has increased. After testing the feedback controller in continuous time, the controller is then discretized. Tustin transformation is then used [33]. The Tustin transformation defines an equivalent quantity for every term (S) in the continuous time domain. The equivalent term for every (S) would be:

$$S = \frac{2}{T}\frac{Z-1}{Z+1} \tag{3.24}$$

The designed compensator would then be:

$$G_v(z) = Kp + Ki\frac{T}{2}\frac{z+1}{z-1} \tag{3.25}$$

And after substituting Kp and Ki the transfer function becomes:

$$G_v(z) = 0.1 + \frac{z+1}{2500(z-1)} \tag{3.26}$$

This transfer function can then be implemented in our TI F28335 DSP for digital control of the converter.

CHAPTER 4

MAGNETICS DESIGN

It can be seen that this converter depends mainly on transformers and inductors for energy transfer. Each element has a different design process. Each element's design process will be discussed in the following subsections.

4.1 Input Inductor design

The design process of the input inductors is straight forward. The value of the inductance is specified based of the desired current ripple, the switching frequency, and the input voltage.

$$L_{in} = \frac{V_{in}.D}{\Delta i_{in}.f} \tag{4.1}$$

Usually, the current ripple is desired to be less than 10% in the input inductor to have smooth current waveform that is easy to measure and to simplify the maximum power tracking in the case of solar PV applications. However, since the proposed converter is interleaved, the ripple of each inductor can be double and it will not affect the current coming from the source. Because of interleaving, the current ripple can be double of that for a single inductor converter which is in this case around 20%. For 25 KHz switching frequency, 36 V input voltage, and 0.4 duty cycle, required inductance is calculated to be 320 uH. After finding the desired electrical parameters. The magnetic and geometric parameters need to be found. First, the characteristics of magnetic materials and the B-H curve is discussed. After that, the difference between the transformer and inductor design is discussed. After understanding the difference, Gap calculation and window area are established to facilitate the understanding of the area product approach which is presented next. After that a general design procedure is established and used to design a coupled inductor with 1:1 ratio. Finally, conclusion and references are presented. Faraday's law of induction states that the induced voltage in a coil is a function of the change in magnetic flux times the number of turns.

$$E = n.\frac{d\phi}{dt} \tag{4.2}$$

And the flux is a function of the flux density time the cross sectional area.

$$\phi = A_e . B \tag{4.3}$$

Therefore there is a relationship between the flux density and the imposed voltage which is:

$$E = n . A_e . \frac{dB}{dt} \tag{4.4}$$

And since the voltage in a coil is equal to the inductance times the change of current we find the

$$L \frac{di}{dt} = n \frac{d\phi}{dt} \tag{4.5}$$

$$L \int_0^{Ipk} \left(\frac{di}{dt}\right) dt = nAe \int_0^{Bmax} \left(\frac{dB}{dt}\right) dt \tag{4.6}$$

$$L . I_{pk} = n . Ae . B_{max} \tag{4.7}$$

We can see that (4.7) is an important equation in the design of magnetic elements. Another important law is the Ampere's law which states that the total magnetic field force is equal to the current times the number of turns divided by the magnetic path length.

$$H = \frac{n.I}{l_e} \tag{4.8}$$

In Practice, ferromagnetic materials reach a saturation limit where the flux density (B) does not increase with the increase of magnetic force (H). There is a near linear zone in which a magnetic material operates in as shown in the next figure.

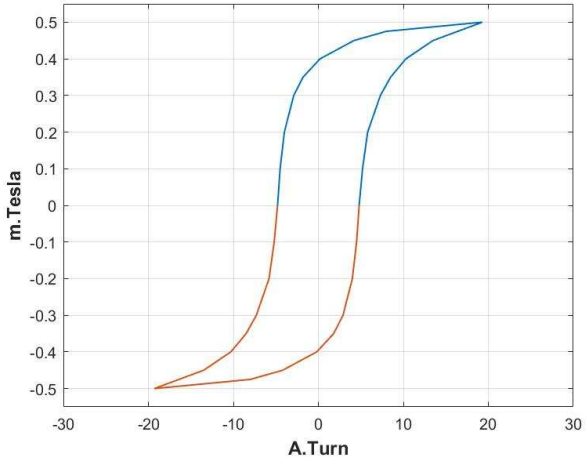


Fig. 4.1 Hysteretic B-H curve [34]

Therefore, any magnetic element should be designed to operate within the linear zone. There is a big difference between designing for a transformer and designing for an inductor. In the case of a transformer. The total amount of power is transferred from one side to the other.

$$n_1.I_1 = n_2.I_2 \tag{4.9}$$

Therefore all the energy passing through the magnetic core passes through to the other winding (in an ideal case). In the case of an inductor, there is only one winding on the core. The energy is stored in the core. For a high permeability material, the core will reach saturation very quickly when storing the energy inside it. Therefore an air gap is introduced to slow the rate of change of the magnetic flux. In most cases, inductors require gaps and transformers don't.

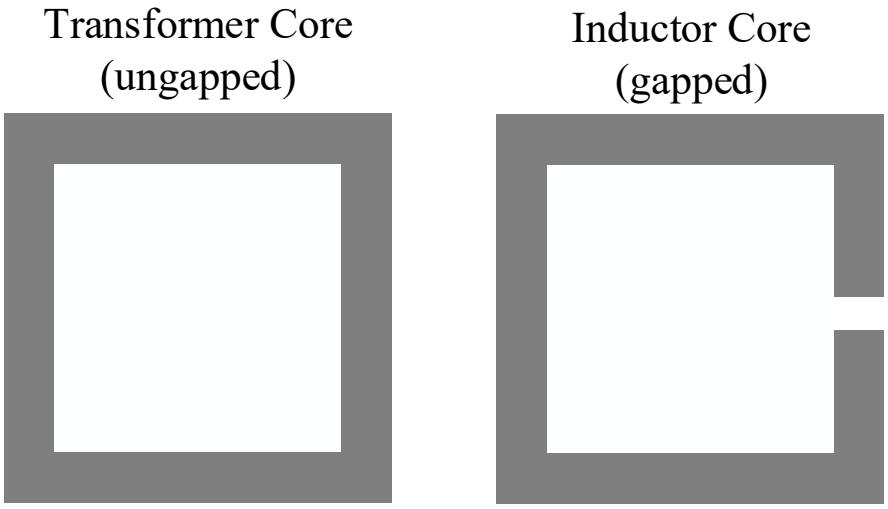


Fig. 4.2 Transformer core vs Inductor core.

And from (4.7) we find that

$$L\frac{di}{dt} = \frac{n^2 A_e \mu}{l_e}\frac{di}{dt} \tag{4.10}$$

$$L = \frac{n^2 A_e \mu}{l_e} \tag{4.11}$$

In the beginning, there are a few simplifying assumptions to make. First it is assumed that the length of the gap is much smaller than the length of the magnetic path

$$l_g \ll l_e \tag{4.12}$$

$$l_g + l_e \cong l_e \tag{4.13}$$

In addition, we also assume that the flux is almost the same and B does not change much. In that case:

$$H = \frac{B}{\mu_e} = \frac{B_m}{\mu_m} + \frac{B_a}{\mu_o\left(\frac{le}{lg}\right)} \tag{4.14}$$

$$\frac{1}{\mu_e} = \frac{1}{\mu_m} + \frac{1}{\mu_o\left(\frac{le}{lg}\right)} \tag{4.15}$$

And dividing by μ_o yield to:

$$\frac{1}{\mu_{re}} = \frac{1}{\mu_{rm}} + \frac{1}{\left(\frac{le}{lg}\right)} \tag{4.16}$$

And rearranging:

$$\mu_{re} = \frac{\mu_{rm}.\left(\frac{le}{lg}\right)}{\mu_{rm}+\left(\frac{le}{lg}\right)} \tag{4.17}$$

And if the ration of the lengths is much smaller than the relative permeability:

$$\left(\frac{le}{lg}\right) \cong \mu_{re} \tag{4.18}$$

Which means that the gap length can be easily estimated if the magnetic length is much bigger but at the same time the ratio is much smaller than the relative effective permeability which is valid for most ferromagnetic with high permeability and the length of the gap is:

$$lg \cong \left(\frac{le}{\mu_{re}}\right) \tag{4.19}$$

And in practice, an iterative approach is used to find the right gap that does not reduce the desired inductance value. The window area of the winding is a key design factor in magnetic elements. It is the area inside the core to be filled with winding wires. This area needs to be fully exploited as much as can be to minimize leakage flux. Ideally, this area is the sum of all the wire areas. However, since there will be gaps between wires, a filling factor k is included to estimate the ratio of the unfilled area. Therefore the expression for calculating the Window area is:

$$A_w = \frac{[W_{A1}.n_1 + W_{A2}.n_2]}{k} \tag{4.20}$$

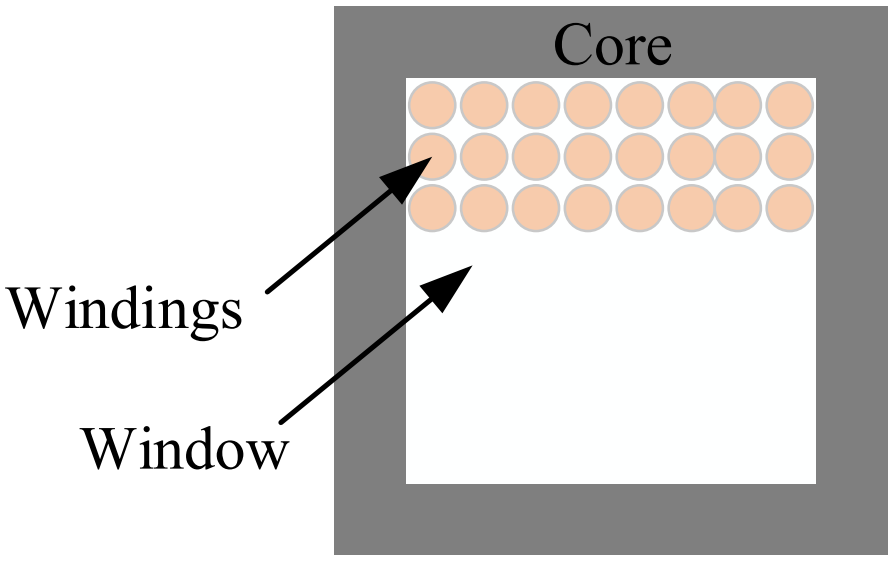


Fig. 4.3 Window Area.

Where W is the wire area which is:

$$W_{A1} = \frac{I_{rms}}{J} \tag{4.21}$$

Where j is the desired current density in the wire and n is the number of turns. The previous formula is for a two winding magnetic element. The window area for a certain inductor can also be expressed as:

$$A_w = \frac{I_{rms}.n}{J.k} \tag{4.22}$$

The area product approach gives a relationship between the physical size of the core and the electrical/magnetic parameters of desired inductor. It is basically the product of the cross sectional area and the window area which are two physical geometrical values that can also be expressed by electrical values. From the following basic equation:

$$L\frac{di}{dt} = n\frac{d\phi}{dt} \tag{4.23}$$

$$L\int_0^{Ipk}\left(\frac{di}{dt}\right)dt = nAe\int_0^{Bmax}\left(\frac{dB}{dt}\right)dt \tag{4.24}$$

We find that:

$$L.I_{pk} = n.Ae.B_{max} \tag{4.25}$$

Therefore the cross sectional area of the core will be:

$$Ae = \frac{L.I_{pk}}{n.B_{max}} \tag{4.26}$$

And since we just found that:

$$A_w = \frac{I_{rms}.n}{J.k} \tag{4.27}$$

The area product is:

$$A_p = A_e.A_w = \frac{L.I_{pk}.I_{rms}}{B_{max}.J.K} \tag{4.28}$$

Therefore by knowing the information on the right hand side, a core can be selected from a manufacturer's datasheet that satisfies the desired number by finding the product on the left hand side. An iteration between the cross sectional area, the window area and the number of windings could be performed to satisfy the equation.

It can be seen that B_{max} is an important factor in the operation of a magnetic element. In addition to the limitation of the saturation zone, the flux density is also limited by the frequency due to magnetic losses

$$P_{Loss} = F(f_{sw}, \Delta B) \tag{4.29}$$

And the power is dissipated through the volume of the core. Therefore, the magnetic loss unit is mW/cm^3 or kW/m^3. When selecting a core. The selected ΔB along with the switching frequency must present reasonable and accepted losses.

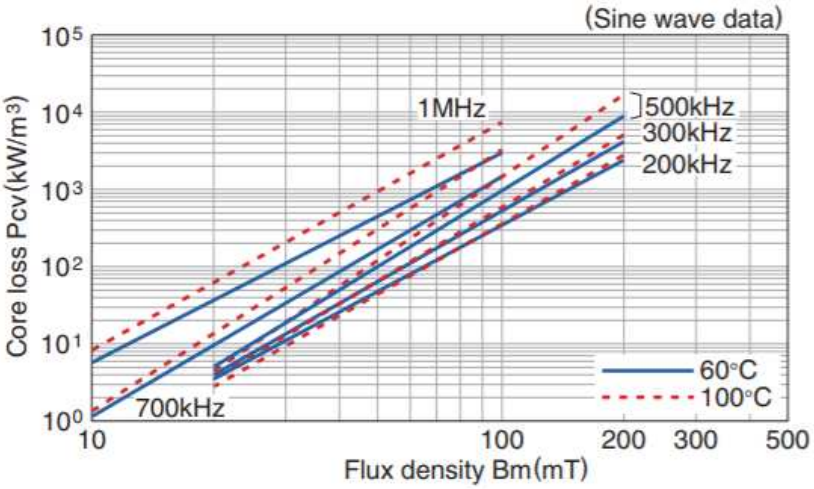


Fig 4.4 Core loss vs ΔB and frequency. Diagram from [35]

The same information can be given in the form of tables instead of graphs in some manufacturers' datasheet. One of the common core types is the toroidal core. It is very popular because it has the minimum amount of leakage flux.

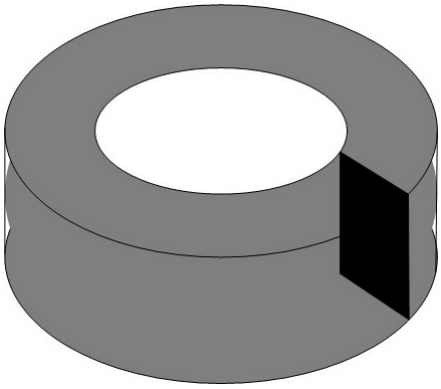


Fig. 4.5 Toroidal Core Type [36]

The material used with toroidal cores is usually powdered to form a distributed gap. This type of cores has many benefits including:

- Stability with time and temperature
- Low core losses
- Stability of inductance over a large change in flux.
- Low leakage

Another type is the EE/EI/EP core. The used material is usually ferrite.

Fig. 4.6 EE/EI Core Types [37]

These types of shapes usually utilize more volume to space ratio and could go to high frequencies up to a few megahertz. The gap is physically placed in the core and calculated in the design. The window area is more utilized in the shape.

From the past information, a generalized procedure for designing a magnetic element can be developed.

1. Transformer Design Procedure
    A. Calculate Ap
    B. Choose a core based on ΔB and switching frequency
    C. Calculate n1
    D. Calculate n2 based on voltage value.
2. Gapped inductor Design Procedure
    A. Calculate Ap
    B. Choose a core based on ΔB and switching frequency
    C. Iterate for Ae and Aw to find the right value
    D. Calculate gap length

A core from FERROXCUBE is selected based on Choose a core based on ΔB and acceptable losses for the desired switching frequency for calculations that has the following geometrical specs:

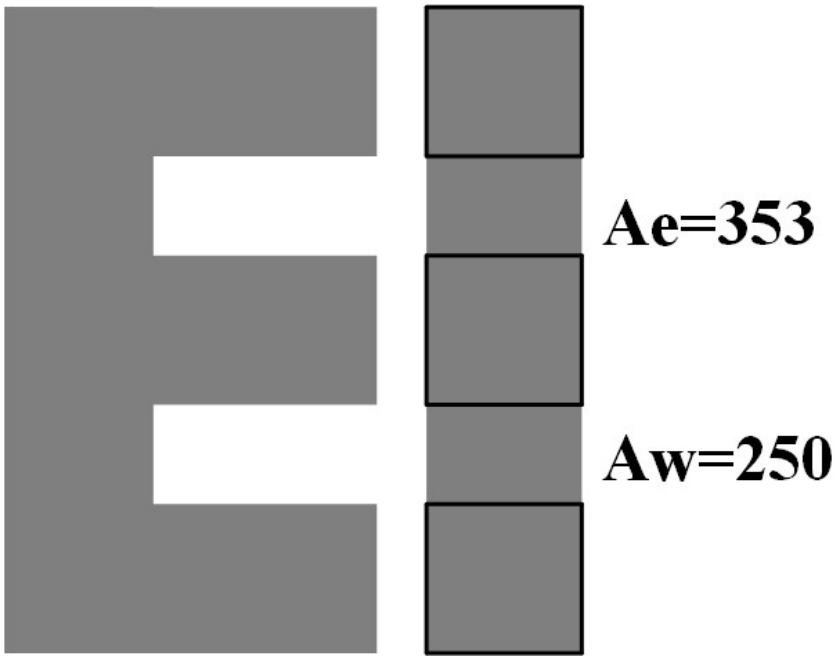


Fig. 4.7 E55/28/21 Core [38]

Table 4.1: Power loss at given frequency and flux density [38].

Power Loss				
Measuring Conditions			Max	Unit
100KHz	200mT	100 C	21	W/set
100KHz	200mT	25 C	23	W/set

Table 4.2: Saturation flux density for different core materials at 100 degrees [38].

B Sat.					
Measuring Conditions			Material	Min	Unit
25KHz	250A/m	100 C	3C91	320	mT
25KHz	250A/m	100 C	3C92	370	mT
25KHz	250A/m	100 C	3C94	320	mT

The following parameters are gathered from the electrical circuit:

Table 4.3: Transformer design parameters

V_{in}	$36v$
V_o	$400v$
f_s	$25Khz$
N	1
I_m	8.5
I_{pk}	12
I_{rms}	11
B_{max}	0.25

From these, the needed Area product is:

$$A_p = Ae.Aw = \frac{\frac{V_{in}}{1-D}.(0.5+\delta).I_{lk1\_rms}}{B_{max}.J.K.f_{sw}} = 43022mm^4$$

From EE55/28/21 core datasheet:

$$A_p = A_e.A_w = 353 \times 250 = 88250\ which\ is > 43022$$

$$n = \frac{L.I_{pk}}{Ae.B_{max}} = 14\ turns$$

$$A_{Wneeded} = \frac{n.I_{rms}}{J.K} = 122.22mm^2 \times 2(for\ primary\ and\ secondary) =$$

$$244.44mm^2\ which\ is < 250mm^2\ from\ data\ sheet$$

The same approach can also be used for the rest of the transformers.

CHAPTER 5

PROTOTYPE AND EXPERIMENTAL RESULTS

A 450 w 380 V output voltage prototype was developed in the laboratory to validate the concept of this converter.

Table 5.1: Experiment Parameters

Parameter	Value
Vin	36 V
Vout	380 V
Power	450 W
Frequency	25 KHz

The building of the prototype consists of three stages. The first stage is the passive components design and sizing. The second stage is the switch sizing and gate drive design. Each stage will be discussed and detailed in the next following sections.

5.1 Passive element design

The first step in this stage is to find the right capacitor size for the desired power and output voltage. Based on equation ( ), the value of the capacitor Cs1/Cs2 should be bigger than 120uF. In addition, the ripple in the current is highest at these capacitors. Therefore film capacitors are used for their ability to endure high current ripple. Since other capacitors are known to be smaller than Cs1/Cs2, all other capacitors are chosen to be more than 120uF. Therefore the chosen capacitors for this prototype are KEMET 70uFx2 metalized polypropylene film capacitors.

Filter inductor (or input inductor) are abundant and do not require special design procedures. The only two factors are the DC resistance and the saturation current that effect the performance of input inductors. From design Equation ( ), the needed inductors L1/L2 are required to be more than 200uH. Coilcraft shielded filter inductors are chosen that have a very low DC resistance and a saturation current of 6 A. The maximum current needed for this inductor is 4.5 A.

The transformers' design procedure that is presented in chapter four is used to design both the main and auxiliary transformers. For the main transformer, an E55/28/21 Core is chosen to satisfy the area product value needed for the main transformer. The wire used is a 26 AWG twisted pair in a bundle of three. This approach has been taken because Litz wires are fairly expensive and are not available in our lab. The transformer has 14 turns for both the primary and secondary. Using the impedance analyser, the measured leakage inductance for the main transformer is 3uH and the magnetizing inductance is around 990uH.

For the auxiliary transformers, the same procedure was used. The chosen core is E42/21/15 to satisfy the area product value needed. The same 26 AWG wire was used a twisted pair bundle of 2 since there is less current flowing through the auxiliary transformers. The measured leakage is 1uH and the magnetizing inductance was around 900uH.

The series leakage inductance was designed with an ETD 29/16/10 core and a 1 mm gap. The number of turns for this is chosen to produce around 21uH inductance which is 11 turns. The same 26 AWG wire with a twisted pair bundle of 2 is used.

5.2 Switch sizing and gate drive design

In this stage, the switch and diode sizes are discussed. After that, the gate drive circuit that is used for these switches is presented and detailed. Since the maximum duty cycle that the converter exhibits is 0.5, the maximum voltage across the switch will not exceed 72 volts in any case. Therefore a 100 V MOSFET is chosen with a very low on resistance of 3.9 mΩ. Similarly, the maximum voltage across the diodes is 150 V. Therefore, a 250 V diode can be used. Since we have available 650 V diodes in the lab, they are used in this prototype.

The gate drive circuit that is used for these switches is shown in Figure 5.1 which is mainly a full wave rectifier and a linear regulator (L7815) connected to FOD3120 opto-coupler. The opto-coupler provides isolation between the signal and the power sides. And protects the micro controller from high side voltages.

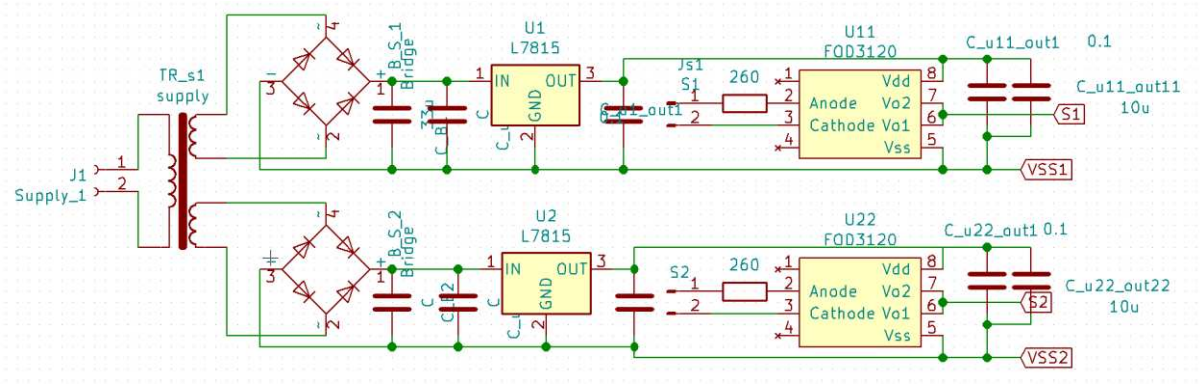


Fig. 5.1 Drive circuit for MOSFETs using FOD3120 opto-couplers.

Where L7815 is a 15V regulator and FOD3120 is a gate drive opto-coupler. The FOD3120 diagram is shown in Fig. 5.2.

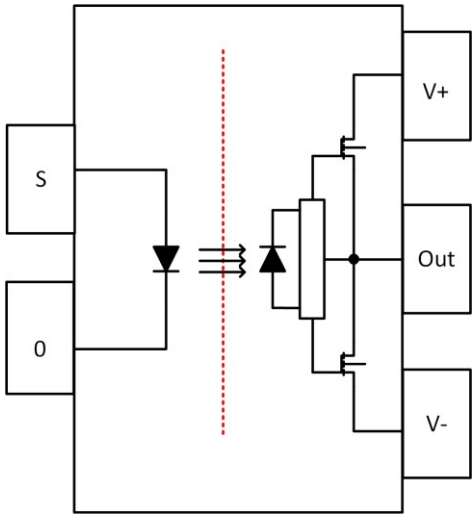


Fig. 5.2 FOD3120 opto-couplers internal functional diagram [39].

The opto-coupler pulls the 15 V supply to the gate when the anode to cathode voltage is positive. The gate voltage is zero when the anode to cathode voltage is zero or negative.

5.3 PCB design and layout

The PCB design and layout stage has also many steps. The first step is to draw the schematic of the system. The software used in this project is KiCad. After having all the required power and auxiliary circuits, the complete system can now be laid out in a schematic. The schematic for the system is shown in figures 5.3 and 5.4.

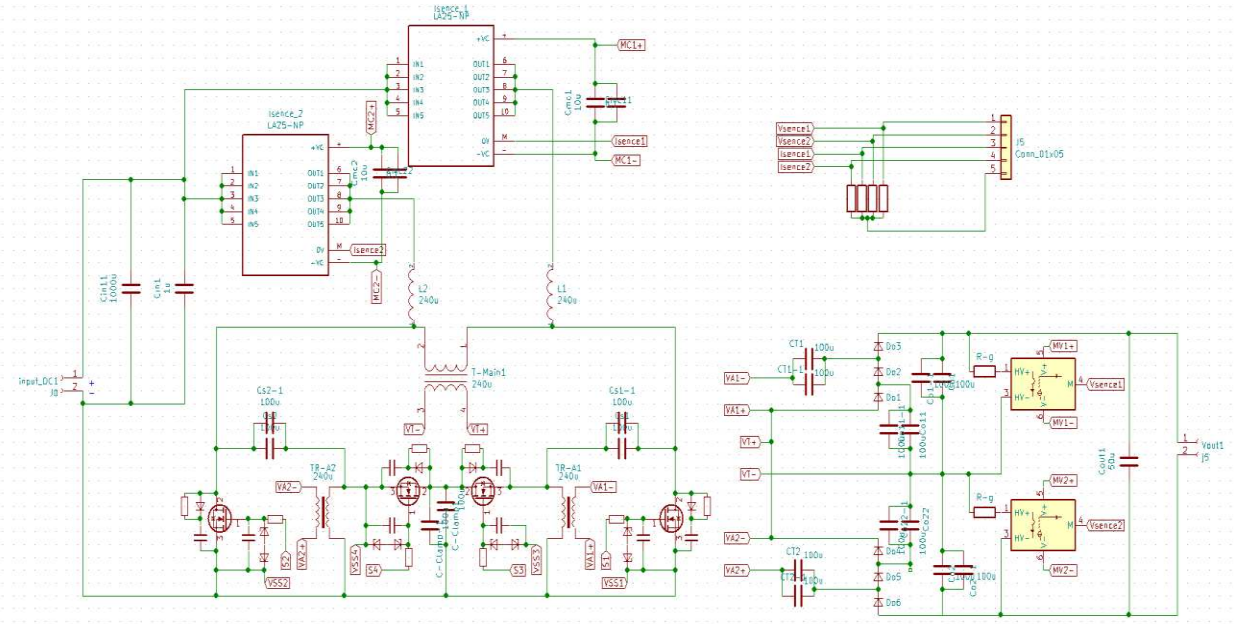


Fig. 5.3 Main schematic for the proposed system.

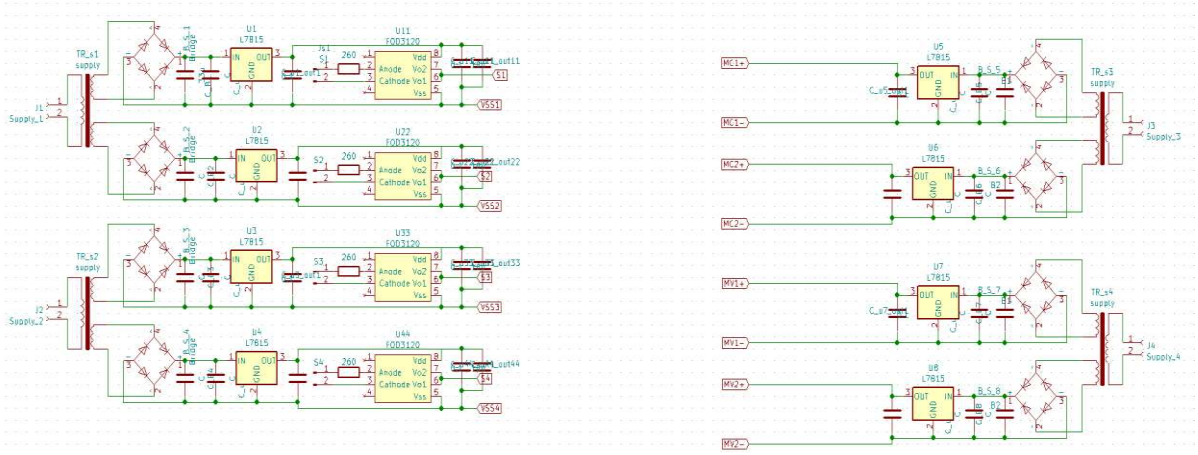


Fig. 5.4 Switch gate drive and censors power supplies schematic.

After drawing the schematic, the next step is to assign footprints for each symbol to a physical component in the PCB. After assigning all the footprints, they can be laid out in the PCB as shown in Fig. 5.5.

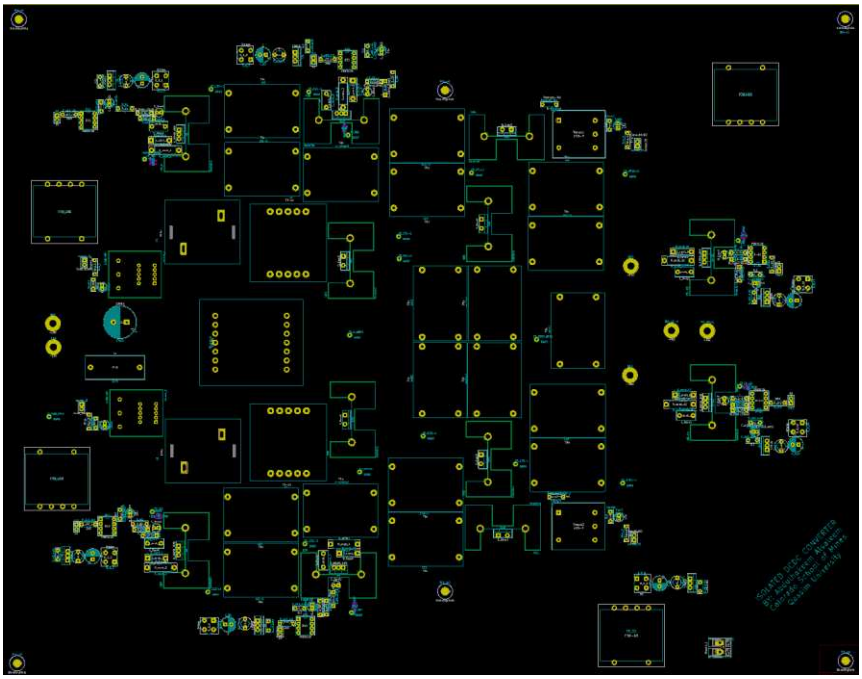


Fig. 5.5 Footprint layout of all components.

After finding the suitable layout for the components, the routing of all power and signal paths can be done for both front and back layers as seen in Fig. 5.6.

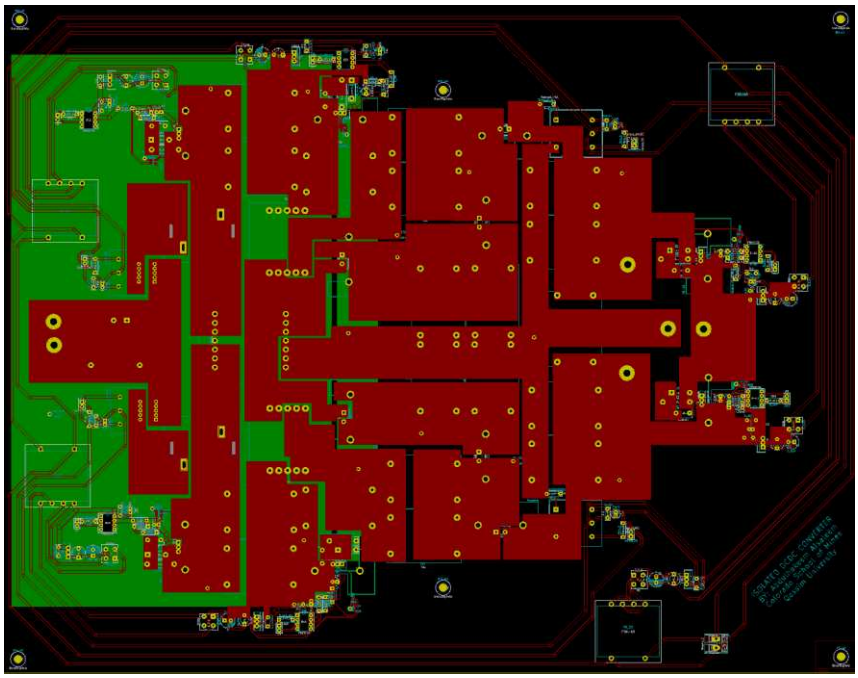


Fig. 5.6 Layout and routing of all components.

5.4 Experimental results

Several experimental results are shown in this section. Each experiment is implemented to examine certain performance parameters separately. The component parameters are detailed in the next table.

Table 5.2: Description of components

Component	Description
Input inductors	Coilcraft AGP4233-224ME. 220 uH
Main Transformers	1:1 ratio TDK E55/28/21 N87 material
Auxiliary transformers	1:1 ratio TDK E42/21/15 N87 material
Leakage Inductor	22 uH ETD core 29x16x10 N87 gapped 11 turns
Capacitors	2x 70 uF Kemet C4AQLBW5700A3LK
MOSFETs	100v 3.9mOhm Infineon IPP039N10N5
Diodes	Infineon Schottky IDH08SG60C

The first experiment was performed as a proof of concept to validate the analysis made in chapter two. Fig. 5.8 shows the designed prototype and its layout. The current of the input inductors is measured through 2 LA 25NP sensors. The switches are being driven by FOD 3182 drivers with isolated floating supplies. In addition, each switch is equipped by an RC snubber to prevent over voltages from parasitic inductances at turn offs. The RC snubber consists of an 8.2 ohm resistor and a 10nF capacitor and can be seen in Fig. 5.7. The converter is operated first at 320 W and output voltage of 380 volts. The input voltage is 37 volts and the duty cycle 0.4.

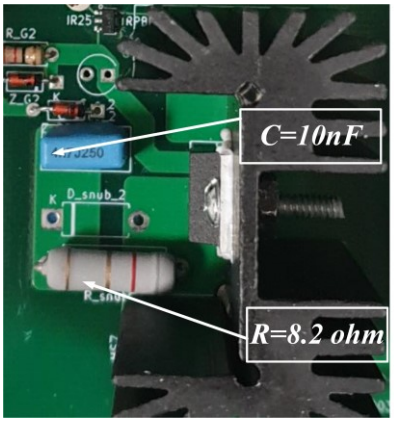


Fig. 5.7 RC snubber used in the prototype [33].

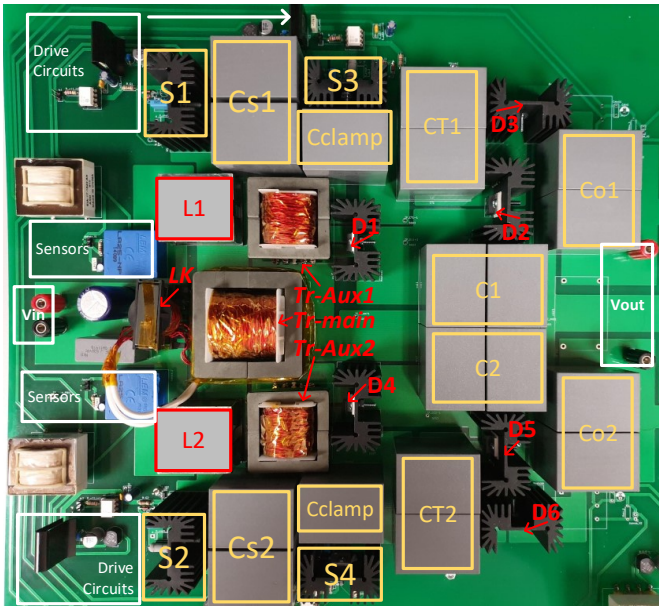


Fig. 5.8 PCB implementation of the proposed converter [33].

Fig. 5.9. a.) Shows the current waveform of the main transformer I_{LK1} which is probed by a current probe that conforms to the presented analysis in chapter two. Fig. 5.9. b.) Shows the two input inductors share the current equally and will effectively reduce the ripple of the input source. With the addition of capacitors at the input, combined with the interleaved structure, the source can achieve zero ripple.

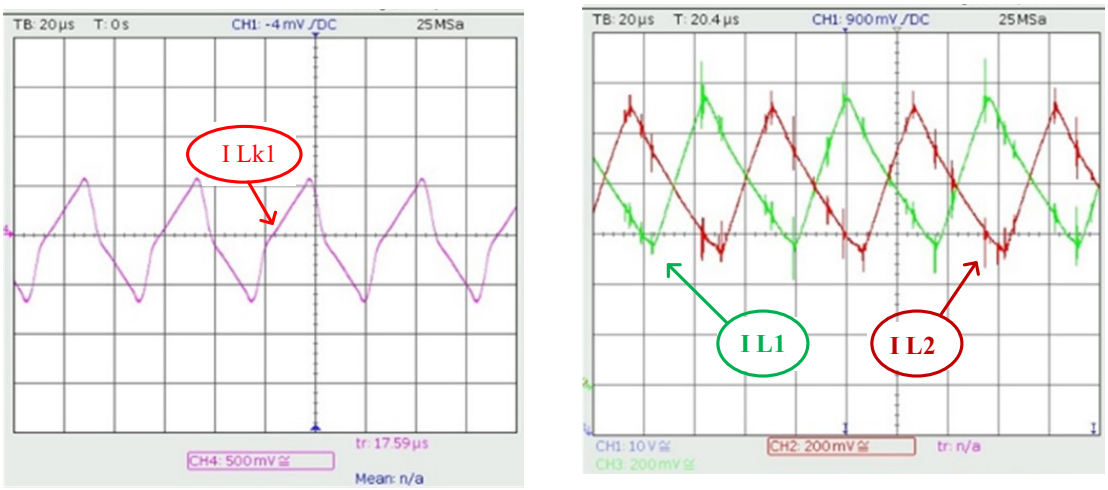


Fig. 5.9 a) Current waveform of the main transformer b) Current waveform of the input inductors [33].

Fig. 5.10 shows the active switch voltage when the output voltage is 380 volts and the duty cycle is 0.4 and 300 W load. It can be seen that the voltage stress on the switch is 60 volts which is much less than the one in [12] and [15] which would be 120 volts for the same output voltage level.

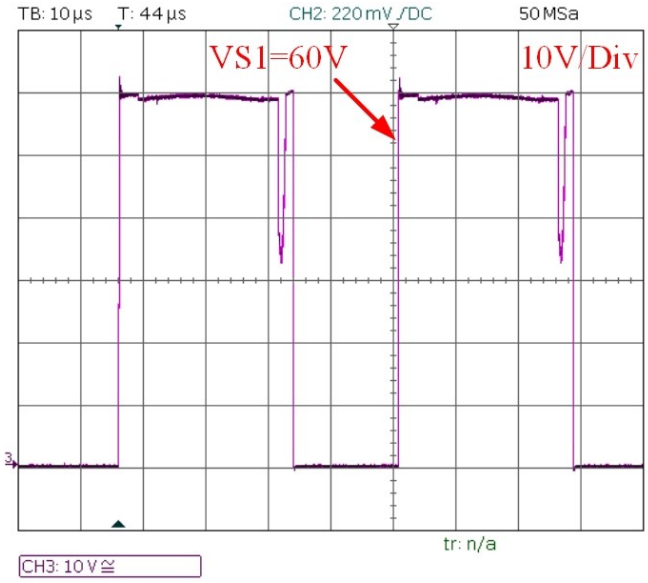


Fig. 5.10 Voltage stress on switch 1 which is the same for all switches [33].

Fig. 5.11 shows the switch currents under ZVS operation for the main and complementary switch under full load of 450 W. The other two switches have the same waveforms only phase shifted 180 degrees.

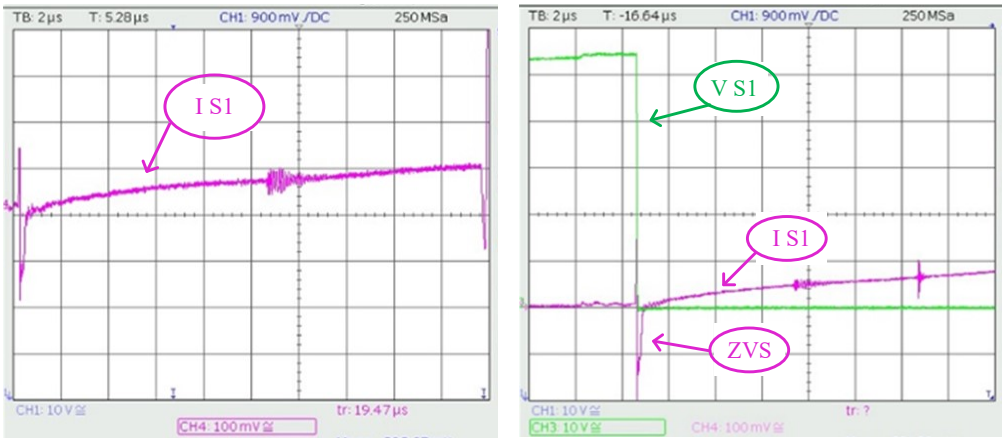


Fig. 5.11 a) Current waveform of switch 1. b) Current and voltage waveforms of switch 1 [33].

Fig. 5.12 shows the voltages and currents of all diodes in a single leg. The other diodes have the exact waveforms only phase shifted 180 degrees.

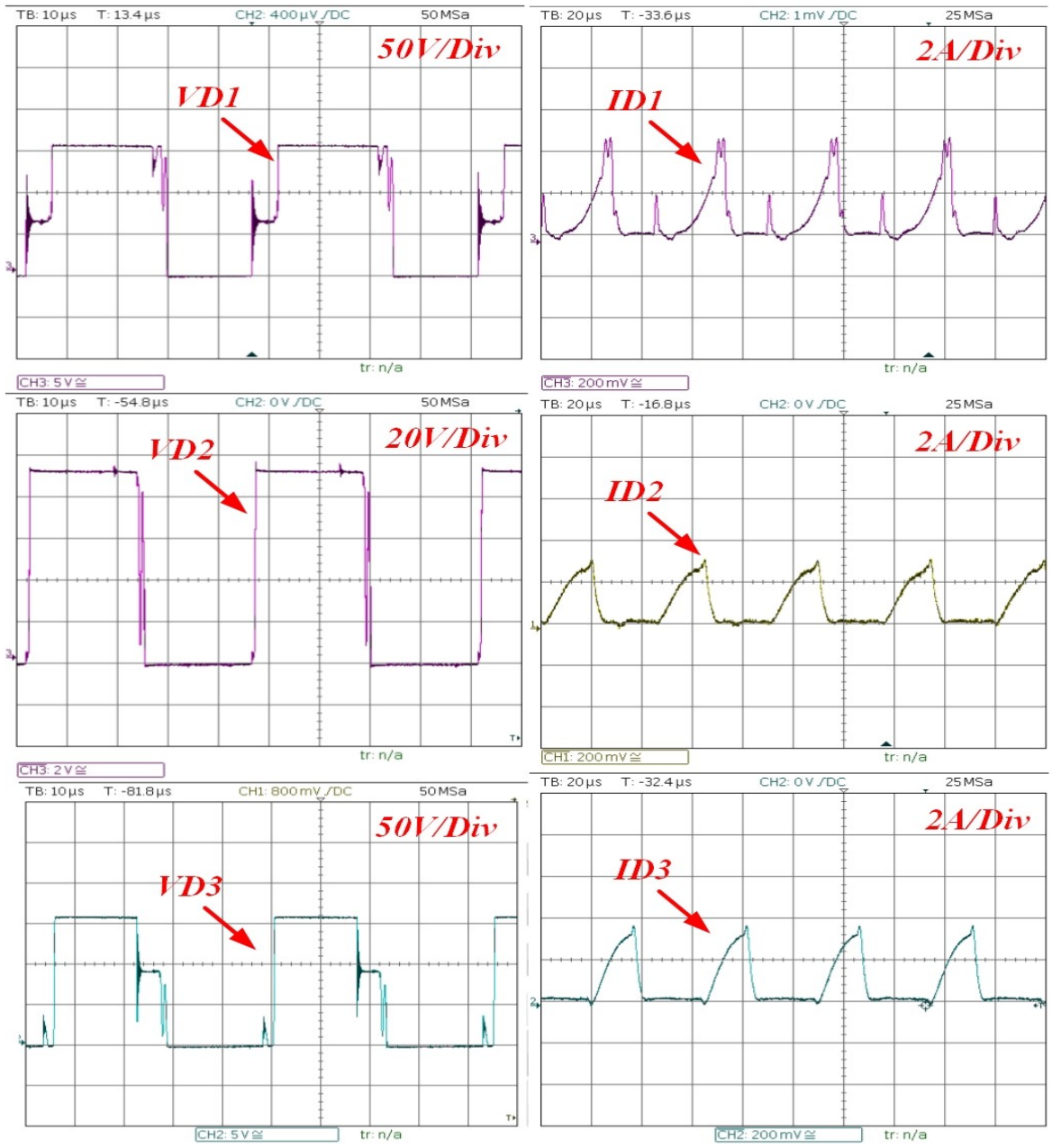


Fig. 5.12 Voltages and currents of diodes 1, 2, and 3 [33].

It can be seen that the waveforms conform to the analysis and it can be seen how diode 1 collects all the leakages. These measurements were performed under a load of 450 ohms. And an output voltage of 380 volts. The efficiency of the converter is found by measuring the input power and

the output power at different loads. Fig. 5.13 shows the overall efficiency of the converter during these loading conditions.

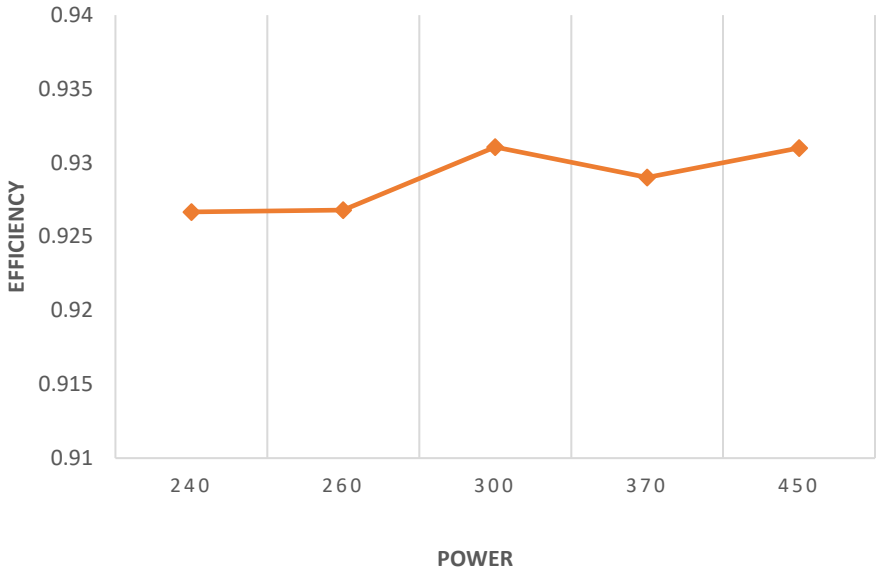


Fig. 5.13 Efficiency of the converter at 37 V input and different loading points [33].

It can be seen that the converter maintains an efficiency of around 93% even at half load. The prototype in [10] for example drops in efficiency from 93% to 90% at half load. In addition, prototype in [11] has a peak efficiency of 96% that drops to 89% at half load. After that, a power loss distribution study was performed under a 320 W load and an output voltage of 380 volts. The losses for different parts of the converter were calculated based on measured currents and datasheet parameters. The following power loss calculations were performed:

$$P_D = I_{D-ave} * V_{DF} * D \tag{5.1}$$

$$P_{s1-s2} = {I_{s1-s2-ave}}^2 * R_{DSon} * D \tag{5.2}$$

$$P_{s3-s4} = {I_{s3-s4-ave}}^2 * R_{DSon} * (1 - D) \tag{5.3}$$

$$P_{L1-L2} = {I_{L1-L2-RMS}}^2 * R_{L1-L2} \tag{5.4}$$

$$P_{snubbers} = C.V^2 * f_{sw} * D \tag{5.5}$$

Where VFD is the diode forward voltage that is given in the data sheet and RDS on is the on resistance of the switch found in the datasheet. RL1 and RL2 are the parasitic input inductor resistances. The Power loss distribution is presented in Fig. 5.14 and shows how losses are distributed in the converter. The transformers are built manually in the lab with twisted pair magnetic wires to reduce the skin effect and proximity effect. However, even though DC resistance can be measured, the effective resistance of the wires can't be defined exactly under that switching frequency and therefore the whole loss of the transformers is combined in the others section. The values of parasitic parameters are considered for the actual temperature and current during the calculation of losses.

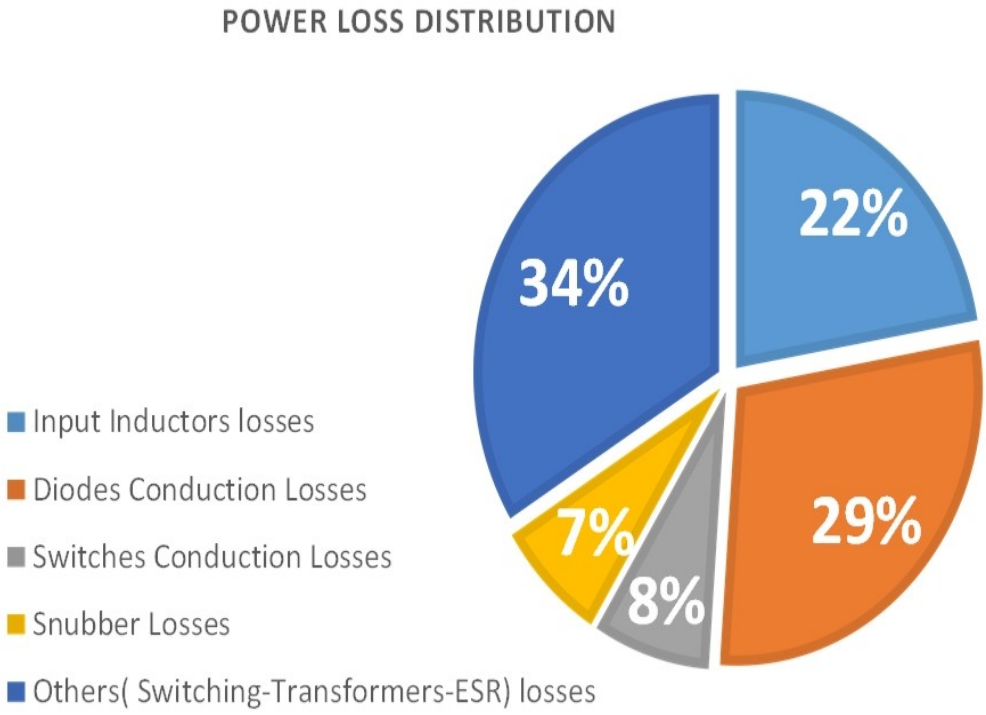


Fig. 5.14 Power loss distribution of the proposed converter [33].

The next procedure is to test the converter with an inverter and a filter as part of a complete system. A half bridge inverter is installed in the PCB board.

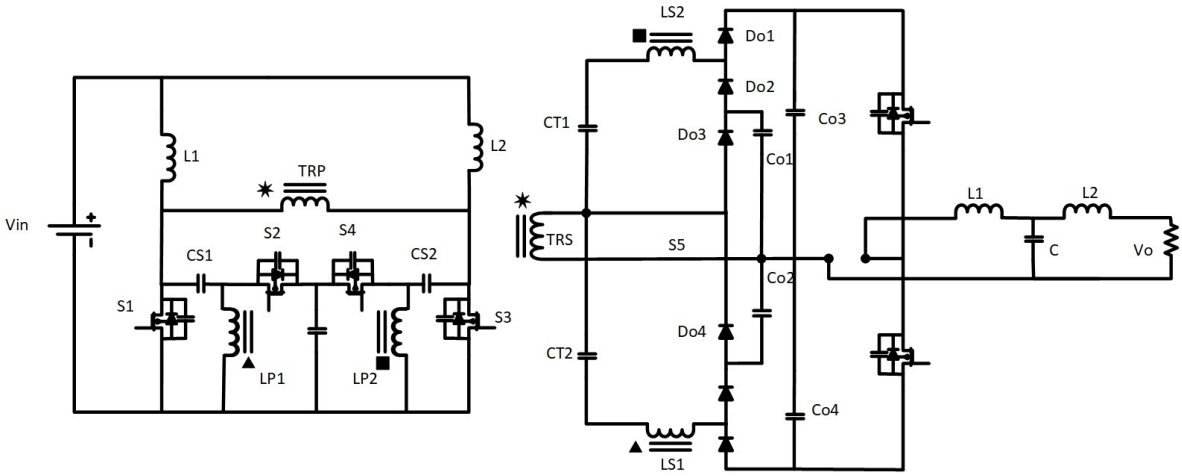


Fig 5.15 Full system diagram.

The inverter is added to the PCB board only by bn adding two MOSFETs. The filter to produce sinusoidal AC waveforms can be either an L filter, LC filter, or and LCL filter. The simplest filter would be an L filter. However, the L filter attenuates harmonics at very high frequencies but causes a high voltage drop [42]. The filter need a capacitor to maintain the voltage and further reduces harmonics. Therefore LC filters have been explored. It is seen that LC filters are more prone to load variations and inrush currents [42]. The LCL filter seems to be the best for attenuation and load variations [42]. The procedure used in [43] is followed to obtain the LCL values of the filter. The complete set up can be seen in figure 5.16:

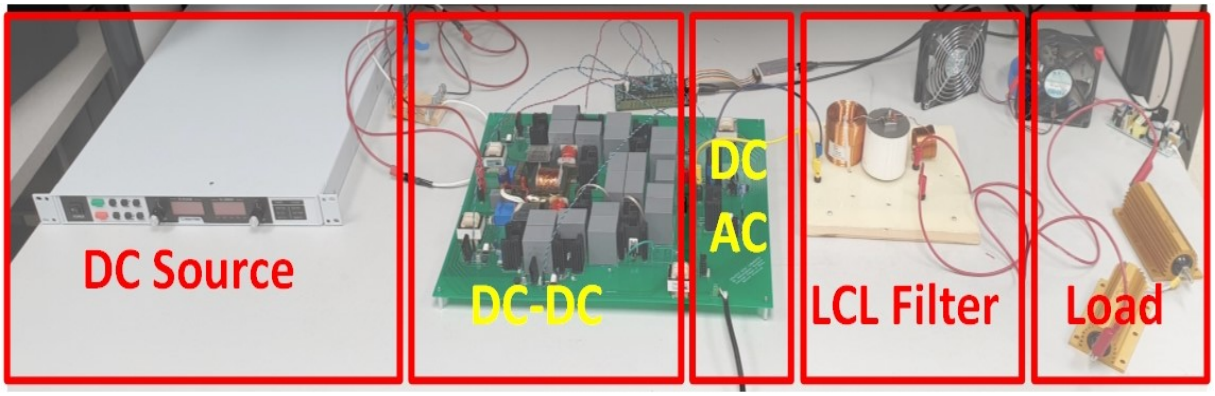


Fig. 5.16 Full system set up.

Output voltage and current were observed at different loading levels. The first waveform shows the PWM output of the half bridge inverter with the LCL filter input inductor current:

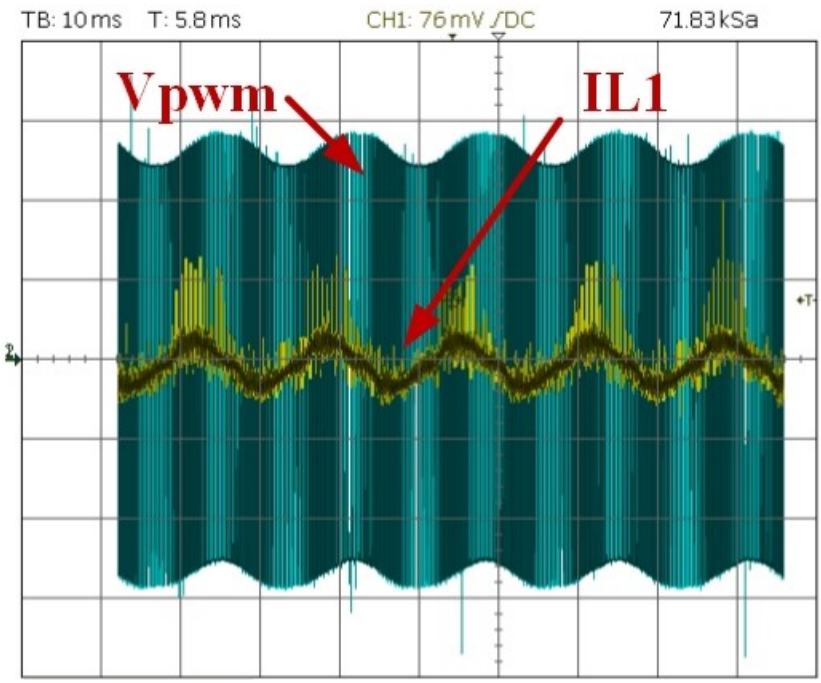


Fig. 5.17 Inverter PWM output voltage and filter input current.

This PWM output is then fed to the LCL filter to produce AC voltage and current at 100 V DC and a 0.75 modulation index at a 300 Ω load in figure 5.18:

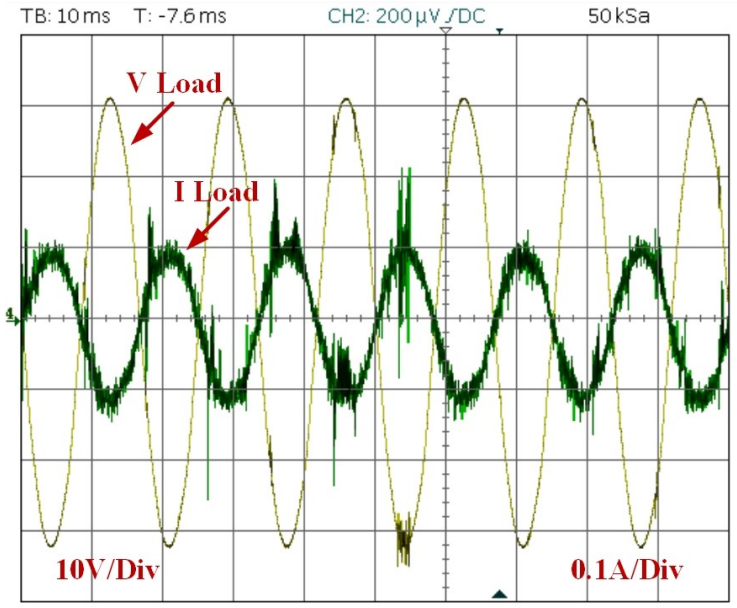


Fig. 5.18 Load voltage and current waveforms at 100V DC and 0.75 modulation index and a 300 Ω load.

The second waveform was measured at 200V DC and a 0.75 modulation index under a 300 Ω load:

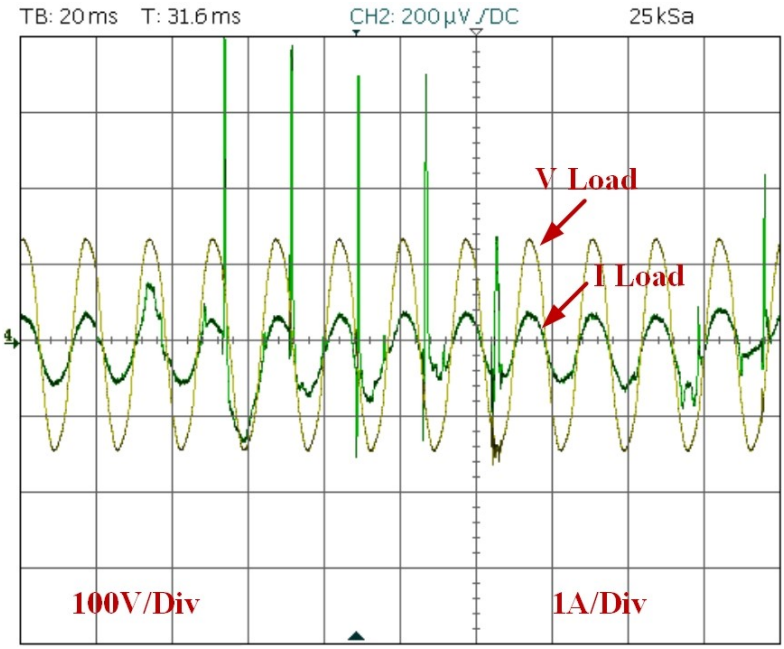


Fig. 5.19 Load voltage and current waveforms at 200V DC and 0.75 modulation index and a 300 Ω load.

It can be seen that the inverter is working properly with the Designed DC-DC converter and the filter produces a pure sine wave AC voltage. To reduce double line to frequency ripples, larger capacitor values will be needed to reduce the ripples' amplitude. However they will still exist because power transfer from capacitors occurs at 120 Hz.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

This Dissertation presented a high voltage gain DC-DC converter that utilizes very low rating components while producing a high step ratio. The proposed converter also reduces the required duty cycle for PV applications. The design equations for the converter have been presented and validated by simulation and experimental results. A 450 W prototype has been designed and built in the laboratory. The experimental results show the ability of the converter to step up the voltage and all the voltage and current waveforms conform to the theoretical waveforms presented. The efficiency of the converter is also studied and presented. The converter under the designed parameters is able to maintain a high efficiency even at half load.

It can be seen that the power loss distribution does not specify the distribution of losses inside the transformer. The transformer losses are calculated is by measuring input and output currents and voltages and then calculating the power loss. It is difficult to specify how much power loss in copper and how much power loss in the core (hysteresis and Eddy currents). The copper losses could be found accurately if the effective AC resistance is found at the operating frequency (25 KHz in our case). However, the value of the effective AC resistance is hard to define without an AC spectrum analysis, especially with the twisted pair. This issue is under heavy investigation and research and one of the early works on it is the Dowell equations in [44]. However, the model developed in [44] received many modifications and was progressed by other researchers to develop a model for copper loss calculations such as [45]. Litz wires also provide AC resistance values in the data sheets under a range of operating frequencies. A comparative table is shown below to illustrate how the proposed converter stands in terms of components count, voltage gain, and voltage stress ratings for active switches and diodes, and the turns' ration for transformers under a 400 V application. It can be seen that the converter presents many advantages on the count of components. However, the rating of these components are about half the ones presented in the other topologies.

Table 6.1: Comparison between proposed converter and other converters

	Duty Ratio	Vs/Vo	Component Count	N1:N2
Converter in [10]	0.8	0.51	15	1:4
Converter in [12]	0.5	0.19	17	1:2
Proposed Converter	0.4	0.157	27	1:1

6.2 Future work

Future applications for this converter could be in medium voltage integration of renewables and energy storage systems. By the way this converter is reducing the rated components, integration of renewable sources could be improved. The nominal voltage value in medium voltage applications is 4 kV. 400 battery systems can be integrated by using this converter and the 650 V MOSFETs can be used in the primary and 3 kV IGBTs can be used in the secondary.

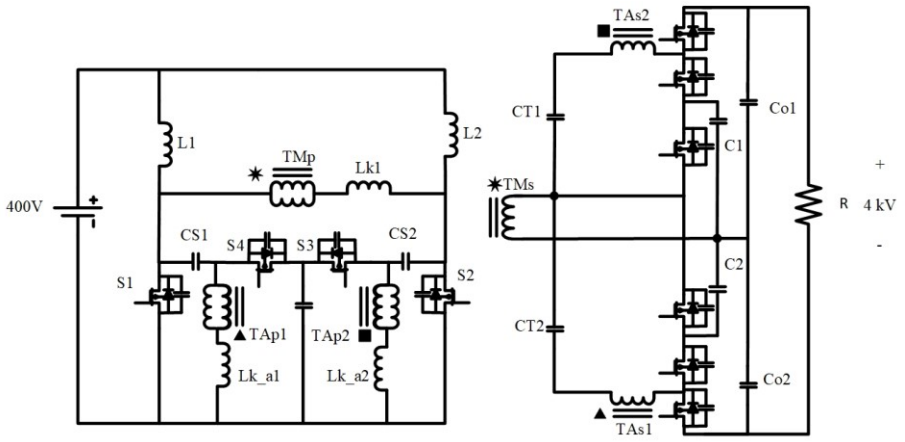


Fig 6.1 Medium voltage possible application for the proposed converter.

In addition, by replacing the diodes with MOSFETs or IGBTs, The converter can operate in a bidirectional manner which served battery applications. The transformers would not require any special insulation levels between primary and secondary since they both will operate at 800 V maximum value for a 4 kV application. Comparable work in [40] can definitely be used as reference to evaluate advantages and disadvantages of the proposed converter.

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