MODELING AND DIGITAL CONTROL OF A SINGLE-PHASE QUASI-Z-SOURCE INVERTER BASED ON TMS320F28335-DSP

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ABSTRACT

One important advantage of quasi-Z-source inverter is that it has a quasi-Z-network, which is consisted of inductors and capacitors, between input DC source and H-Bridge inverter. This quasi-Z-network enables the possibility of simultaneous turning on of both switches in one leg of Inverter Bridge (shoot-through state). The control system design for quasi-Z-source inverter includes two parts, one is the control of quasi-Z-network output DC voltage, which is the input voltage of Inverter Bridge and the other one is standard inverter bridge output AC voltage control. Modelling and control of the quasi-Z-network has been developed in the past. However, most of the work modeled the non-shoot-through state load of quasi-Z-network as a constant current source. My main contribution is to derive a new modeling method, which modeling the quasi-Z-network with three different states instead of two states. The above mentioned traditional modeling method was further improved. A new model will be derived out which could be exclusively decided by input DC voltage and load condition if quasi-Z-network reference output voltage set to constant. Based on this new model, an integral state feedback control algorithm was developed in discrete time domain. For each working condition (input DC voltage and AC load), same control algorithm with specific gain value for this condition was designed. This gain scheduling process could extend the control validity of quasi-Z-network. Another contribution of this thesis is to design a robust control system for Inverter Bridge which could fit for DSP based control system. Successful operation will be illustrated by means of hardware prototype.

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NOMENCLATURE

V_{in}	DC input voltage
V_{PN-NS}	Quasi-Z-Network output voltage at non-shoot-through state
I_{PN-NS}	Quasi-Z-Network output current at non-shoot-through state
$\overline{i_{DC}}$	i_a averaged over one switching cycle
$power$	Total power consumed by load
r	Reference for Quasi-Z-Network output voltage
d	Shoot-through state modulation signal
i_a	Inverter output current
m	Inverter modulation signal
$\overline{i_L}$	Inductor current averaged over one switching cycle
$\overline{v_C}$	Capacitor voltage averaged over one switching cycle
i_{L_1}	Current of L_1
i_{L_2}	Current of L_2
v_{C_1}	Voltage of C_1
v_{C_2}	Voltage of C_2
L_1	One of inductor of Quasi-Z-Network
L_2	One of inductor of Quasi-Z-Network
C_1	One of capacitor of Quasi-Z-Network
C_2	One of capacitor of Quasi-Z-Network
f_s	Sampling frequency
ω_w	W domain rad frequency

CHAPTER 1
INTRODUCTION

This chapter will present an introduction about this thesis. It will present the objectives, background and motivation, and a detailed literature review. In the literature review, the development of Z-Source inverter will be discussed. Then, the modeling and digital control of Quasi-Z-Source converter will be presented. Finally, the proposed modeling and gain scheduling state feedback control method will be explained at scope and contribution part.

1.1 Objective

My objective is to derive a new modeling method, which modeling the quasi-Z-network with three different states instead of two states. The above mentioned traditional modeling method was further improved. A new model will be derived out which could be exclusively decided by input DC voltage and load condition if quasi-Z-network reference output voltage set to constant. Based on this new model, an integral state feedback control algorithm was developed in discrete time domain. For each working condition (input DC voltage and AC load), same control algorithm with specific gain value for this condition was designed. This gain scheduling process could extend the control validity of quasi-Z-network. Another contribution of this thesis is to design a robust control system for Inverter Bridge which could fit for DSP based control system. Successful operation will be illustrated by means of hardware prototype using TMS320F28335.

1.2 Background and Motivation

There are two traditional converters: voltage-source converter and current-source converter. A DC input voltage source connected parallel by a relatively large capacitor provides the main power to the converter circuit, a three-phase inverter or single-phase inverter. The DC input voltage source could be considered as a battery, fuel-cell stack, diode rectifier, or capacitor. Six switches are deployed in the main circuit; each switch is usually consisted of a power transistor and an antiparallel diode, or freewheeling diode, to provide a bidirectional current flow and unidirectional voltage blocking ability. The Voltage-source converter has a widely application. It, however, has the following barriers and limitations, both conceptual and theoretical. [1]

1) The peak AC output voltage is limited below the DC input voltage and cannot exceed the DC input voltage or the DC input voltage has to be set greater than the AC output voltage. Therefore, the Voltage-source inverter is a buck (step-down) inverter for DC-AC power conversion and the Voltage-source converter is a boost (step-up) rectifier (or boost converter) for AC-DC power

conversion. For applications where step up inverter is desirable and the available DC voltage is limited, an additional DC-DC boost converter is needed to obtain a desired AC voltage. The additional power converter stage is necessary which increases system cost and lowers system efficiency. [1]

2) The upper and lower switches of each phase leg cannot be switched on at the same time either by purpose or by EMI noise. Otherwise, a short circuit would occur and destroy the switches and power devices. The short circuit problem by electromagnetic interference (EMI) noise's mis-turn on is a major problem to the converter's reliability. Dead time to block both upper and lower switches has to be introduced into the Voltage-source converter, which could cause waveform distortion, etc. [1]
3) An output LC filter is needed for providing a sinusoidal voltage compared with the current-source inverter, which causes additional power loss and control complexity. [1]

To overcome the above problems, a topology called Z-source converter was developed and its control method for achieving DC-AC, AC-DC, AC-AC, and DC-DC power conversion. And in the following years, a Quasi-Z source converter topology was developed. It employs a different impedance network (or circuit) to couple the inverter main circuit to the input DC power source, load, or another converter, for the purpose of providing unique features that cannot be observed in the traditional Voltage-converters where a capacitor are used. The Quasi-Z-source converter overcomes the above-mentioned conceptual and theoretical disadvantages. [1] As its improved topologies increasing each year, control techniques of qZSI was rarely discussed. Because of this reasons, I started working on research the modeling and control method of Quasi-Z-Source inverter.

1.3 Literature Review

This section details the background and literature on the development from Z-source-inverter to Quasi-Z-source inverter; modeling and control of Quasi-Z-source inverter; digital control design of Quasi-Z-source inverter.

1.4 Z-Source Inverter

The Z-source inverter presented in [1] is a relatively new converter topology whose main character is that it has a fully reactive network, which is composed of inductors and capacitors, between input DC voltage source and H-Bridge Inverter. In a traditional voltage source inverter (VSI), the two switches in one leg of a H-Bridge inverter should not be turned on at the same time because this action short-circuits the input DC voltage source. The inclusion of a impedance network —the Z network— between input DC voltage source and H-Bridge inverter enables the utilization of this short-circuit condition, i.e. the shoot-through state, to achieve voltage boost ability. Hence, the Z-source inverter can

be regarded as the combination of a DC-DC boost converter with a voltage source inverter without using an extra power switches. [12]

1.5 Quasi-Z-Source Inverter

Quasi-Z-source inverters (qZSIs) [2] are improved topology of the Z-Source inverter topology that preserves Z-source-inverter main advantages (Z network, shoot-through mode) and improves on other disadvantages. Especially, there exist a voltage source input qZSIs that absorb continuous current from the input DC voltage source and have a common reference DC bus shared by the input DC voltage source and output of the quasi-Z-network (the input DC bus of inverter bridge). This voltage-fed qZSI with continuous input current, because of a input inductor, is well suited to DC-AC application where use photovoltaic as input voltage sources which requires minimum current harmonics for the purpose of increasing lifetime of PV. Also, the above mentioned common reference DC ground bus facilitates the measurement of electrical variables, which are required for inverter control, and in favors of EMI reduction. A single-phase voltage-fed quasi-Z-source inverter with continuous input current is shown in Figure 1.1. [12]

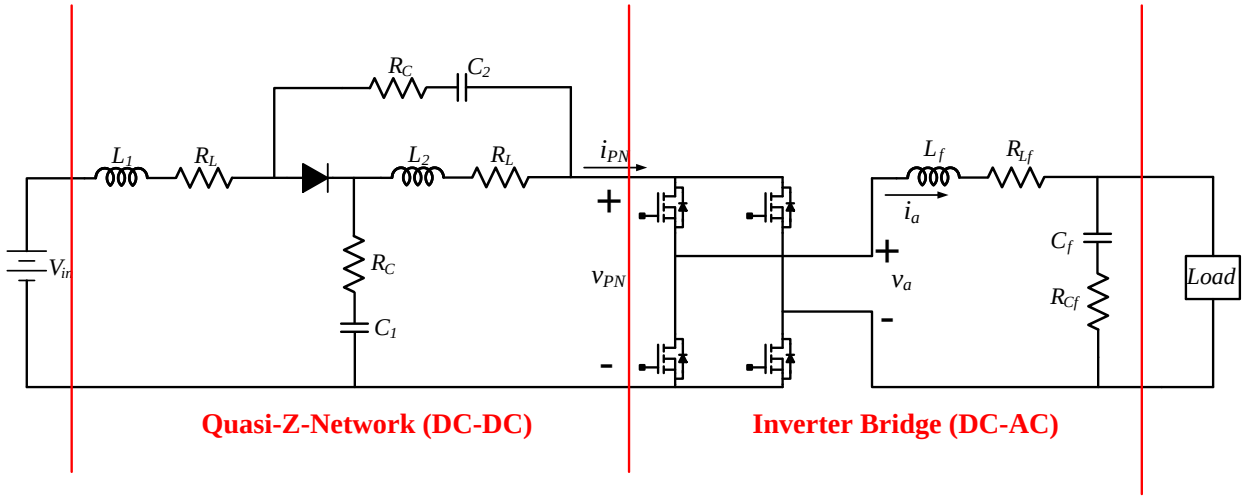


Figure 1. 1 Single-phase quasi-Z-source inverter

1.6 Modeling of Quasi-Z-Source Network

Typical working condition of the qZSI requires control the quasi-Z-network output DC voltage, hereafter the DC bus voltage, to a constant reference voltage so that traditional voltage source inverter control can be conducted in the same way as for a standard VSI with constant inverter bridge input DC voltage. Control of the DC bus voltage can be performed through the control of the shoot-through duty-cycle and inverter bridge is controlled by traditional PWM modulation techniques, including the provision for shoot-through mode. [12]

Traditional PWM modulation method is alternating PWM active state, where power is transmitted from DC bus to AC load, and null state, where DC bus and AC load are disconnected, four times over one PWM switching period, and repeating this alternation. The shoot-through state happens during null state, when at least three out of the four switches are turned on in the single-phase inverter bridge, short circuiting both the DC voltage bus and the filter circuit. Hence, shoot-through state is only happened while the traditional PWM modulation generates a null satte. How active state, null state, and nshoot-through state occur over time, are illustrated in Figure 1.2, where d denotes the shoot-through state, m active state and 1-d-m null state. [12]

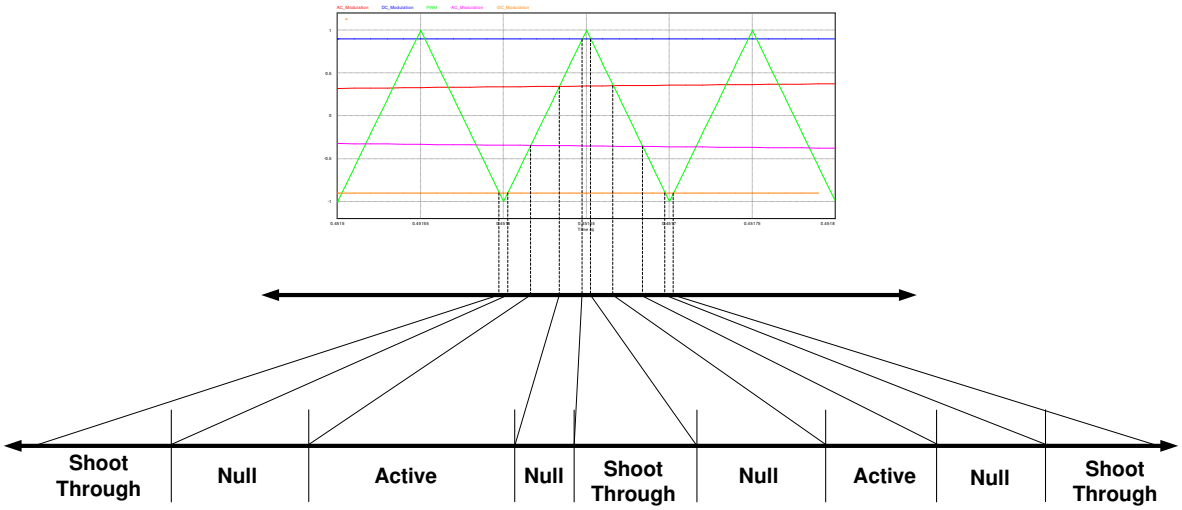


Figure 1. 2 Different working states of quasi-Z-network.

As of modeling the quasi-Z-network, one important issue is how to model the quasi-Z-network load at active state. Although much efforts have been dedicated to modelling and controlling the Z-Source converters, most of the existing papers concentrate on modeling of three-phase quasi-Z-source inverters, whose essential difference with respect to single-phase quasi-Z-source inverters is that the quasi-Z-network output DC current contains a second-order harmonics during non-shoot-through states, this is due to the power balance between DC side of inverter and AC side of inverter. In [3], the load of Z-network during non-shoot-through state of a three-phase Z-Source inverter is modelled as a resistor. Similarly, [4] and [5] model the H-Bridge inverter and its AC load as a current source during non-shoot-through states. Their main disadvantages are that they did not separate the null state and active state. Model quasi-Z-network load in different states becomes especially important in the single-phase inverter modeling since that current during non-shoot-through states could not be considered constant during this time interval. The contributions of papers like [6], [7] and [8] is to substitute the three-phase inverter and its balanced AC load into an equivalent resistor and inductor circuit connected to the Z-network output.

Again, this model method could not be directly utilized in the modelling of a single-phase inverter because of the DC bus second order harmonics during shoot-through states. In [9], a qZSI dynamic model is derived based on physical circuit rather than mathematical method. [10] presents a state-space averaged model, obtaining the same results as [4] but ignoring input DC voltage and load current disturbance in the process of controller design. Like in other models discussed before, the DC bus current is modelled as a constant current source, but the relationship between this current source and the H-Bridge inverter AC load is not clear. [12]

1.7 Control Design System of Quasi-Z-Source Network

As of the control method for Quasi-Z-Source network, most of the proposed control method is either limited to a certain input voltage and load condition or without an integral part in their controller design which makes the DC network output voltage have a big steady state error compared with the reference. [11] obtained the transfer function from a state space averaging model and designed a traditional PI controller based on this transfer function. However this way of control could not fit for a large range of load change or input voltage change. This problem was solved by the paper [12], which utilized gain scheduling state feedback method to extend the validity of the model, but there is no integral part in the controller. This could will results in a faster response but big steady state error. Except these problems, there is no paper presented digital control design of qZSI, which is necessary for DSP based control system.

1.8 Control System Design of VSI

Control system design of single phase inverter is highly developed [13] [14]. Since the purpose of this thesis is to demonstrate the qZSI on hardware using TMS320F28335 DSP, thus digital control system design is a key issue. Unlike analog controller, there is a calculation delay inside DSP for digital control system, which makes designing the digital controller in z domain necessary, instead of designing controller in s domain and then transferred to z domain. [15] showed a robust control design with delay compensation.

1.9 Thesis Scope and Contributions

My main contribution is to derive a new modeling method, which modeling the quasi-Z-network with three different states instead of two states. The modeling method presented in [12] would be further improved. A new model will be derived out which could be exclusively decided by input DC voltage and load condition if quasi-Z-network reference output voltage set to constant. Thesis will also show how the model can be successfully employed in the design of digital control system for Quasi-Z-Network. Digital control system design of voltage source inverter will also be presented in detail.

Finally, a Quasi-Z-Source inverter will be constructed and proposed digital control method will be demonstrated on the hardware. All control functions will be executed by TMS320F28335-DSP. Additionally, the hardware will include additional ancillary circuits that are necessary for good function of hardware, including: gate drivers, analog signal measurement, and overvoltage and overcurrent protection. This prototype will be demonstrated and experimental results presented.

1.10 Project Outline

This thesis is structured in 6 chapters:

Chapter 1 is an introduction to the project, containing short background, the project motivation and the goals of the project.

Chapter 2 contains the detail development of modeling of Qusai-Z-Source inverter and its digital control system design.

Chapter 3 presents elements selection; gate drive design; PCB design; DSP programing

Chapter 4 showed hardware prototype testing and results

Chapter 5 is the conclusion, which includes also future work.

CHAPTER 2

MATHEMATICAL AND ENGINEERING ANALYSIS

2.1 Introduction

This chapter will present the mathematical analysis of the single-phase Quasi-Z-Source inverter and its control method. It will present the details of modeling method for qZSI. Upon the derived model, a gain scheduling state feedback digital control method will be described.

2.2 Modeling of Single-Phase Quasi-Z-Source inverter

Figure 2.1 shows the qZSI circuit subjected to be analyzed. Considering the asymmetric quasi-Z-source network, there are four state variables: the currents through two inductors $\boldsymbol{i_{L_1}}$ and $\boldsymbol{i_{L_2}}$ and the voltages across the capacitors $\boldsymbol{v_{C_1}}$ and $\boldsymbol{v_{C_2}}$. The system output is $\boldsymbol{v_{C_1} + v_{C_2}}$, system input is $\boldsymbol{v_{in}}$ and $\boldsymbol{i_a}$. Qusai-Z-Source inverter has three operating states, including shoot-through state($\boldsymbol{d}$), null state($\boldsymbol{n}$) and active state($\boldsymbol{m}$), as presented in Figure 1.2. Active state is represented by the modulation signal $\boldsymbol{m}$ for the AC side voltage control of H-bridge. Shoot-through state is represented by the modulation signal $\boldsymbol{d}$ for the DC side voltage control of H-bridge. $\boldsymbol{m + n + d}$ represents the one switching cycle. Following paragraph will discuss these three operating states.

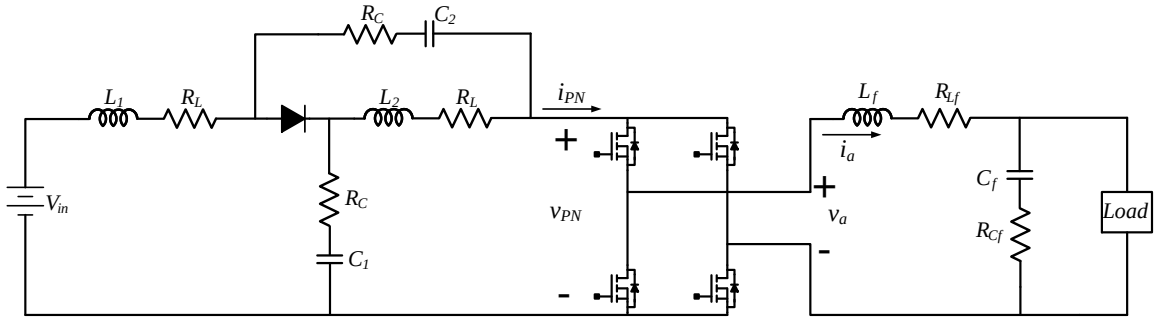


Figure 2. 1 Single-phase Quasi-Z Source inverter.

As analyzed before, there are three states for the operating of quasi-Z-source inverter. In traditional modeling method, only two states were considered in the modeling process, which is shoot-through state and non-through state. However, in non-shoot-through state, there are two separate states: one is null state, the other state is active state. Because null state is short and no power transmission, researchers usually combine it together with active state. This modeling method could limit the range of application of the developed model. This thesis will consider null state and active state separately.

At the shoot-through state shown in Figure 2.2, the capacitors transfer their electrostatic energy to magnetic energy stored in the inductors. The differential equations are derived as below. [11]

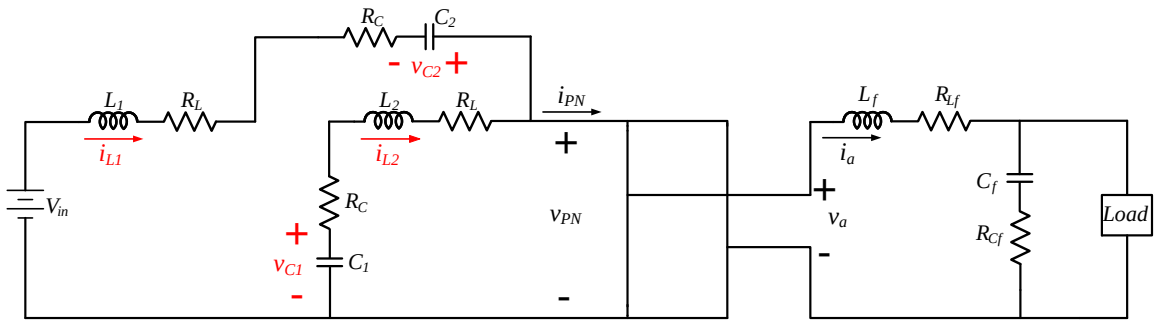


Figure 2. 2 Quasi-Z-Network in shoot-through state.

$$\begin{cases} \boldsymbol{L_1 \frac{di_{L_1}}{dt} = V_{in} + v_{C_2} - (R_c + R_L) \cdot i_{L_1}} \\ \boldsymbol{L_2 \frac{di_{L_2}}{dt} = v_{C_1} - (R_c + R_L) \cdot i_{L_2}} \\ \boldsymbol{C_1 \frac{dv_{C_1}}{dt} = -i_{L_2}} \\ \boldsymbol{C_2 \frac{dv_{C_2}}{dt} = -i_{L_1}} \end{cases} \tag{2.1}$$

The state space equation is

$$\boldsymbol{\frac{df}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} -\frac{R_c+R_L}{L_1} & 0 & 0 & \frac{1}{L_1} \\ 0 & -\frac{R_c+R_L}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ -\frac{1}{C_2} & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{in} \\ i_a \end{bmatrix}} \tag{2.2}$$

$$\boldsymbol{\dot{x} = A_s x + F_s v} \tag{2.3}$$

Where

$$\boldsymbol{A_s = \begin{bmatrix} -\frac{R_c+R_L}{L_1} & 0 & 0 & \frac{1}{L_1} \\ 0 & -\frac{R_c+R_L}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ -\frac{1}{C_2} & 0 & 0 & 0 \end{bmatrix} \quad F_s = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad x = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} \quad v = \begin{bmatrix} V_{in} \\ i_a \end{bmatrix}}$$

At the null state shown in Figure 2.3, the dc power source, as well as the inductors, begins to charge the capacitors. The H-bridge is opened. The differential equations are derived as below.

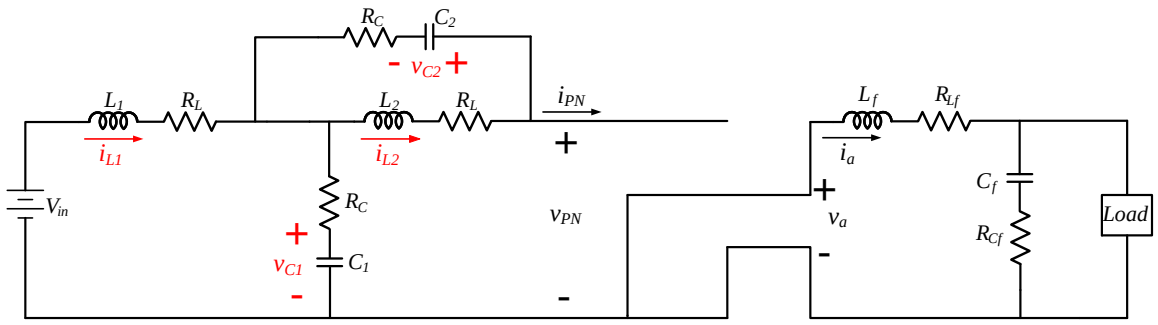


Figure 2. 3 Quasi-Z-Network in null state.

$$\begin{cases} \boldsymbol{L_1 \frac{di_{L_1}}{dt} = V_{in} - v_{C_1} - (R_c + R_L) \cdot i_{L_1}} \\ \boldsymbol{L_2 \frac{di_{L_2}}{dt} = -v_{C_2} - (R_c + R_L) \cdot i_{L_2}} \\ \boldsymbol{C_1 \frac{dv_{C_1}}{dt} = i_{L_1}} \\ \boldsymbol{C_2 \frac{dv_{C_2}}{dt} = i_{L_2}} \end{cases} \tag{2.4}$$

The state space equation is

$$\boldsymbol{\frac{df}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} -\frac{R_c+R_L}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_c+R_L}{L_2} & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{in} \\ i_a \end{bmatrix}} \tag{2.5}$$

$$\boldsymbol{\dot{x} = A_N x + F_N v} \tag{2.6}$$

where

$$\boldsymbol{A_N = \begin{bmatrix} -\frac{R_c+R_L}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_c+R_L}{L_2} & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \quad F_N = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad x = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} \quad v = \begin{bmatrix} V_{in} \\ i_a \end{bmatrix}}$$

At the active state shown in Figure 2.3, the dc power source, as well as the inductors, charges and powers the external ac load, boosting the dc voltage across the H-bridge. The differential equations are derived as below. [11]

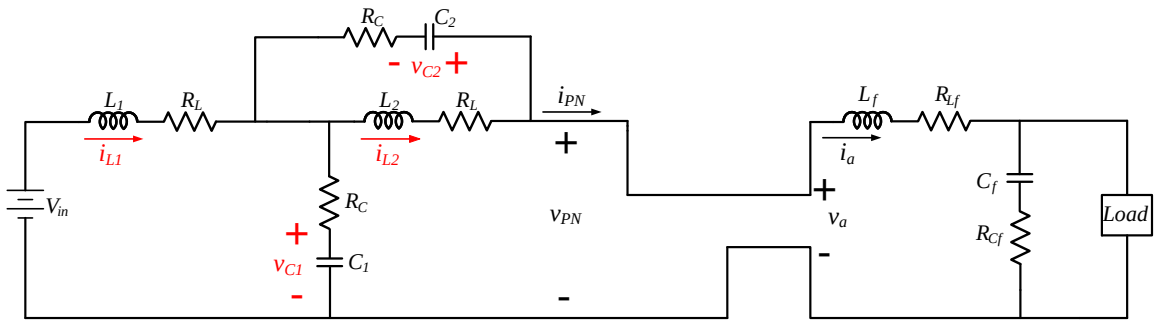


Figure 2. 4 Quasi-Z-Network in active state.

$$\begin{cases} \boldsymbol{L_1 \frac{di_{L_1}}{dt} = V_{in} - v_{C_1} - (R_c + R_L) \cdot i_{L_1}} \\ \boldsymbol{L_2 \frac{di_{L_2}}{dt} = -v_{C_2} - (R_c + R_L) \cdot i_{L_2}} \\ \boldsymbol{C_1 \frac{dv_{C_1}}{dt} = i_{L_1} - i_a} \\ \boldsymbol{C_2 \frac{dv_{C_2}}{dt} = i_{L_2} - i_a} \end{cases} \tag{2.7}$$

$$\boldsymbol{\frac{df}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} -\frac{R_c+R_L}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_c+R_L}{L_2} & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & -\frac{1}{C_1} \\ 0 & -\frac{1}{C_2} \end{bmatrix} \cdot \begin{bmatrix} V_{in} \\ i_a \end{bmatrix}} \tag{2.8}$$

$$\boldsymbol{\dot{x} = A_A x + F_A v} \tag{2.9}$$

Where

$$\boldsymbol{A_A = \begin{bmatrix} -\frac{R_c+R_L}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_c+R_L}{L_2} & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \quad F_A = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & -\frac{1}{C_1} \\ 0 & -\frac{1}{C_2} \end{bmatrix} \quad x = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} \quad v = \begin{bmatrix} V_{in} \\ i_a \end{bmatrix}}$$

For one switching cycle, the length of shoot through state is $\boldsymbol{d}$, the length of active state is $\boldsymbol{m}$, the length of null state is $\boldsymbol{1 - d - m}$. The state-space averaged equations over one switching cycle can be obtained as

$$\boldsymbol{\dot{\bar{x}} = (A_s \bar{x} + F_s \bar{v}) \cdot d + (A_n \bar{x} + F_n \bar{v}) \cdot (1 - d - m) + (A_a \bar{x} + F_a \bar{v}) \cdot m}$$

$$\boldsymbol{\dot{\bar{x}} = (A_s d + A_n (1 - d - m) + A_a m) \cdot \bar{x} + (F_s d + F_n (1 - d - m) + F_a m) \cdot \bar{v}} \tag{2.10}$$

The derived state space equation is

$$\frac{df}{dt}\begin{bmatrix}\overline{i_{L_1}}\\ \overline{i_{L_2}}\\ \overline{v_{C_1}}\\ \overline{v_{C_2}}\end{bmatrix}=\begin{bmatrix}-\frac{R_c+R_L}{L_1} & 0 & -\frac{1-d}{L_1} & \frac{d}{L_1}\\ 0 & -\frac{R_c+R_L}{L_2} & \frac{d}{L_1} & -\frac{1-d}{L_2}\\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0\\ -\frac{d}{C_2} & \frac{1-d}{C_2} & 0 & 0\end{bmatrix}\cdot\begin{bmatrix}\overline{i_{L_1}}\\ \overline{i_{L_2}}\\ \overline{v_{C_1}}\\ \overline{v_{C_2}}\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1} & 0\\ 0 & 0\\ 0 & -\frac{1}{C_1}\\ 0 & -\frac{1}{C_2}\end{bmatrix}\cdot\begin{bmatrix}\overline{V_{in}}\\ m\cdot i_a\end{bmatrix} \tag{2.11}$$

$$\dot{x}=A_4x+F_4v \tag{2.12}$$

where

$$A_4=\begin{bmatrix}-\frac{R_c+R_L}{L_1} & 0 & -\frac{1-d}{L_1} & \frac{d}{L_1}\\ 0 & -\frac{R_c+R_L}{L_2} & \frac{d}{L_1} & -\frac{1-d}{L_2}\\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0\\ -\frac{d}{C_2} & \frac{1-d}{C_2} & 0 & 0\end{bmatrix}\quad F_4=\begin{bmatrix}\frac{1}{L_1} & 0\\ 0 & 0\\ 0 & -\frac{1}{C_1}\\ 0 & -\frac{1}{C_2}\end{bmatrix}\quad x=\begin{bmatrix}\overline{i_{L_1}}\\ \overline{i_{L_2}}\\ \overline{v_{C_1}}\\ \overline{v_{C_2}}\end{bmatrix}\quad v=\begin{bmatrix}\overline{V_{in}}\\ m\cdot i_a\end{bmatrix}$$

In the state space averaged function, $m\cdot i_a$ represents the inverter output current, which only appeared at active state space equation, averaged over one switching cycle, noted as (2.13). I_{PN-NS} represents i_a averaged over non-shoot-through state ($1-d$), as shown at equation (2.14).

$$\overline{i_{DC}}=m\cdot i_a \tag{2.13}$$

$$I_{PN-NS}=\frac{i_{L_f}\cdot m}{1-d}=\frac{\overline{i_{DC}}}{1-d} \tag{2.14}$$

The relationship between these three averaged current is explained by Figure 2.5

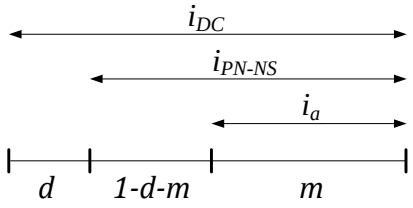


Figure 2. 5 Averaged current representaiton in one switching cycle.

A standard design criterion for Z-source inverters is to select equal L1 and L2 inductance values and equal C1 and C2 capacitance values. Consequently, if $L=L_1=L_2$ and $C=C_1=C_2$, the averaged model (2.12) becomes simpler when rewritten in terms of the new state variables [12]

$$\begin{cases} \overline{i_L} = \overline{i_{L_1}} + \overline{i_{L_2}} \\ \overline{v_C} = \overline{v_{C_1}} + \overline{v_{C_2}} \end{cases} \tag{2.15}$$

The averaged model in these new variables becomes

$$\frac{df}{dt}\begin{bmatrix} \overline{i_L} \\ \overline{v_C} \end{bmatrix} = \begin{bmatrix} -\frac{R_c+R_L}{L} & -\frac{1-2d}{L} \\ \frac{1-2d}{C} & 0 \end{bmatrix} \cdot \begin{bmatrix} \overline{i_L} \\ \overline{v_C} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{2}{C} \end{bmatrix} \begin{bmatrix} \overline{V_{in}} \\ \overline{i_{DC}} \end{bmatrix} \tag{2.16}$$

$$\dot{x} = Ax + Fv \tag{2.17}$$

where

$$A = \begin{bmatrix} -\frac{R_c+R_L}{L} & -\frac{1-2d}{L} \\ \frac{1-2d}{C} & 0 \end{bmatrix} \quad F = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{2}{C} \end{bmatrix} \quad x = \begin{bmatrix} \overline{i_L} \\ \overline{v_C} \end{bmatrix} \quad v = \begin{bmatrix} \overline{V_{in}} \\ \overline{i_{DC}} \end{bmatrix}$$

This averaged model is non-linear because the A matrix contains the control input variable d. In order to separate d from A matrix, (2.16) will be linearized at a steady state working condition as (2.18) (2.19) described, where $x_{ss} = [I_L \quad V_C = r]$. r is the reference of Quasi-Z-Source network output voltage in feedback control system. [17]

$$A = \frac{\partial A}{\partial x}|_{d=D} \tag{2.18}$$

$$B = \frac{\partial A}{\partial d}|_{x=x_{ss}} \tag{2.19}$$

All the state variables could be separated into AC value and DC value as follows

$$\begin{cases} \overline{i_L} = \widetilde{i_L} + I_L \\ \overline{v_C} = \widetilde{v_C} + V_C \\ \overline{i_{DC}} = \widetilde{i_{DC}} + I_{DC} \\ \overline{V_{in}} = \widetilde{v_{in}} + V_{IN} \\ d = \tilde{d} + D \end{cases} \tag{2.20}$$

At the steady state point, V_C and I_L has following relationship (will be explained at next chapter)

$$V_C = \frac{1}{1-2D} V_{IN} \tag{2.21}$$

$$I_L = \frac{2}{1-2D} I_{DC} \tag{2.22}$$

During the linearizing process, DC value will be canceled, left only the AC variable. The linearized model is shown at (2.23)

$$\frac{df}{dt}\begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_C} \end{bmatrix} = \begin{bmatrix} -\frac{R_c+R_L}{L} & -\frac{1-2D}{L} \\ \frac{1-2D}{C} & 0 \end{bmatrix} \cdot \begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_C} \end{bmatrix} + \begin{bmatrix} \frac{2V_C}{L} \\ -\frac{2I_L}{C} \end{bmatrix} \cdot \tilde{d} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{2}{C} \end{bmatrix} \cdot \begin{bmatrix} \widetilde{v_{in}} \\ \widetilde{i_{DC}} \end{bmatrix} \tag{2.23}$$

$$\dot{x} = Ax + Bu + Fv \tag{2.24}$$

where

$$A = \begin{bmatrix} -\frac{R_c+R_L}{L} & -\frac{1-2D}{L} \\ \frac{1-2D}{C} & 0 \end{bmatrix} \quad B = \begin{bmatrix} \frac{2V_C}{L} \\ -\frac{2I_L}{C} \end{bmatrix} \quad F = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{2}{C} \end{bmatrix} \quad x = \begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_C} \end{bmatrix} \quad v = \begin{bmatrix} \widetilde{v_{in}} \\ \widetilde{i_{DC}} \end{bmatrix} \quad u = [\tilde{d}]$$

Based on (2.21) (2.22), (2.25) could be derived out.

$$\begin{cases} -\frac{1-2D}{L} = -\frac{V_{in}}{rL} \\ \frac{1-2D}{C} = \frac{V_{in}}{rC} \\ \frac{2V_C}{L} = \frac{2r}{L} \\ -\frac{2I_L}{C} = -\frac{4rI_{DC}}{CV_{in}} \end{cases} \tag{2.25}$$

Then, the new model comes as follow

$$\frac{df}{dt}\begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_C} \end{bmatrix} = \begin{bmatrix} -\frac{R_c+R_L}{L} & -\frac{V_{in}}{rL} \\ \frac{V_{in}}{rC} & 0 \end{bmatrix} \cdot \begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_C} \end{bmatrix} + \begin{bmatrix} \frac{2r}{L} \\ -\frac{4rI_{DC}}{CV_{in}} \end{bmatrix} \cdot \tilde{d} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{2}{C} \end{bmatrix} \cdot \begin{bmatrix} \widetilde{v_{in}} \\ \widetilde{i_{DC}} \end{bmatrix} \tag{2.26}$$

Since I_{DC} is hard to determine, I transfer I_{DC} to $power$, which is easy to decide once AC output voltage reference is set. The following is derivation.

Since

$$\begin{cases} v_a = M \cdot V_{PN-NS} \cdot \sin(\omega t) = V_a \cdot \sin(\omega t) \\ i_a = I_a \cdot \sin(\omega t - \emptyset) \end{cases} \tag{2.26}$$

therefore

$$v_a \cdot i_a = V_a I_a \sin(\omega t) \sin(\omega t - \emptyset)$$

$$= \frac{V_a I_a}{2}\cos(\varphi) - \frac{V_a I_a}{2}\cos(2\omega t - \varphi)$$

$$= \frac{M \cdot V_{PN-NS} \cdot I_a}{2}\cos(\varphi) - \frac{M \cdot V_{PN-NS} \cdot I_a}{2}\cos(2\omega t - \varphi) \tag{2.27}$$

During the active state, the power is transmitted from DC side to AC side; while, during the shoot-through state, there is no power transmission because the DC-link voltage is zero. Considering the switch frequency is greater than the AC voltage frequency, the instantaneous power balance equation is obtained as [18]

$$v_a \cdot i_a = V_{PN-NS} \cdot I_{PN-NS} \cdot (1-d) \tag{2.28}$$

$$= V_{PN-NS} \cdot \frac{\overline{i_{DC}}}{1-d} \cdot (1-d)$$

$$= V_{PN-NS} \cdot \overline{i_{DC}}$$

Compare (2.27) and (2.28), comes out to be

$$V_{PN-NS} \cdot \overline{i_{DC}} = \frac{M \cdot V_{PN-NS} \cdot I_a}{2}\cos(\varphi) - \frac{M \cdot V_{PN-NS} \cdot I_a}{2}\cos(2\omega t - \varphi)$$

$$\overline{i_{DC}} = I_{DC} + \widetilde{i_{DC}} = \frac{M \cdot I_a}{2}\cos(\varphi) - \frac{M \cdot I_a}{2}\cos(2\omega t - \varphi)$$

$$I_{DC} = \frac{M \cdot I_a}{2}\cos(\varphi) \tag{2.29}$$

because of

$$power = \frac{V_a \cdot I_a}{2}\cos(\varphi) = V_{PN-NS}\frac{M \cdot I_a}{2}\cos(\varphi)$$

thus

$$I_{DC} = \frac{power}{V_{PN-NS}} = \frac{power}{r} \tag{2.30}$$

And hence comes the new model

$$\frac{df}{dt}\begin{bmatrix}\widetilde{i_L}\\ \widetilde{v_C}\end{bmatrix} = \begin{bmatrix}-\frac{R_c+R_L}{L} & -\frac{V_{in}}{rL}\\ \frac{V_{in}}{rC} & 0\end{bmatrix}\cdot\begin{bmatrix}\widetilde{i_L}\\ \widetilde{v_C}\end{bmatrix} + \begin{bmatrix}\frac{2r}{L}\\ -\frac{4 \cdot power}{CV_{in}}\end{bmatrix}\cdot\widetilde{d} + \begin{bmatrix}\frac{1}{L} & 0\\ 0 & -\frac{2}{C}\end{bmatrix}\cdot\begin{bmatrix}\widetilde{v_{in}}\\ \widetilde{i_{DC}}\end{bmatrix} \tag{2.31}$$

$$\dot{x} = A_c x + B_c u + F_c v \tag{2.32}$$

where

$$A_c = \begin{bmatrix}-\frac{R_c+R_L}{L} & -\frac{V_{in}}{rL}\\ \frac{V_{in}}{rC} & 0\end{bmatrix}\quad B_c = \begin{bmatrix}\frac{2r}{L}\\ -\frac{4 \cdot power}{CV_{in}}\end{bmatrix}\quad F_c = \begin{bmatrix}\frac{1}{L} & 0\\ 0 & -\frac{2}{C}\end{bmatrix}\quad x = \begin{bmatrix}\tilde{i}_L\\ \tilde{v}_C\end{bmatrix}\quad v = \begin{bmatrix}\widetilde{v_{in}}\\ \widetilde{i_{DC}}\end{bmatrix}\quad u = [\widetilde{d}]$$

Note that, A_c and B_c matrix could be exclusively defined by V_{in} and $power$. Once V_{in} and $power$ are selected, which represent the steady state, then A_c and B_c matrix are constant and a specific controller for this steady state could be designed. For each steady state point, an exclusive controller will

be assigned. This characteristics help extend the validity of the model and the range of application of Quasi-Z-Source inverter.

2.3 Digital Control System Design of Quasi-Z-Network

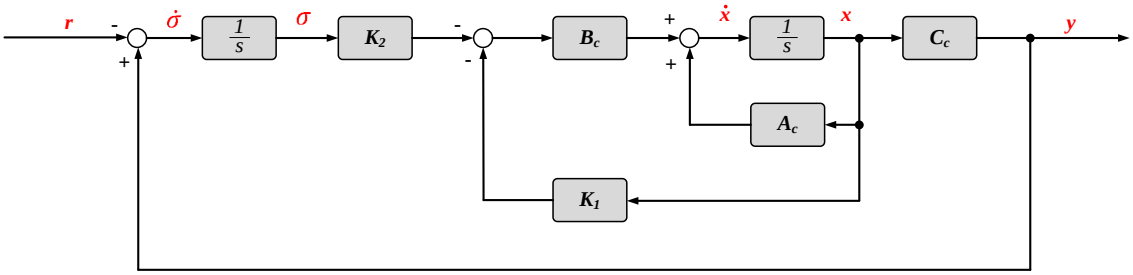


Figure 2. 6 Analog integral state feedback control design.

For analog control system, all the feedback signals are continuous. Figure 2.6 presents a typical integral state feedback control system. As one could see, all the system states and system output are measured continuously as feedback signal. System output will be compared with a reference, which is Quasi-Z-Network boost voltage reference in this thesis, and the error will be sent to an integrator. Each state is feed backed by a proportional gain. Thus, there is a PI controller built in. Applying this control method on Quasi-Z-Network model (2.32), will come out the following equations, and $\boldsymbol{d}$ is control input. [17]

$$\begin{cases} \dot{\boldsymbol{x}} = \boldsymbol{A_c x} + \boldsymbol{B_c u} \\ \dot{\boldsymbol{\sigma}} = \boldsymbol{y} - \boldsymbol{r} \\ \boldsymbol{y} = \boldsymbol{C_c x} \\ \boldsymbol{u} = -\boldsymbol{K_1} \cdot \boldsymbol{x} - \boldsymbol{K_2} \cdot \boldsymbol{\sigma} \end{cases} \tag{2.33}$$

where

$$\boldsymbol{A_c} = \begin{bmatrix} -\dfrac{\boldsymbol{R_c} + \boldsymbol{R_L}}{\boldsymbol{L}} & -\dfrac{\boldsymbol{V_{in}}}{\boldsymbol{rL}} \\ \dfrac{\boldsymbol{V_{in}}}{\boldsymbol{rC}} & \boldsymbol{0} \end{bmatrix} \boldsymbol{B_c} = \begin{bmatrix} \dfrac{\boldsymbol{2r}}{\boldsymbol{L}} \\ -\dfrac{\boldsymbol{4 \cdot power}}{\boldsymbol{CV_{in}}} \end{bmatrix} \boldsymbol{C_c} = \begin{bmatrix} \boldsymbol{0} \\ \boldsymbol{1} \end{bmatrix}^{\boldsymbol{T}}$$

$$\boldsymbol{x} = \begin{bmatrix} \tilde{\boldsymbol{\imath}}_{\boldsymbol{L}} \\ \tilde{\boldsymbol{v}}_{\boldsymbol{C}} \end{bmatrix} \quad \boldsymbol{u} = [\tilde{\boldsymbol{d}}] \quad \boldsymbol{K_1} = \begin{bmatrix} \boldsymbol{k_1} \\ \boldsymbol{k_2} \end{bmatrix} \quad \boldsymbol{K_2} = [\boldsymbol{k_3}] \quad \boldsymbol{r} = \boldsymbol{V_C}$$

Simplify (2.33) to state space array as follows

$$\begin{bmatrix}\dot{x}\\ \dot{\sigma}\end{bmatrix}=\begin{bmatrix}A_c & 0\\ C_c & 0\end{bmatrix}\cdot\begin{bmatrix}x\\ \sigma\end{bmatrix}+\begin{bmatrix}B_c\\ 0\end{bmatrix}u+\begin{bmatrix}0\\ -1\end{bmatrix}r \tag{2.34}$$

The above is the application of integral state feedback control. In state feedback control design, I will ignore $F_c v$, which usually be considered as disturbance. However, this control method will be applied inside a DSP. Thus, the entire feedback signal will be discrete and the modulation signal will be executed through a zero order hold by the inverter, as shown in Figure 2.7.

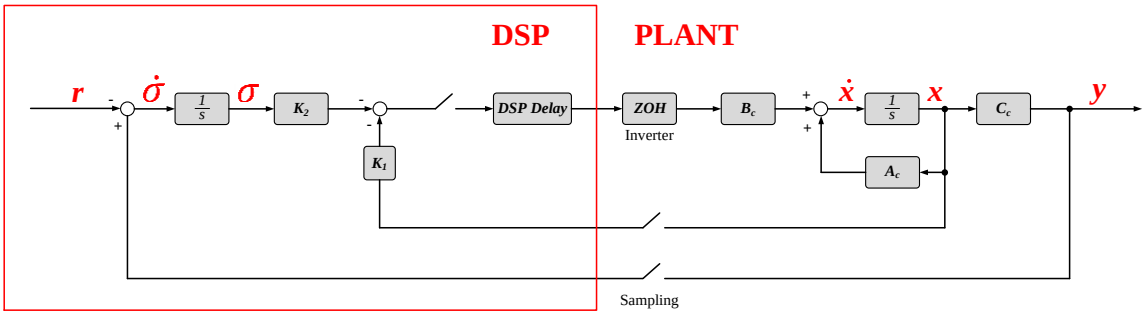


Figure 2. 7 Analog state feedback control system design.

This makes the controller to be designed in z domain necessary. The parameters which are used to design Quasi-Z-Network discrete controller are the following:

Table 2.1 Summarized parameters

f_s	DSP sampling frequency	*10kHz*
V_{in}	DC input Voltage	*100V*
L	Inductor of qZSI	*1.85mH*
R_L	Parasitic resistor of L	*24.63mΩ*
C	Capacitor of qZSI	*2440μF*
R_C	Buffer resistor	*2Ω*

Firstly, a discrete model of the Quasi-Z-Network will be developed. Figure 2.8 is the sampled data system. We need to transfer continuous system matrix to discrete matrix as presented in (2.35). [16]

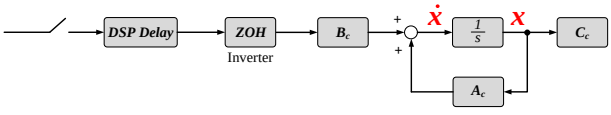


Figure 2. 8 Sampled data system of Quasi-Z-Network.

$$\begin{cases} \boldsymbol{A_d = \mathrm{I} + A_c T_s + \frac{A_c^2 T_s^2}{2} + \cdots} \\ \boldsymbol{B_d = (\mathrm{I} T_s + \frac{A_c T_s^2}{2!} + \frac{A_c^2 T_s^3}{3!} + \cdots) B_c} \\ \boldsymbol{C_d = C_c} \end{cases} \tag{2.35}$$

Using $\boldsymbol{A_d}$, $\boldsymbol{B_d}$ and $\boldsymbol{C_d}$ build a new discrete model as follows, utilizing bilinear transformation to achieve the integrator in DSP. And the newly build block diagram is shown in Figure 2.9.

$$\begin{cases} \boldsymbol{x_{k+1} = A_d \cdot x_k + B_d \cdot u_k} \\ \boldsymbol{V_{k+1} = V_k + \frac{T_s}{2}(E_k + E_{k+1})} \\ \boldsymbol{Y_k = C_d \cdot x_k} \\ \boldsymbol{u_k = -K_1 \cdot x_k - K_2 \cdot v_k} \end{cases} \tag{2.36}$$

where

$$\boldsymbol{A_d = \begin{bmatrix} 0.891 & -0.034 \\ 0.0258 & 0.9995 \end{bmatrix} \qquad B_d = \begin{bmatrix} 15.31 \\ 0.137 \end{bmatrix}}$$

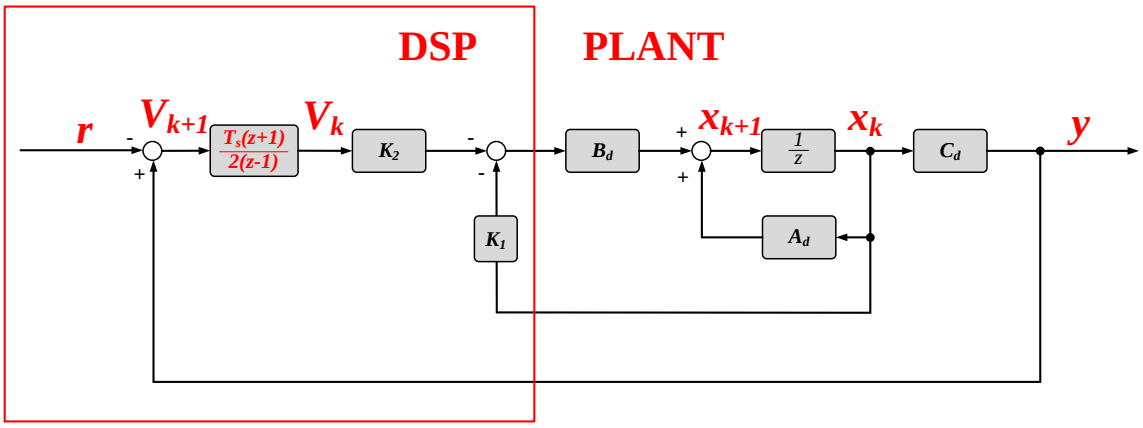


Figure 2. 9 Sampled data system of Quasi-Z-Network.

Rewriting (2.36)

$$\boldsymbol{V_{k+1} = V_k + \frac{T_s}{2}(E_k + E_{k+1})}$$

$$\boldsymbol{= V_k + \frac{T_s}{2}(Y_k - r + Y_{k+1} - r)}$$

$$\boldsymbol{= V_k + \frac{T_s}{2}(Y_k + Y_{k+1}) - T_s r} \tag{2.37}$$

because

$$\boldsymbol{Y_{k+1} = C_d \cdot x_{k+1}}$$

$$\boldsymbol{Y_{k+1} = C_d \cdot (A_d \cdot x_k + B_d \cdot u_k)}$$

$$\boldsymbol{Y_{k+1} = C_d A_d \cdot x_k + C_d B_d \cdot u_k} \tag{2.38}$$

Substitute (2.38) and (2.36) in (2.37)

$$\boldsymbol{V_{k+1} = V_k + \frac{T_s}{2}(C_d \cdot x_k + C_d A_d \cdot x_k + C_d B_d \cdot u_k) - T_s r}$$

$$\boldsymbol{V_{k+1} = \frac{T_s}{2}(C_d + C_d A_d) \cdot x_k + V_k + \frac{T_s}{2} C_d B_d \cdot u_k - T_s \cdot r} \tag{2.39}$$

Combine (2.37) and (2.36)

$$\begin{cases} \boldsymbol{x_{k+1} = A_d \cdot x_k + B_d \cdot u_k} \\ \boldsymbol{V_{k+1} = \frac{T}{2}(C_d + C_d A_d) \cdot x_k + V_k + \frac{T}{2} C_d B_d \cdot u_k - T \cdot r} \end{cases} \tag{2.40}$$

Simplify (2.40)

$$\begin{bmatrix} \boldsymbol{x_{k+1}} \\ \boldsymbol{v_{k+1}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{A_d} & \boldsymbol{0} \\ \boldsymbol{\frac{T_s}{2}(C_d + C_d A_d)} & \boldsymbol{1} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{x_k} \\ \boldsymbol{v_k} \end{bmatrix} + \begin{bmatrix} \boldsymbol{B_d} \\ \boldsymbol{\frac{T_s}{2} C_d B_d} \end{bmatrix} \cdot \boldsymbol{u_k} + \begin{bmatrix} \boldsymbol{0} \\ \boldsymbol{-T_s} \end{bmatrix} \cdot \boldsymbol{r} \tag{2.41}$$

$$\boldsymbol{\chi_{k+1}} = \mathbf{A} \cdot \boldsymbol{\chi_k} + \mathbf{B} \cdot \boldsymbol{u_k} + \mathbf{H} \cdot \mathbf{r} \tag{2.42}$$

where $\boldsymbol{u_k}$ is control input and

$$\mathbf{A} = \begin{bmatrix} \boldsymbol{A_d} & \boldsymbol{0} \\ \boldsymbol{\frac{T}{2}(C_d + C_d A_d)} & \boldsymbol{1} \end{bmatrix} = \begin{bmatrix} \boldsymbol{0.891} & \boldsymbol{-0.034} & \boldsymbol{0} \\ \boldsymbol{0.0258} & \boldsymbol{0.9995} & \boldsymbol{0} \\ \boldsymbol{0.00000129} & \boldsymbol{0.0000999763} & \boldsymbol{1} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} \boldsymbol{B_d} \\ \boldsymbol{\frac{T_s}{2} C_d B_d} \end{bmatrix} = \begin{bmatrix} \boldsymbol{15.318} \\ \boldsymbol{0.137} \\ \boldsymbol{0.00000685} \end{bmatrix} \qquad \mathbf{H} = \begin{bmatrix} \boldsymbol{0} \\ \boldsymbol{0} \\ \boldsymbol{-0.0001} \end{bmatrix}$$

Now we have the new discrete model. Based on this model, a new control input could be formed as follows:

$$\begin{cases} \boldsymbol{\chi_{k+1}} = \mathbf{A} \cdot \boldsymbol{\chi_k} + \mathbf{B} \cdot \boldsymbol{u_k} + \mathbf{H} \cdot \mathbf{r} \\ \boldsymbol{Y_k} = \mathbf{C} \cdot \boldsymbol{\chi_k} \\ \boldsymbol{u_k} = -\boldsymbol{K_1} \cdot \boldsymbol{x_k} - \boldsymbol{K_2} \cdot \boldsymbol{v_k} = -\mathbf{K} \cdot \boldsymbol{\chi_k} \end{cases} \tag{2.43}$$

Digitalize (2.43) in $\boldsymbol{z}$ domian to get the characteristics matrix:

$$z\boldsymbol{\chi}(z) = \mathbf{A}\boldsymbol{\chi}(z) - \mathbf{BK}\boldsymbol{\chi}(\mathbf{z}) + \mathbf{H}\boldsymbol{r}(z)$$

$$(z\boldsymbol{I} - \mathbf{A} + \mathbf{BK}) \cdot \boldsymbol{\chi}(z) = \mathbf{H} \cdot \boldsymbol{r}(z)$$

$$\boldsymbol{\chi}(z) = (z\boldsymbol{I} - \mathbf{A} + \mathbf{BK})^{-1} \cdot \mathbf{H} \cdot \boldsymbol{r}(z)$$

$$\boldsymbol{Y}(z) = \mathbf{C} \cdot (z\boldsymbol{I} - \mathbf{A} + \mathbf{BK})^{-1} \cdot \mathbf{H} \cdot \boldsymbol{r}(s)$$

$$\frac{\boldsymbol{Y}(z)}{\boldsymbol{r}(z)} = \mathbf{C} \cdot (z\boldsymbol{I} - \mathbf{A} + \mathbf{BK})^{-1} \cdot \mathbf{H} \tag{2.44}$$

Equation (2.44) is the DC network feedback control system transfer function. Because of the high time constant of Quasi-Z-Network, the pole selection for the state feedback system should be very close to the complex axis, in order not to pass the physical limitation of Quasi-Z-Network. The following is the derivation of transferring $\boldsymbol{s}$ domain poles to $\boldsymbol{z}$ domain poles.

$$\boldsymbol{G_{ref}}(\boldsymbol{s}) = (\boldsymbol{s} - \boldsymbol{s_1})(\boldsymbol{s} - \boldsymbol{s_2})(\boldsymbol{s} - \boldsymbol{s_3}) = (\boldsymbol{s} - \boldsymbol{P})(\boldsymbol{s^2} + \mathbf{2}\boldsymbol{\xi}\boldsymbol{\omega_n}\boldsymbol{s} + \boldsymbol{\omega_n^2}) \tag{2.45}$$

$$\begin{cases} \boldsymbol{s_1} = \boldsymbol{P} \\ \boldsymbol{s_2} = -\boldsymbol{\xi}\boldsymbol{\omega_n} + \boldsymbol{\omega_n}\sqrt{\boldsymbol{\xi^2} - \mathbf{1}} \\ \boldsymbol{s_3} = -\boldsymbol{\xi}\boldsymbol{\omega_n} - \boldsymbol{\omega_n}\sqrt{\boldsymbol{\xi^2} - \mathbf{1}} \end{cases} \tag{2.46}$$

$$\begin{cases} \boldsymbol{z_1} = \boldsymbol{e}^{\boldsymbol{s_1}\boldsymbol{T_s}} \\ \boldsymbol{z_2} = \boldsymbol{e}^{\boldsymbol{s_2}\boldsymbol{T_s}} \\ \boldsymbol{z_3} = \boldsymbol{e}^{\boldsymbol{s_3}\boldsymbol{T_s}} \end{cases} \tag{2.47}$$

The $\boldsymbol{s}$ domain poles could be determined by $\boldsymbol{e} = \mathbf{2}, \boldsymbol{\omega_n} = \mathbf{40}, \boldsymbol{P} = -\mathbf{1000}$. The desire transfer is shown as below

$$\boldsymbol{G_{ref}}(\boldsymbol{z}) = (\boldsymbol{z} - \boldsymbol{z_1})(\boldsymbol{z} - \boldsymbol{z_2})(\boldsymbol{z} - \boldsymbol{z_3}) = \mathbf{det}(\boldsymbol{sI} - \mathbf{A} + \mathbf{BK}) \tag{2.48}$$

Then the final gain value could be calculated as :

$$\begin{cases} \boldsymbol{k_1} = \mathbf{9.31} \times \mathbf{10^{-5}} \\ \boldsymbol{k_2} = \mathbf{0.0014534} \\ \boldsymbol{k_3} = \mathbf{0.03682} \end{cases} \tag{2.49}$$

These gain values are calculated based on a certain pair value of $\boldsymbol{V_{in}}$ and $\boldsymbol{power}$. When both input voltage and load condition have changed, a new set of gain value could be calculated following above process from (2.31) to (2.49). For each working condition, there is a specific gain value for it, as described in Table 2.2. In this way, the gain scheduling integral control method could control a wide

range of Quasi-Z-Network working condition.

Table 2.2 Working conditions

	$power_1$	$power_2$	⋯	$power_n$
V_{in_1}	$[k_1 \quad k_2 \quad k_3]_{(V_{in_1}, power_1)}$	$[k_1 \quad k_2 \quad k_3]_{(V_{in_1}, power_2)}$		$[k_1 \quad k_2 \quad k_3]_{(V_{in_1}, power_n)}$
V_{in_2}	$[k_1 \quad k_2 \quad k_3]_{(V_{in_2}, power_1)}$	$[k_1 \quad k_2 \quad k_3]_{(V_{in_2}, power_2)}$		$[k_1 \quad k_2 \quad k_3]_{(V_{in_2}, power_n)}$
⋮			⋱	
V_{in_n}	$[k_1 \quad k_2 \quad k_3]_{(V_{in_n}, power_1)}$	$[k_1 \quad k_2 \quad k_3]_{(V_{in_n}, power_2)}$		$[k_1 \quad k_2 \quad k_3]_{(V_{in_n}, power_n)}$

2.4 Digital Control System Design for Single-Phase Inverter

This part will discuss about single phase inverter control fit for DSP application. Many analysis and design techniques for continues-time LTI systems, such as the Routh-Hurwitz criterion and bode techniques, are based on the property that in the s-plane the stability boundary is the imaginary axis. Thus these techniques cannot be applied to LTI systems in the z-plane since the stability boundary is the unit circle. However, through the use of the bilinear transformation [16]

$$z = \frac{1+(T/2)w}{1-(T/2)w} \tag{2.50}$$

Or solving for w

$$w = \frac{2}{T}\frac{z-1}{z+1} \tag{2.51}$$

The unit circle of the z–plane transforms into the imaginary axis of the w-plane. This can be seen through the following development. On the unit circle in the z-plane, $z = \varepsilon^{j\omega T}$ and

$$w = \frac{2}{T}\frac{z-1}{z+1}\Big|_{z=\varepsilon^{j\omega T}} = \frac{2}{T}\frac{\varepsilon^{j\omega T}-1}{\varepsilon^{j\omega T}+1} = \frac{2}{T}\frac{\varepsilon^{j\omega T/2}-\varepsilon^{-j\omega T/2}}{\varepsilon^{j\omega T/2}+\varepsilon^{-j\omega T/2}} = j\frac{2}{T}tan\frac{\omega T}{2} \tag{2.52}$$

Thus it is seen that the unit circle of z-plane transforms into the imaginary axis of the w-plane. It is noted that the stable region of w-plane is the left half-plane. [16]

Let $j\omega_w$ be the imaginary part of w. We will refer to ω_w as the w-plane frequency. Then (2.51) can be expressed as

$$\omega_w = \frac{2}{T} tan \frac{\omega T}{2} \tag{2.53}$$

and this expression gives the relationship between frequencies in the s-plane and frequencies in the w-plane.

For small values of real frequency (s-plane frequency) such that ωT is small, (2.53) becomes

$$\omega_w = \frac{2}{T} tan \frac{\omega T}{2} \approx \frac{2}{T} \frac{\omega T}{2} = \omega \tag{2.54}$$

Thus the w–plane frequency is approximately equal to the s-plane frequency for this case. The approximation is valid for those values of frequency for which $\tan(\omega T/2) \cong \omega T/2$. For

$$\frac{\omega T}{2} \leq \frac{\pi}{10} \qquad\qquad \omega \leq \frac{2\pi}{10T} = \frac{\omega_s}{10} \tag{2.55}$$

the error in this approximation is less than 4 percent. Because of the phase lag introduced by the zero-order hold, we usually choose the sample period T such that (2.55) is satisfied over most of the system bandwith. At $\omega = \omega_s/10$, the zero-order hold introduces a phase lag of 18°, which is an appreciable amount and can greatly affect system stability. Therefore, the best crossover frequency is $\frac{\omega_s}{10}$. [16]

Figure 2.10 presents a typical dual-loop digital control block diagram for single-phase inverter output filter. The two blocks on right is the model of inverter filter. The red box on the left is the current controller and voltage controller which will be programed into DSP. There is a calculation delay in DSP (this delay will not be considered in the following controller design, details will be explained at the following chapter), and after each calculation cycle, the DSP will send the result to PWM black and hold for one cycle. This DSP model is shown in the middle red box of Figure 2.10. [16]

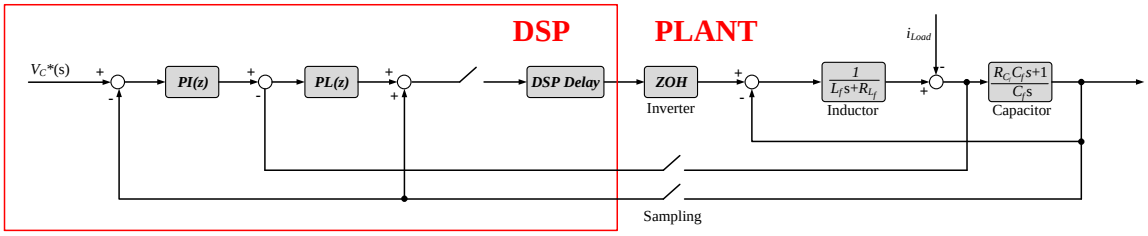


Figure 2. 10 DSP based dual-loop digital control system

In order for easy understanding of controller design process, I deleted the filter plant model feedback and feed forward signal inside DSP, only left a simplified dual-loop control system with sampling switch, Figure 2.11. The inner loop is current control loop. The outer loop is voltage control loop. We will go through current controller design first and then combine closed current control loop and capacitor block as voltage loop plant, voltage controller will be designed based on this combined plant. The design process will utilize direct control method. Firstly, transfer $\boldsymbol{s}$ domain transfer function into $\boldsymbol{z}$ domain with zero order hold and then use bilinear transformation to transfer $\boldsymbol{z}$ domain transfer function to $\boldsymbol{w}$ domain.

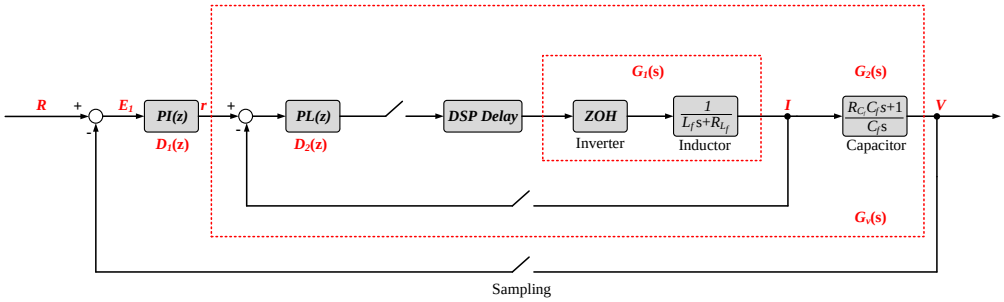


Figure 2. 11 Simplified DSP based dual-loop digital control system.

For DSP based digital control system, the plant could always be modeled as a sampling switch, zero order hold and plant transfer function as shown in Figure 2.11. Transfer function of zero order hold is shown in the figure. The inverter output filter parameters are summarized as in Table 2.2.

Table 2.3 Summarized parameters of inverter filter

$\boldsymbol{f_s}$	DSP sampling frequency	$\boldsymbol{10kHz}$
$\boldsymbol{L_f}$	Inductor of qZSI	$\boldsymbol{11.4mH}$
$\boldsymbol{R_{L_f}}$	Parasitic resistor of $\boldsymbol{L}$	$\boldsymbol{213.7m\Omega}$
$\boldsymbol{C_f}$	Capacitor of qZSI	$\boldsymbol{20\mu F}$
$\boldsymbol{R_{C_f}}$	Buffer resistor	$\boldsymbol{0.008\Omega}$

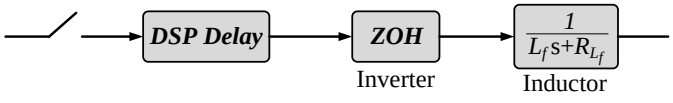


Figure 2. 12 Sample data system of inductor.

(2.56) is $\boldsymbol{s}$ domain current plant transfer function.

$$\boldsymbol{G_1(s) = \frac{1-\varepsilon^{-Ts}}{s} \cdot \frac{1}{L_f s + r_{Lf}}} \tag{2.56}$$

Check the $\boldsymbol{s}$ to $\boldsymbol{z}$ table to get the $\boldsymbol{z}$ domain transfer function as follows

$$\boldsymbol{G_1(z) = \mathbb{Z}\left[\frac{1-\varepsilon^{-Ts}}{s} \cdot \frac{1}{L_f s + r_{Lf}}\right] = \frac{0.008764}{z - 0.9981}} \tag{2.57}$$

Use bilinear transformation to achieve $\boldsymbol{w}$ domain transfer function as follow:

$$\boldsymbol{G_1(w) = \mathbb{Z}\left[\frac{1-\varepsilon^{-Ts}}{s} \cdot \frac{1}{L_f s + r_{Lf}}\right]_{z=\frac{1+\frac{T_s}{2}w}{1-\frac{T_s}{2}w}}} \tag{2.58}$$

Bode diagram of $\boldsymbol{G_1(w)}$ is shown in Figure 2.13

Since the sampling frequency is $\boldsymbol{10kHz}$, based on the discussion above, the crossover frequency for current loop should be $\boldsymbol{1kHz}$, noted as $\boldsymbol{f_{c-i} = 1kHz}$. From the bode diagram, Figure 2.13, at the crossover frequency the phase angle is $\boldsymbol{-108^\circ}$, compared with $\boldsymbol{-180^\circ}$ the phase margin is more than $\boldsymbol{45^\circ}$, thus there is no need to choose a controller to boost the phase of current plant. Considering the inner loop of control system should be as faster as possible, therefore I decide to use phase lag controller, which does not have an integrator built in. Phase lag controller has a form shown in (2.59). [16]

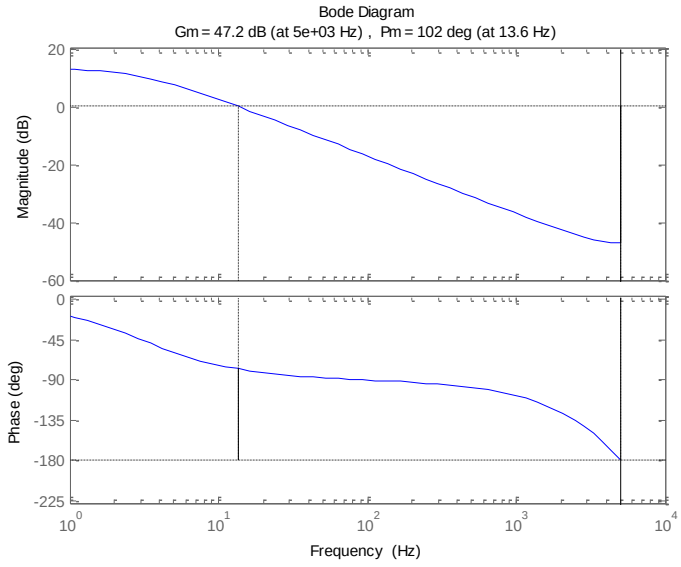


Figure 2. 13 Bode diagram of current plant.

The phase lag controller is presented in $\boldsymbol{w}$ domain in order to design it in $\boldsymbol{w}$ domain. Figure 2.14 is the bode diagram of phase lag controller. One could easily observe from bode diagram that phase lag controller has a flat magnitude at low bandwidth, which means it could magnify the fundamental frequency very well. [16]

$$\boldsymbol{D_2(w) = K\frac{1+\frac{w}{\omega_{w0}}}{1-\frac{w}{\omega_{wp}}}} \tag{2.59}$$

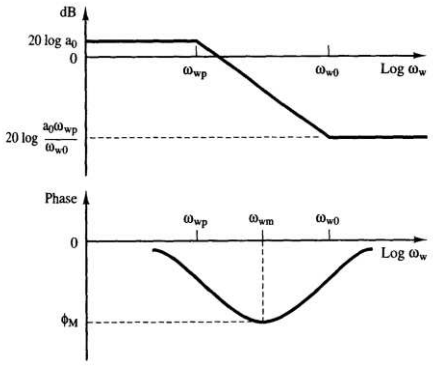


Figure 2. 14 Bode diagram of general phase lag controller.

The drawback is that it will introduce a big phase delay to the system. However, the current plant has big enough phase margin, thus this phase delay will not influence the system stability. Following is the phase lag controller design procedure:

1. Determine the crossover frequency, which is $\boldsymbol{f_{c-i} = 1kHz}$, $\boldsymbol{\omega_{c-i} = 2\pi f_{c-i} = 6283.2}$.
2. Choose $\boldsymbol{\omega_{w0} = \frac{\omega_{c-i}}{10}}$ to ensure that little phase lag is introduced at $\boldsymbol{\omega_{c-i}}$.
3. At $\boldsymbol{\omega_{c-i}}$, we want $\boldsymbol{|D_2(w)\cdot G_1(w)| = 1}$

Following these three rules, I derived out the following equations. [16]

$$\begin{cases} \boldsymbol{\omega_{w0} = \frac{\omega_{c-i}}{10}} \\ \boldsymbol{\tan^{-1}\frac{\omega_{c-i}}{\omega_{w0}} - \tan^{-1}\frac{\omega_{c-i}}{\omega_{wp}} = -1^{\circ}} \\ \boldsymbol{\left|K\frac{1+\frac{j\omega_{c-i}}{\omega_{w0}}}{1-\frac{\omega_{c-i}}{\omega_{wp}}}\right| = 10^{-|G_1(\omega_{c-i})|}} \end{cases} \Longrightarrow \begin{cases} \boldsymbol{K = 82.8} \\ \boldsymbol{\omega_{w0} = 628} \\ \boldsymbol{\omega_{wp} = 518} \end{cases} \tag{2.60}$$

Solving these equations, we could get the $\boldsymbol{w}$ domain phase lag controller and its bode diagram, Figure 2.15. and then transfer the controller from $\boldsymbol{w}$ domain to $\boldsymbol{z}$ domain using bilinear transformation (2.61).

Open loop bode diagram is shown in Figure 2.16.

$$\boldsymbol{D_2(z) = D_2(w)_{w=\frac{2}{T_S}\cdot\frac{z-1}{z+1}} = \frac{68.59z-64.42}{z-0.9495}} \tag{2.61}$$

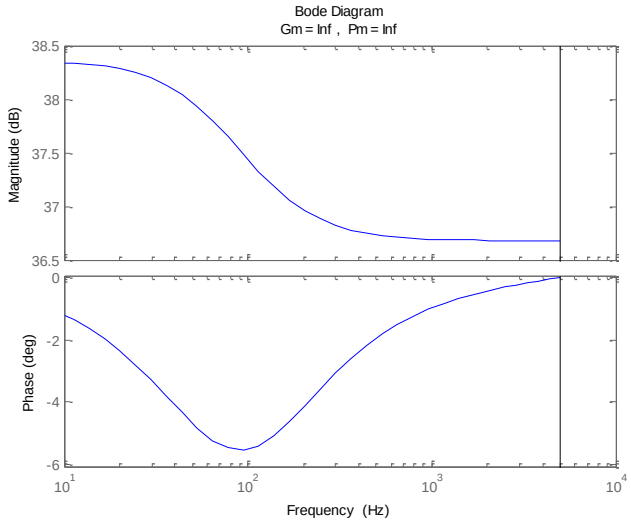


Figure 2. 15 Bode diagram of designed phase lag controller.

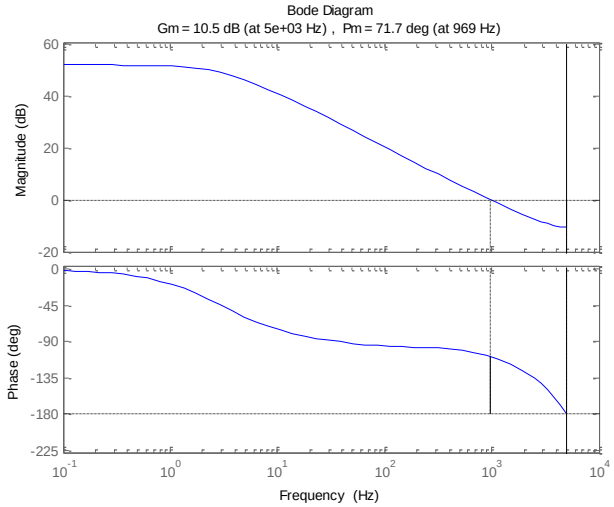


Figure 2. 16 Bode diagram of open current loop.

Figure 2.17 presents the closed loop bode diagram of current loop. As one could observe, the bandwidth of closed loop is 1kHz, which exactly same as the designed expectation. This current closed loop system transfer function will be considered in the controller design of voltage loop. Because this thesis mainly focus on discrete time domain controller design, thus the following paragraph will presents how to design voltage loop in discrete time domain.

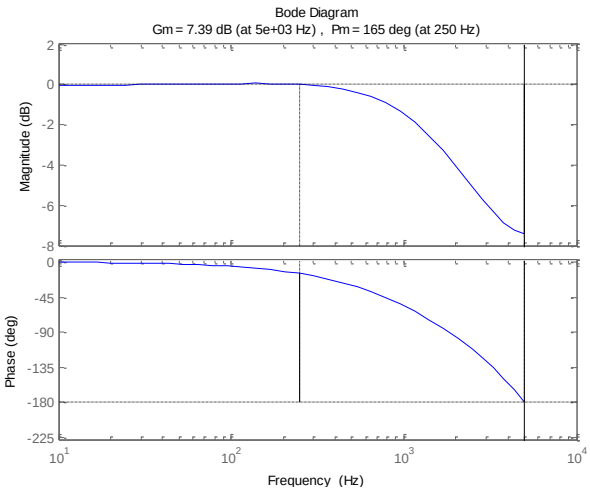


Figure 2. 17 Bode diagram of closed current loop.

Now I am going to discuss the voltage loop controller design. The determination of transfer function of voltage plant for sampled-data system is not the same as in $\boldsymbol{s}$ domain. A step-by-step procedure for finding voltage plant transfer function is explained as follows: [16]

1. Construct the original signal flow graph.
2. Assign a variable to each sampler input. Then the sampler output is this variable starred.
3. Considering each sampler output to be source node (input), express the sampler inputs and the system output in terms of each sampler output and input.

Figure 2.18 shows the block diagram of voltage plant. The purpose of this part is to find out $\boldsymbol{G_v(z)}$. Following the above procedure, I draw the original flow graph (Figure 2.19) based on Figure 2.18. [16]

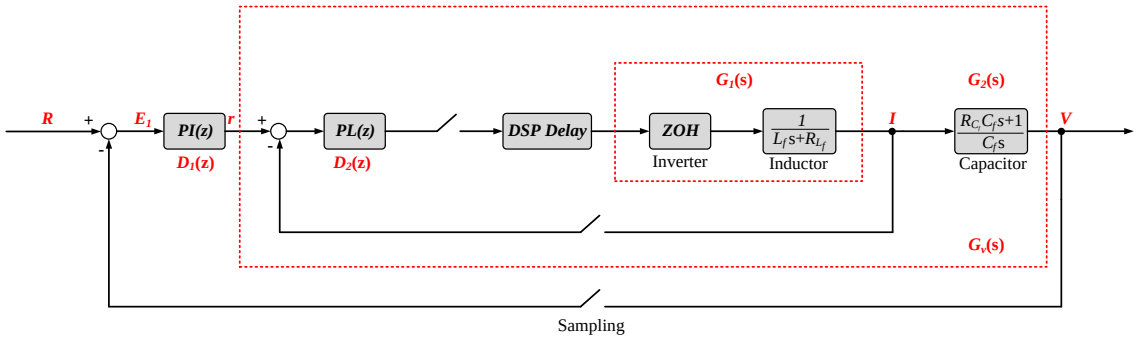


Figure 2. 18 Block diagram of voltage loop.

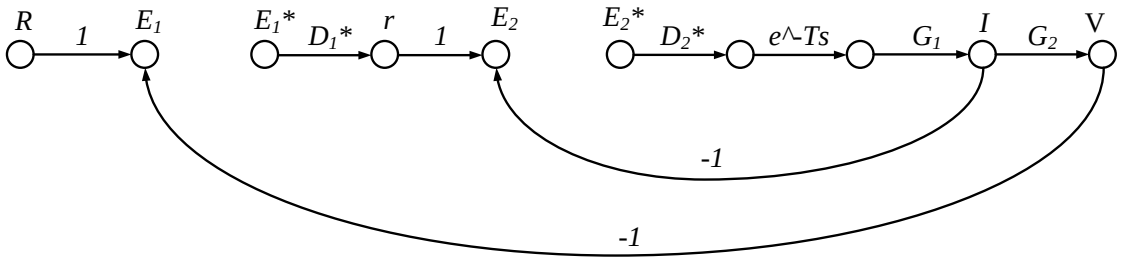


Figure 2. 19 Flow graph for control system.

Based on the Flow graph, we can write

$$\boldsymbol{E_2 = r - I}$$

$$\boldsymbol{V = E_2^* D_2^* G_1 G_2 e^{-Ts}}$$

$$\boldsymbol{I = E_2^* D_2^* G_1 e^{-Ts}}$$

Hence

$$\boldsymbol{r = E_2 + I = E_2 + E_2^* D_2^* G_1 e^{-Ts}}$$

Thus

$$\boldsymbol{r^* = E_2^* + E_2^* D_2^* G_1^* e^{-Ts}}$$

$$\boldsymbol{V^* = E_2^* D_2^* (G_1 G_2)^* e^{-Ts}}$$

Transfer to $\boldsymbol{z}$ domain

$$\boldsymbol{r(z) = E_2(z) + E_2(z) D_2(z) G_1(z) z^{-1}}$$

$$\boldsymbol{V(z) = E_2(z) D_2(z) G_1 G_2(z) z^{-1}}$$

Then we could get the $\boldsymbol{z}$ domain transfer function

$$\boldsymbol{G_v(z) = \frac{V(z)}{r(z)} = \frac{E_2(z) D_2(z) G_1 G_2(z) z^{-1}}{E_2(z) + E_2(z) D_2(z) G_1(z) z^{-1}} = \frac{D_2(z) G_1 G_2(z) z^{-1}}{1 + D_2(z) G_1(z) z^{-1}}} \quad (2.62)$$

At here, the DSP delay will be ignored, and discussed in the following chapter. Thus the final transfer function is (2.63).

$$\boldsymbol{G_v(z) = \frac{V(z)}{r(z)} = \frac{D_2(z) G_1 G_2(z)}{1 + D_2(z) G_1(z)}} \quad (2.63)$$

Observing (2.63), one could find out that the $\boldsymbol{z}$ domain transfer function of voltage plant is not the direct multiplication of current closed loop $\boldsymbol{z}$ domain transfer function and capacitor $\boldsymbol{z}$ domain transfer function. It is their $\boldsymbol{s}$ domain transfer function multiplication transferred to $\boldsymbol{z}$ domain as a whole, shown as follows.

$$\boldsymbol{G_1G_2(z)} = \mathbb{Z}\left[\frac{1-\varepsilon^{-Ts}}{s}\cdot\frac{1}{L_fs+r_{Lf}}\cdot\frac{R_{C_f}C_fs+1}{C_fs}\right] = \frac{0.02199z+0.02183}{z^2+1.998z+0.9981} \tag{2.64}$$

We have already known $\boldsymbol{D_2(z)}$ and $\boldsymbol{G_1(z)}$, $\boldsymbol{G_v(z)}$ could be easily find out. Following (2.65), we will have $\boldsymbol{G_v(w)}$. [16]

$$\boldsymbol{G_v(w)} = \boldsymbol{G_v(z)}\Big|_{z=\frac{1+\frac{T}{2}w}{1-\frac{T}{2}w}} \tag{2.65}$$

Bode diagram for $\boldsymbol{G_v(w)}$ is shown in Figure 2.20. For voltage loop, I will utilize PI controller to assure that AC output voltage will flow the reference voltage with little steady state error. Equation (2.66) presents the $\boldsymbol{w}$ domain PI controller format. For voltage control loop, the crossover frequency could be any value below $\boldsymbol{1kHz}$, here I choose $\boldsymbol{500Hz}$, because it is below one tenth of sampling frequency. [16]

$$\boldsymbol{D_1(w)} = \boldsymbol{K_I}\frac{1+\frac{w}{\omega_{w0}}}{w} \tag{2.66}$$

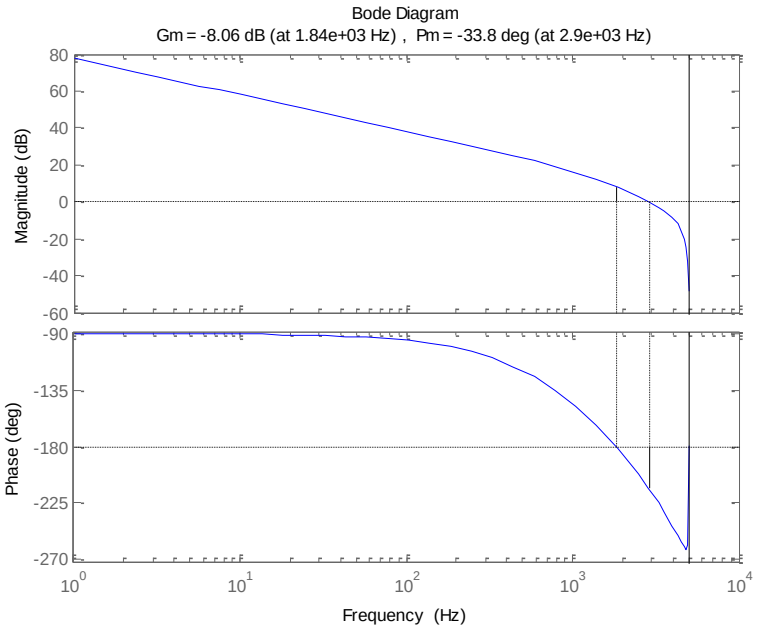


Figure 2. 20 Bode diagram of voltage plant.

Following is the PI controller design procedure: [16]

1. Determine the crossover frequency, which is $\boldsymbol{f_{c-v} = 500Hz}$, $\boldsymbol{\omega_{c-v} = 2\pi f_{c-v} = 628.32}$.

2. Choose $\boldsymbol{\omega_{w0} = 0.3 \cdot \omega_{c-v}}$ to ensure that little phase lag is introduced at $\boldsymbol{\omega_{c-v}}$.

3. At $\boldsymbol{\omega_{c-i}}$, we want $\boldsymbol{|D_1(w) \cdot G_v(w)| = 1}$

Following these three rules, I derived out the following equations.

$$\begin{cases} \omega_{w0} = 0.3 \cdot \omega_{c-v} \\ \left| K_I \frac{1+\frac{j\omega_{c-v}}{\omega_{w0}}}{j\omega_{c-v}} \right| = 10^{-|G_1(\omega_{c-v})|} \end{cases} \Longrightarrow \begin{cases} K_I = 58.86 \\ \omega_{w0} = 942.5 \end{cases} \tag{2.67}$$

Solving these equations, we could get the $\boldsymbol{w}$ domain PI controller and its bode diagram, Figure 2.21. and then transfer the controller from $\boldsymbol{w}$ domain to $\boldsymbol{z}$ domain using bilinear transformation (2.68). Open loop bode diagram is shown in Figure 2.22. The final closed loop bode diagram is shown is shown in Figure 2.23. [16]

$$\boldsymbol{D_1(z) = D_1(w)_{w=\frac{2\,z-1}{T_s z+1}} = \frac{0.0654z-0.05952}{z-1}} \tag{2.68}$$

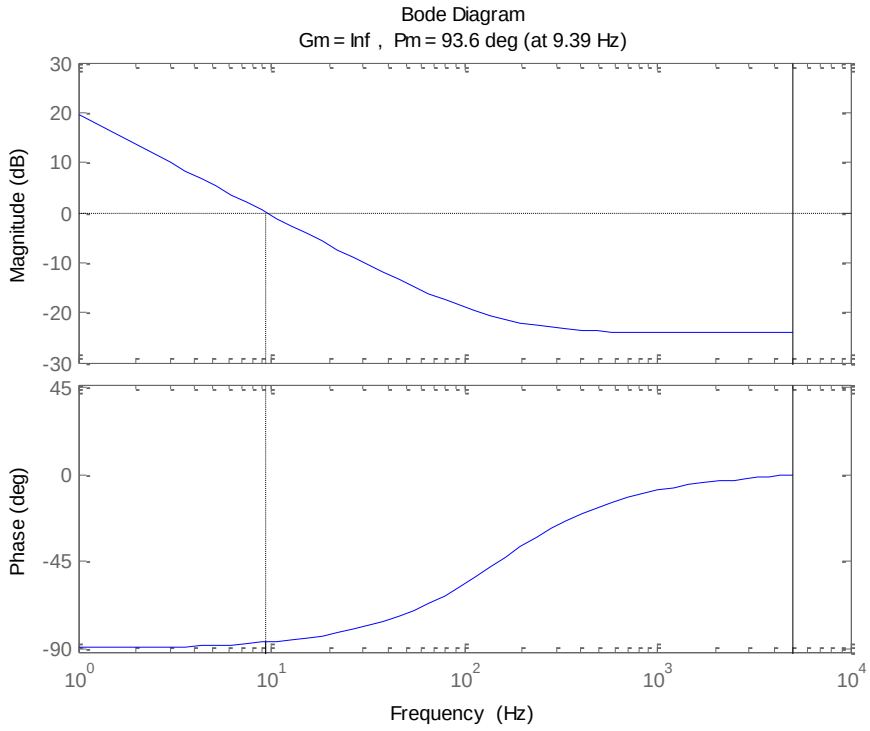


Figure 2. 21 Bode diagram of PI controller

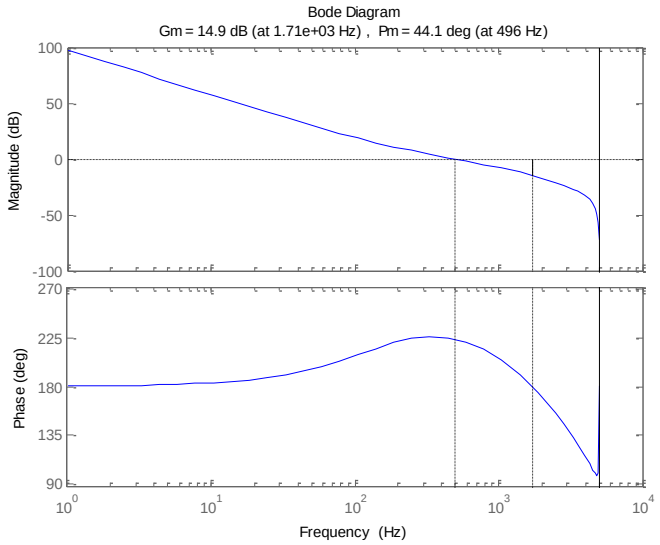


Figure 2. 22 Bode diagram of open voltage loop.

From Figure 2.23 we could observe that both the magnitude bode diagram and phase bode diagram is following the design expectation. For this whole inverter output voltage digital control system, the crossover frequency is $\mathbf{500}\boldsymbol{Hz}$, with phase lag controller work in the inner current loop and PI controller work at the outer voltage loop. Both controller was designed in $\boldsymbol{w}$ domain and then transferred to $\boldsymbol{z}$ domain using bilinear transformation method. These two controllers will to be programed into TMS320F28335-DSP.

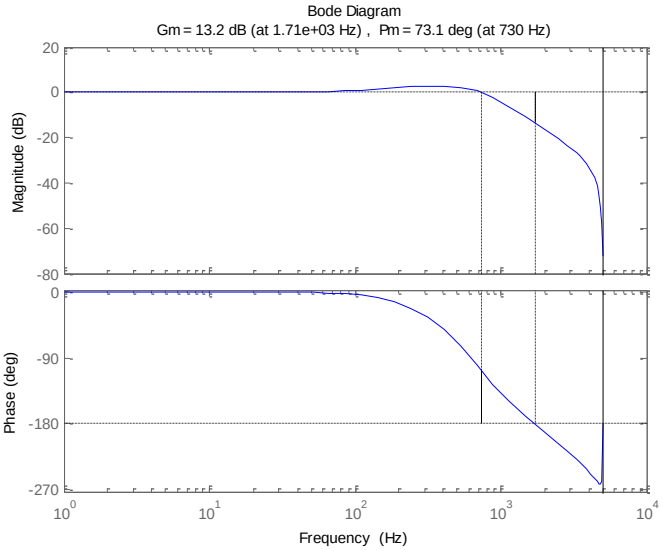


Figure 2. 23 Bode diagram of closed voltage loop.

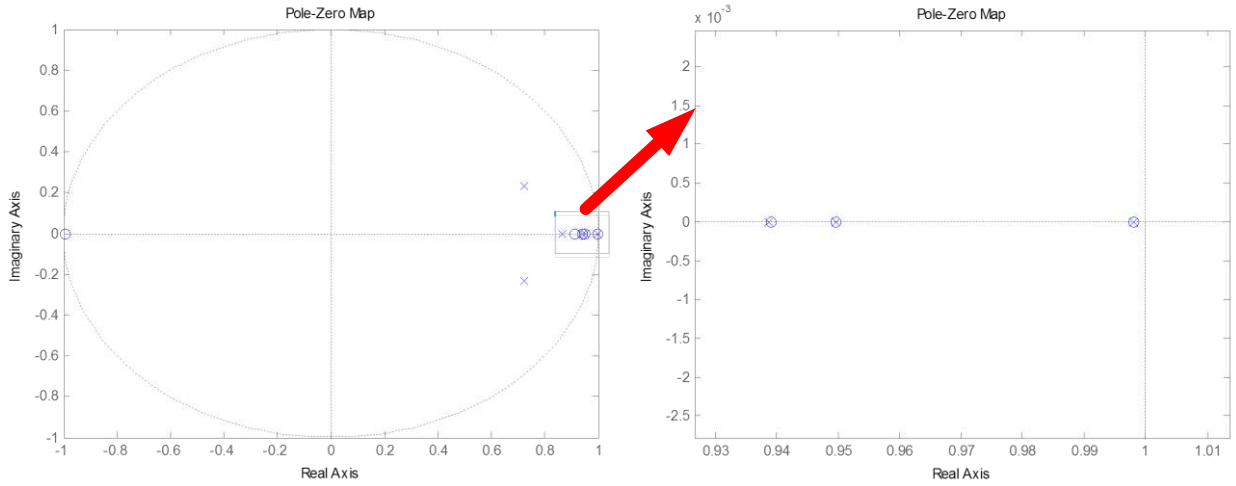


Figure 2. 24 Pole and zero map of closed voltage loop.

In order to make sure this final closed loop digital control system is stable, I draw a pole and zero map which is shown at Figure 2.24. From the figure, we could be sure that all the poles and zeros are in the unit circle of ***z*** domain. This means this control system is stable.

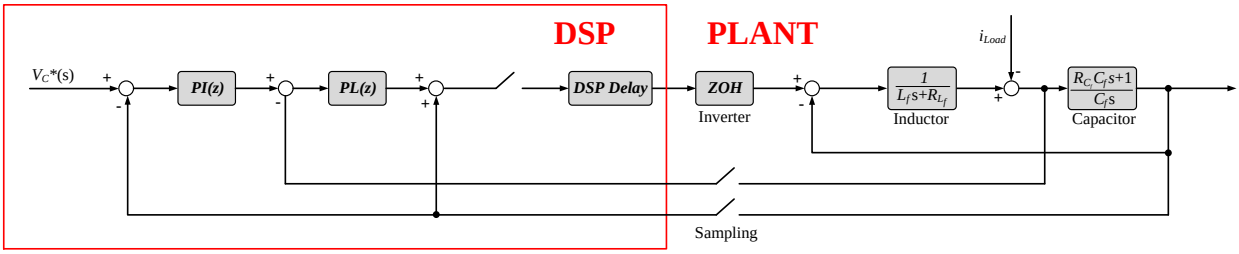


Figure 2. 25 Block diagram of dual-loop control system with feed fordward.

Finally, after finishing design current control and voltage control, we could put feed forward back to decouple the AC output voltage, as shown in Figure 2.25.

In this chapter, I have talked about my proposed Quasi-Z-Source network modeling method and its gain scheduling control method. For the inverter output voltage control, a robust digital control method was introduced in detail. The simulation result to demonstrate these control and modeling method will be provided in the following chapters.

CHAPTER 3

EXPERIMENTAL PROTOTYPE DEVELOPMENT

3.1 Objective

A hardware prototype was constructed based on TMS320F28335-DSP. The prototype was designed for a voltage input 100 VDC, with a nominal 150 VDC and 120 VAC output at 1 kW. The implemented control functions were: sampling analog feedback signals, implementing the dual-loop linear feedback control algorithms and gain scheduling state feedback control algorithms, performing circuit protection, and providing the switching signals to the GaN-FETs. Figure 3.1 is the whole hardware prototype. In this chapter, I will discuss elements selection, GaN-FET gate drive circuit design, signal conditioning circuit design, snubber circuit design, DSP programing and PCB design. For each circuit design, testing result was presented to confirm the validity of designed circuit.

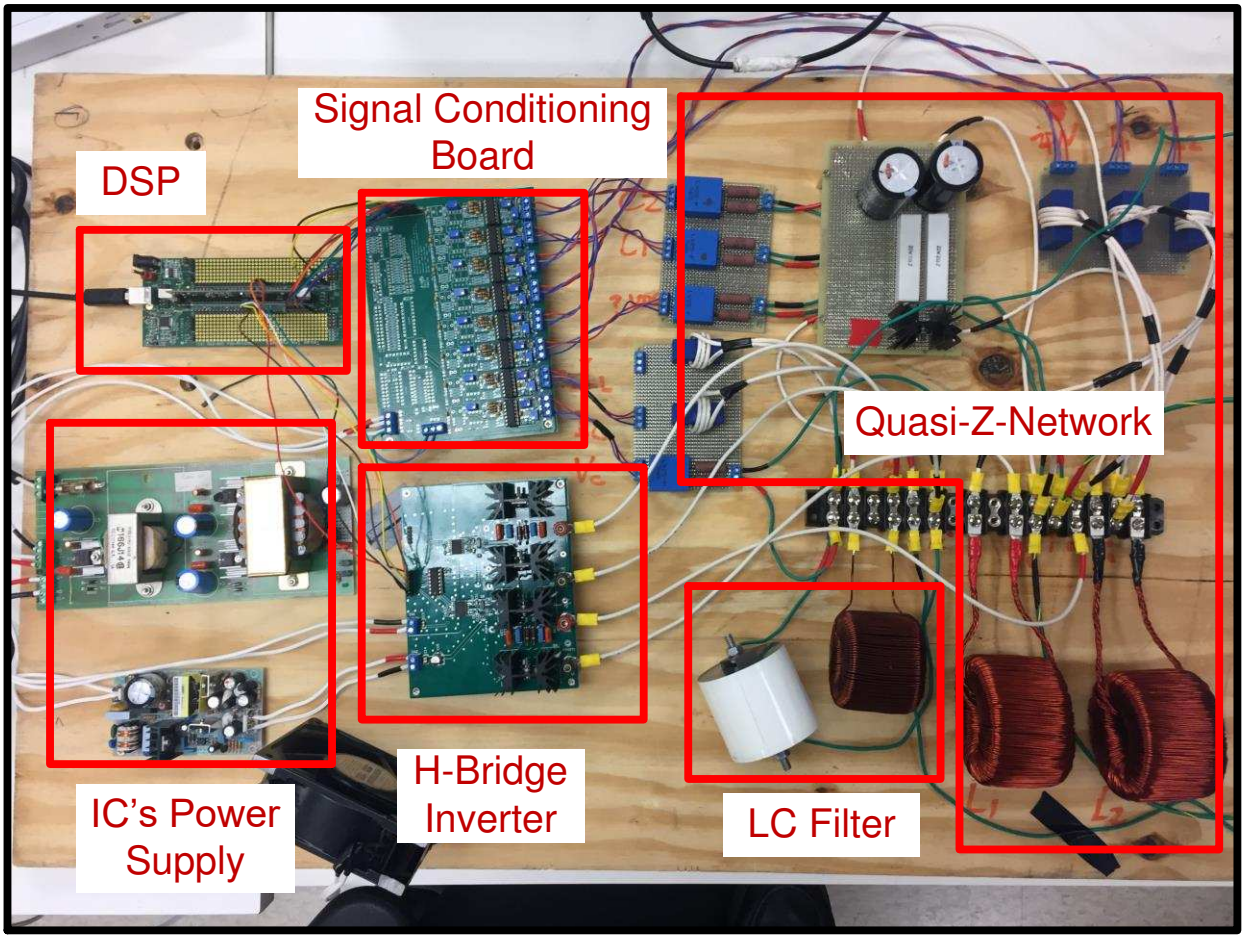


Figure 3. 1 Hardware prototype.

3.2 Switches Selection and GaN-FET Gate Drive Circuit Design

The power MOSFET utilized in Quasi-Z source inverter has two functions. It not only works as bridge inverter to transfer DC voltage to AC voltage, but also works as boost converter to boost DC voltage. This multi-function working mode gives the utilized power MOSFET a lot more stress, which includes enduring high drain to source voltage and conductive current, fast turn-on and turn-off speed. Choosing the right MOSFET is important for the normal operation of Q-ZSI.

I based on the worst switching condition during simulation, presented in figure 3.2, to choose the suitable power MOSFET.

The following figures present modulation waveform of QZ-Source Inverter. The upper and lower straight line is for DC boost network modulation signal, the sinusoidal waveform is for inverter output. In the adjacent area of peak point of sinusoidal waveform, the NULL state between active and shoot-through state is considerably short period for power MOSFET, which also add electrical stress on the MOSFET (Red circle area in each figure).

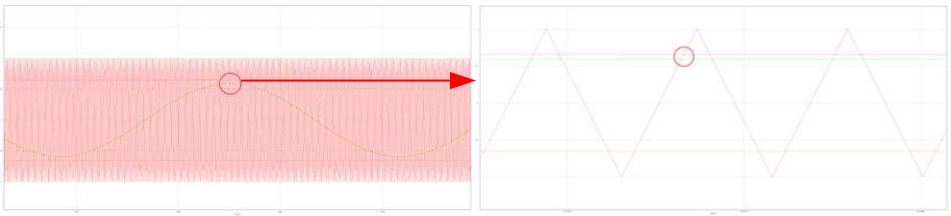


Figure 3. 2 Carrier waveform and modulation signal for inverter and DC boost network.

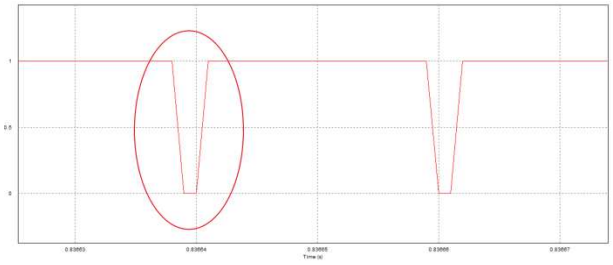


Figure 3. 3 Power MOSFET control signal at red circle area.

The control signal for power MOSFET of inverter at time of red circle area in Figure 3.2 is shown in Figure 3.3. The pulse width of this signal is considerably small as 0.68$\boldsymbol{us}$. During this time period, the power MOSFET should turn-on and turn-off once.

Gallium nitride, known as GaN, is the semiconductor industry's "hot" technology for defense and commercial applications. GaN devices have reached higher output power densities, wider bandwidths, and improved efficiencies. Recent improvements and new lower costs in GaN power semiconductor

technology are making possible high power continuous wave and pulsed amplifiers at microwave frequencies extremely attractive. It support very high operating voltages, roughly double the allowable current per unit FET gate width and provide exceptional performance for High Reliability Applications (such as those designed for Space). Based on this background, power GaN-FET, TPH3006PS, could fully satisfy my circuit's requirements. The following figure shows the GaN-FET schematic and product figure. [19]

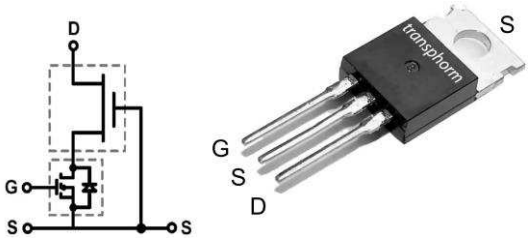
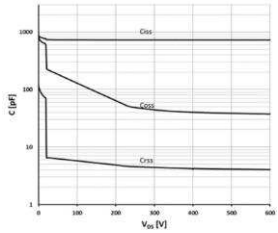


Figure 3. 4 TPH3006PS hardware picture.

It has ultra-low $\boldsymbol{Q_{gs} + Q_{gd}}$ gate charge and low $\boldsymbol{C_{rss}}$ capacitance value at high voltage, which is the charge of gate-to-source and gate-to-drain, could make the turn-on and turn-off delay time considerably short as $0.0178\,\boldsymbol{ns}$ if an effective driver circuit applied. Figure 3.4 presents the characteristics of TPH3006PS. [19]



Q_g	Total Gate Charge	-	6.2	9.3	nC
Q_{gs}	Gate-Source Charge	-	2.1	-	
Q_{gd}	Gate-Drain Charge	-	2.2	-	
$t_{d(on)}$	Turn-On Delay	-	4	-	ns
t_r	Rise Time	-	3	-	
$T_{d(off)}$	Turn-Off Delay	-	10.5	-	
t_f	Fall Time	-	3.5	-	

Figure 3. 5 Electrical characteristics and Capacitance characteristics of TPH3006PS.

GaN power HEMTs are nearly ideal switches for Quasi-Z-Source inverter applicaiton. A particular advantage in bridge circuits is that they can carry the freewheeling current without the need of an additional anti-parallel diode. In the traditional half bridge each switch is paired with a freewheeling diode. Because the HEMT channel exists in pure, undoped GaN, there is no parasitic p-n junction to provide an unwanted current path, and bidirectional flow of majority carriers can be realized in the channel. [19]

In Transphorm's cascade hybrid transistors the freewheeling current does indeed flow in the body diode of a silicon FET, but because it is a low voltage part, the injected charge is very small. Figure 3.6

indicates the current path for three modes of operation. In the reverse conducting mode the conduction loss may be reduced by enhancing the silicon FET (driving Vgs>Vth). As indicated in the figure, the voltage drop from source to drain decreases by about 0.8V with a 5A reverses current when the gate is enhanced. [19]

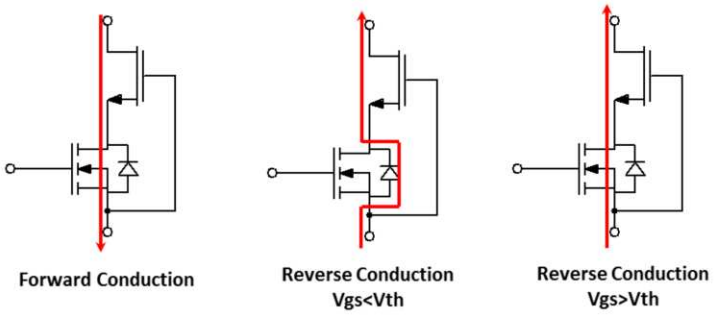


Figure 3. 6 Current paths in the cascade GaN switch for three operating modes.

3.3 GaN-FET Gate Drive Circuit Design

Based on the TPH3006PS technical file, a driver IC, SI8230, is utilized in an example application with TPH3006PS. However, SI8230 has a cross-conduction prevention module which could prevent the shoot-through state to happen. But when I search through the Si823X datasheet, I found out that they have a Si8232 driver IC, which has dual isolated drivers (HS/LS) inside without any overlap protection, shown as Figure 3.7.

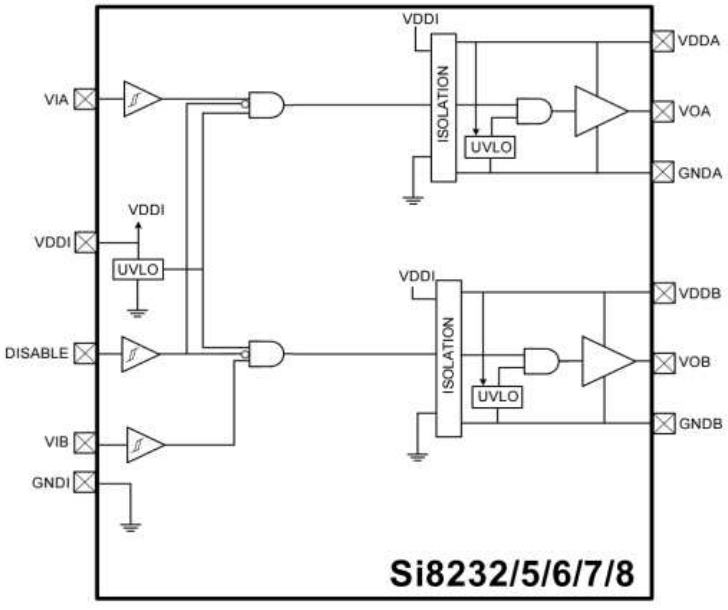


Figure 3. 7 Si8232/5/6/7/8 two input dual isolated drivers.

Thus, instead of four drivers to control four GaN-FETs, I utilized two of Si8232 to control four switches. Si8232 is not only a GaN-FET driver, it also has a built in 5 kVRMS input-to-output isolation that saves the use of another opt-coupler. Figure 3.8 is a typical connection of Si8232.

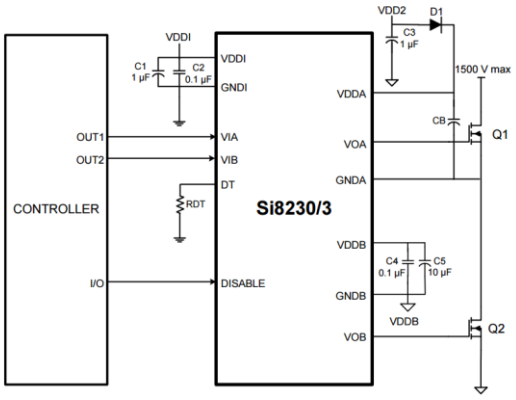


Figure 3. 8 Si8232 half-bridge application.

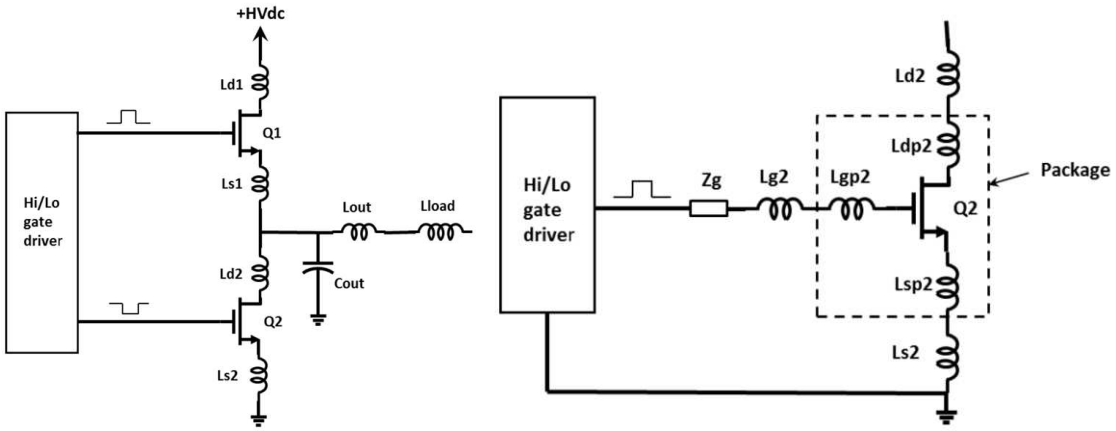


Figure 3. 9 Parasitic elements in the output loop and input loop.

Although the various gate charges are low with GaN-FET switches, they are not zero, and there will be a very fast transient current flowing during switching as these charges are changing. This current will flow from the positive supply DC source, through both transistors to the negative supply DC source. To minimize ringing voltage due to this switching transient, parasite inductors in this path should be minimized. Referring to Figure 3.9, these parasite inductors are noted as $\boldsymbol{L_{s1}}$, $\boldsymbol{L_{d1}}$, $\boldsymbol{L_{s2}}$, and $\boldsymbol{L_{d2}}$. To minimize these inductors, low impedance power and ground traces, or planes, should be utilized and bypass capacitor should be placed as close as possible to the transistors. The connection between the high-side switch (Q_1) source pin and the low-side switch (Q_2) drain pin should also be as short as possible. [19]

As with the output loop of gate drive circuit, minimizing inductance in the input, or gate-drive loop is important but hard. Particularly important is the source parasite inductor, which is common to both loops. Any voltage developed across this inductor due to a change in the output current, di_D/dt, will appear in the input loop. A low impedance layout will minimize this inductance, as previously discussed. However, the TO220 package unavoidably adds inductance in the source lead, as shown in Figure 3.9. This inductance cannot be further reduced, and so its impact must be recognized during gate drive design [19]

During the initial state of the turn-on transient, as the drain current rises from zero up to the value of the load current ($0 < i_D < i_{LOAD}$), the rate of change, di_D/dt, is determined by the gate current. There is no significant change in V_{ds} at this time, and therefore no displacement current caused by it included in i_D. A voltage $v_{L_s} = L_s \frac{di_D}{dt}$ develops across the source inductance which will subtract from the gate drive voltage v_{GS}. Slowing the di_D/dt speed by reducing i_G will reduce the corresponding voltage on the source inductance and also reduce excitation of any related parasitic resonance. Using a gate resistor in the place of Z_g in Figure 3.9 would effectively decrease i_G. A gate resistor will not, however, provide the additional function of limiting slew rate at the switching node: dv_{DS}/dt. This is because the feedback capacitance, $C_{rss} = C_{GD}$, of the cascade combination is low. The common method of limiting C_{rss} discharge with a gate resistor will not be effective since the dominant output capacitance (C_{DS}) is not discharged through the gate resistor. Simply choosing a gate driver with a lower output current is a better way to limit i_G and di_D/dt, Si8232 only provide 0.5A gate drive current. Once the drain current has risen to the level of the load current during turn-on of the GaN-FET switch ($i_D < i_{LOAD}$), a very fast dv_{DS}/dt transition occurs. Values in the range of $100V/ns$ are common. A transient displacement current through C_{DS} due to dv_{DS}/dt will flows into the parasitic source inductance, causing ringing voltage. This ringing voltage couples to the input circuit through C_{GS} of the transistor, and will tend to generate transient currents there. It is found that using a small SMD ferrite bead for Z_g effectively opposes such transient currents and inhibits coupling of the signal, although the voltage waveform on the gate pin is not obviously damped. In this driver circuit design, a ferrite bead with 120 ohms impedance at 100MHz was used in series with each gate of GaN-FET. The GaN-FET is fully on with about $+8V$, gate to source. Since Si8232 gate-drive chips have an under voltage protection threshold of $8V$, I choose to use $12V$ auxiliary supplies to avoid any trips. [19]

The bootstrap circuit for the high-side switch gate drive are composed of bootstrap diode, current limiting resistor and boot strap capacitor. The junction capacitance of diode will contribute to switching loss, and thus a fast, low capacitance diode should be utilized. Resistor is critical for limiting the inrush

charging current; a value of 10Ω works well. [19]

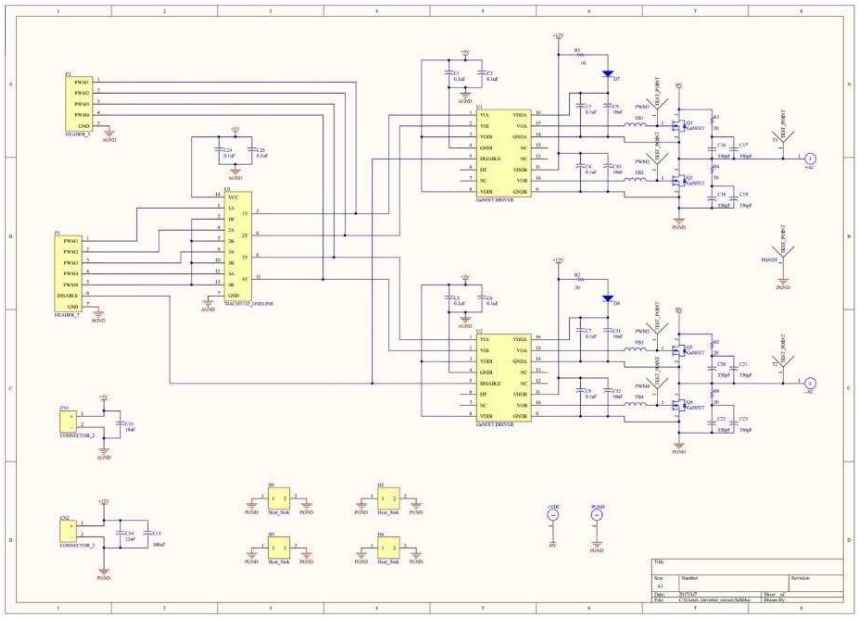


Figure 3. 10 Gate drive circuit for GaN-FET.

Figure 3.10 is the final gate drive circuit schematic and its PCB implementation, Figure 3.11. There is a OR gate before the Si8232 driver. This OR gate is used to introduce the shoot-through state to the Quasi-Z-Source inverter. Because the threshold for a high signal input of Si8232 is $2V$, which is TLL voltage level, we should chose a OR gate chip compatible with TTL voltage and able to provide enough current to drive two Si8232 drivers. SN74AHCT is a perfect fit in this condition.

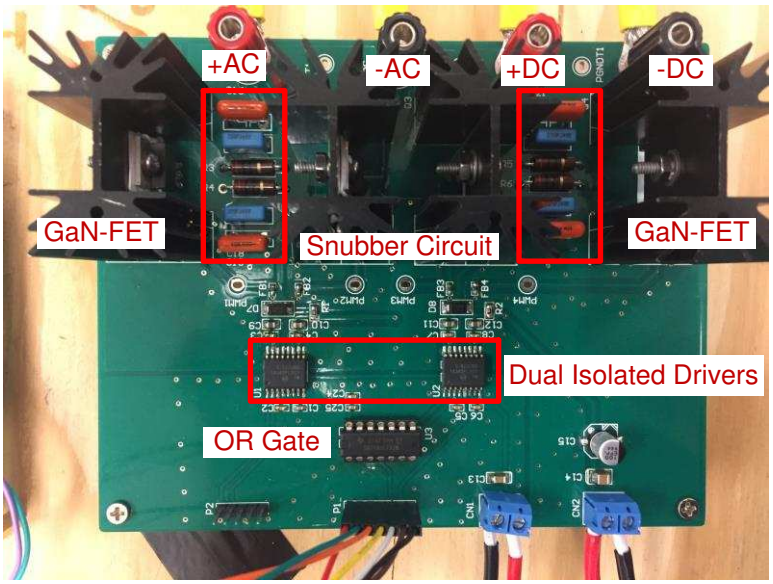


Figure 3. 11 PCB implementation of gate drive circuit.

3.4 Snubber Circuit Design

The purpose of the snubber is to minimize transients during switching operations. The snubber consisted of a capacitor and resistor connected in series across the transistors drain and source (for MOSFETS). Because they are designed to damp high frequency transients, the capacitors and resistors used must be tolerant of voltage and current transients. For this reason, PPE film capacitors and carbon composite resistors were used.

When I first test the circuit at a low input voltage (boost from 15V to 30V), there appeared a high voltage spikes on the GaN-FET switches, as shown in Figure 3.12. From the figure one could observe that voltage spikes are especially high when null state is very short. Even when null state is bigger, the voltage spikes could be as high as 60V

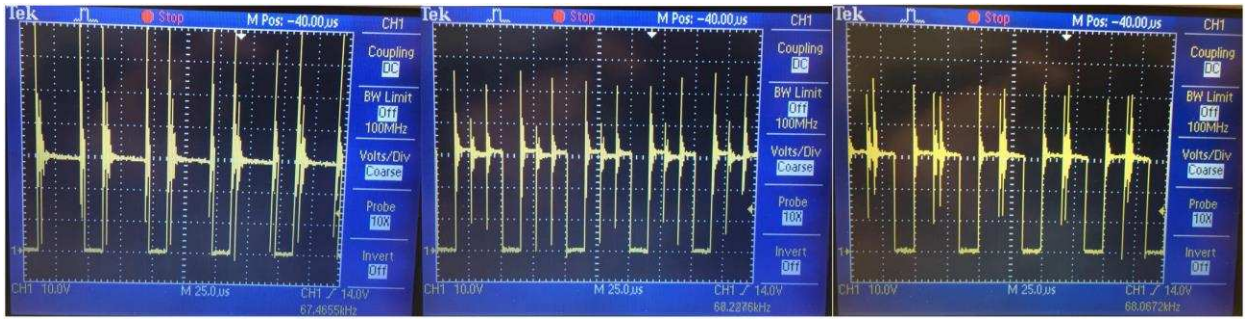


Figure 3. 12 Voltage spikes appeared on the GaN-FETs without snubber circuit.

The reason of this voltage spikes is that the long wire connecting to the capacitor. These long wires have a quit big parasitic inductor inside. Figure 3.13(a) is a simplified Quasi-Z-Source network with parasitic inductor.

During each state transition (shoot-through→null→active→null→shoot-through), the current inside parasitic inductor is either reversed or choked. This big di/dt will induce a high voltage applied on the GaN-FETs. To reduce this high induced voltage, minimize parasitic inductance is critical, which could only achieve by using PCB. Appling a RC snubber circuit is cost-effective. Based on the quick snubber design technique described in [30], capacitor value should be about twice the sum of the output capacitance of the MOSFET (C_{oss}) and the estimated mounting capacitance. GaN-FET has a C_{oss} about $133pF$ according to the manufacturer's data sheet. Mounting capacitance was estimated to be $40pF$. Therefore, snubber capacitor should be around $346pF$. Thus, a 330 pF PPE capacitor was selected and procured. The snubber resistor size was determined based on the drain to source voltage across the GaN-FET (V_{ds}), which is about 150 V, and i_D, which was determined to be around 7.5A. Thus, snubber resister

was calculated to be $\frac{150V}{7.5A} = 20\Omega$. In order to get the best value of snubber circuit, I tested this snubber value and two other capacitor values ($10nF$ *and* $1\mu F$) on a test circuit shown in Figure 3.13(b).

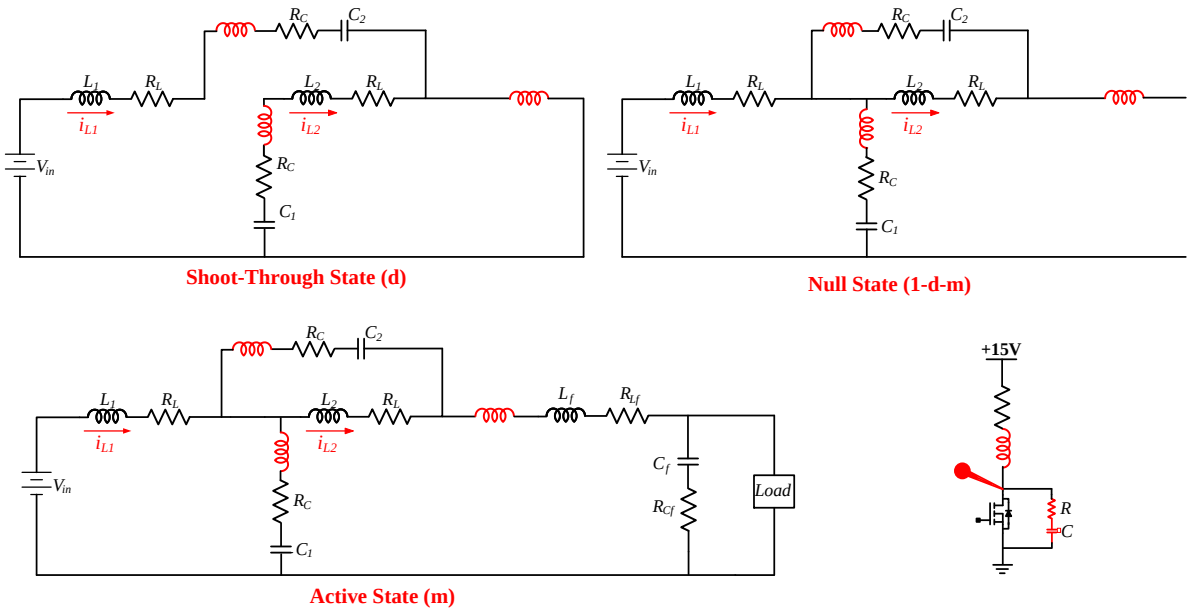


Figure 3. 13 Parasitic inductor on each state and testing circuit.

When the snubber circuit has not been mounted, the drain to source voltage v_{DS} is shown as in Figure 3.14. As one could find out, the ring voltage spike is high and converse to 15V after several cycles. The snubber circuit test result is shown in Figure 3.15. The test result for capacitor value of $330pF$ still has a big voltage spike. $1\mu F$ capacitor has present that it could slow down the rising of voltage which could affect the output voltage waveform. Thus, $10nF$ capacitor and 20Ω resistor value is the best fit snubber circuit.

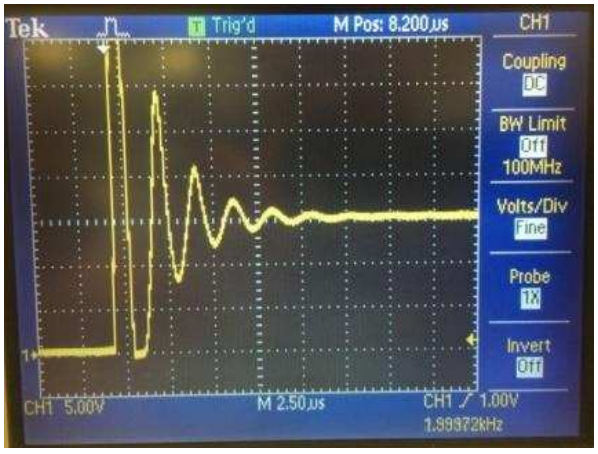


Figure 3. 14 Drain to source voltage without snubber circuit.

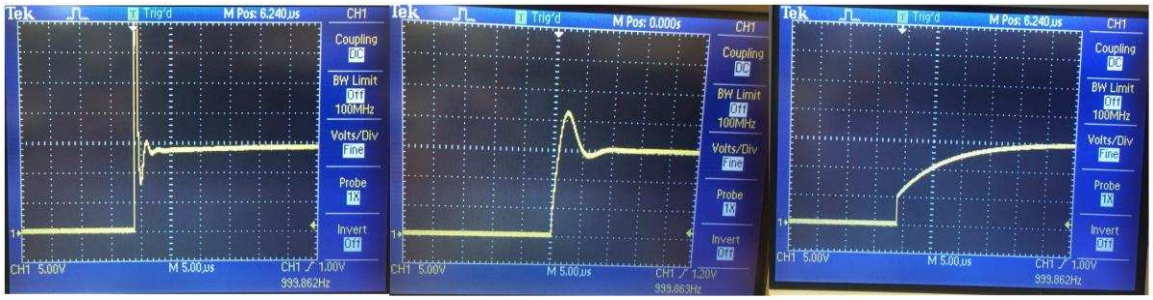


Figure 3. 15 Test result with capacitor value of (a)$330pF$ (b)$10nF$ (c)$1\mu F$.

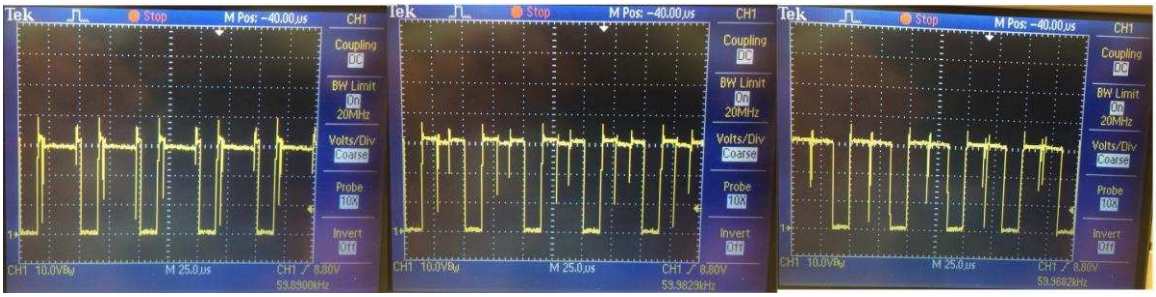


Figure 3. 16 GaN-FET drain to source voltage with snubber circuit.

After mounted the snubber on the H-Bridge PCB, the voltage spikes on the GaN-FET have been largely reduced as shown in Figure 3.16. With this snubber circuit, I dare to test the high voltage condition.

3.5 Signal Conditioning Circuit Design

Signal conditioning circuit is an important part for feedback control. The function of it is to sensor the voltage or current and then transfers it to signals which could fit for DSP-ADC block. Figure 3.17 is the circuit being used for my hardware. This circuit has three stages. First stage is a signal divider, which reduces the large voltage signal to a small value fit to DSP ADC input. Second stage is a buffer following with DC offset addition. Since DSP could only receive voltage signal of 0V-3V, a DC offset has to be added to the input signal to move it up above 0V. Third stage is a low pass filter to reduce the noise.

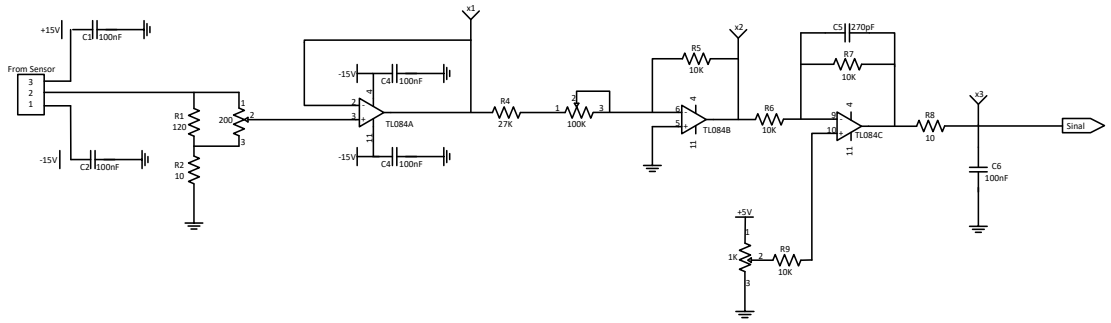


Figure 3. 17 Signal conditioning circuit schematic.

3.6 DSP Programing

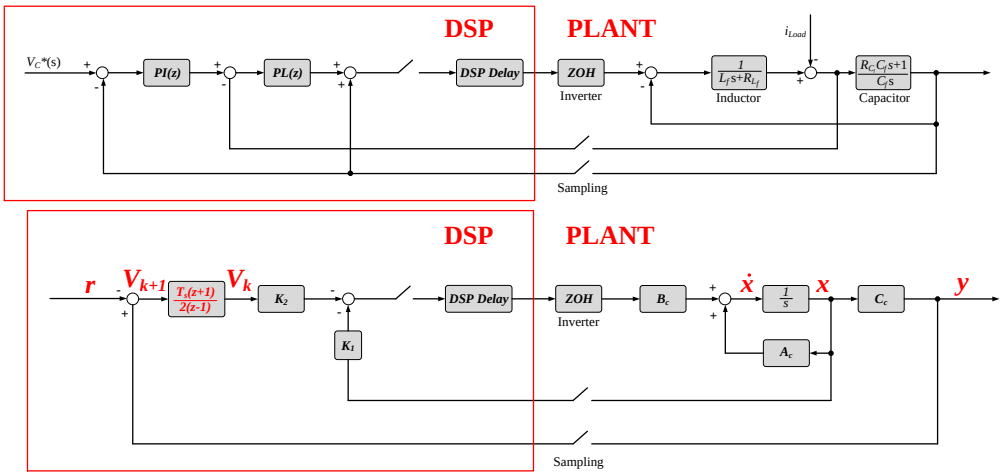


Figure 3. 18 Block diagram for qZSI and inverter control.

Figure 3.18 gives us a whole block diagram for qZSI and inverter control. The block in the red box should be calculated by DSP. For a TMS320F28335-DSP based digital control system, except calculation delay there is also a PWM cycle delay because of the counter compare submodule inside DSP. Figure 3.19 show us a counter compare submodule.

At the beginning of each PWM cycle, ADC will sample all the input signal, and then CPU will take the feedback signal go through all the controller to get the modulation signal which will be sent to the counter compare submodule (CMPA) of PWM block to compare with carrier in order to generate the PWM gate drive signal. However, counter compare submodule does not take the calculation result right away. To keep the stability, counter compare submodule will load the controller output value at the end of each PWM cycle and then generate PWM signal based on this controller output. This process is explained at Figure 3.20(a).

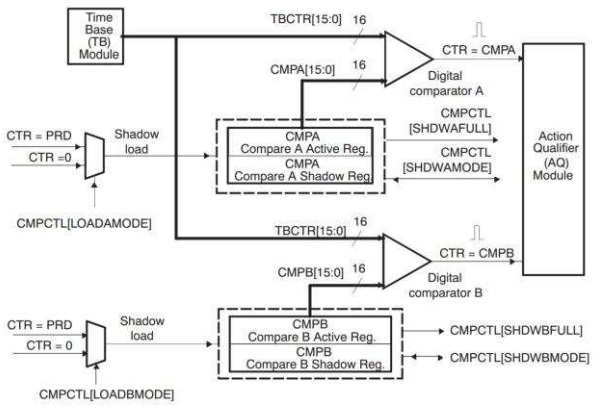


Figure 3. 19 Counter compare submodule inside DSP.

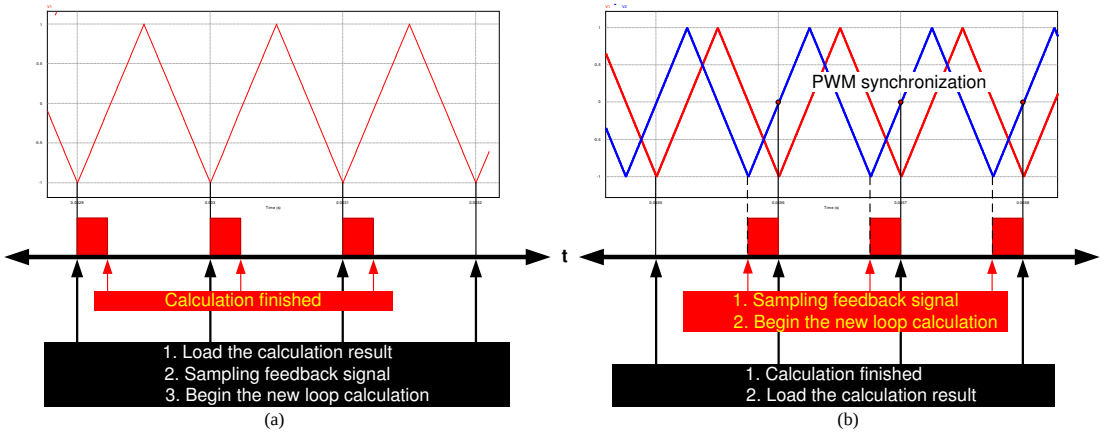


Figure 3. 20 Programming method to compensate for delay inside DSP.

However, one PWM cycle delay is a disaster for control system. Any *s* domain designed controller will not be functional with this delay. That's the reason why *z* domain designed controller is highly recommended.

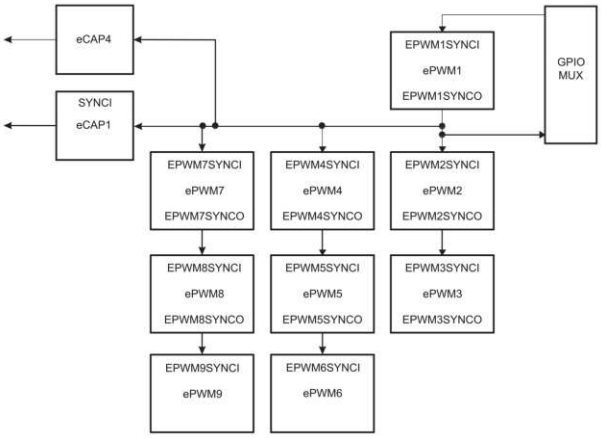


Figure 3. 21 Configuration of PWM block synchronization system in DSP.

In order to further improve the stability of control system, we have to figure out a way to compensate this delay. Most papers use smith estimator to solve this problem. However, this will increase the calculation time and make the control system more complicated. The other method utilized by researchers is to apply a dual core DSP, which has built in loop control module, designed specifically for closed loop control system. But my DSP do not have a built in loop control. I relied on the real time control optimization method to compensate this delay. Instead of sampling feedback signal at the beginning of each PWM cycle, one could program to sample the feedback signal in the middle PWM cycle, as explained at Figure 3.20(b). The application of this process needs another PWM module to begin

an interrupt function to sample the input signal and begin controller calculation. However this PWM waveform needs to be synchronized with main PWM waveform. Figure 3.21 explained the synchronization configuration. When the main PWM module counts down to zero, it will send out a synchronization signal to the next PWM module, once receive this signal, the following PWM module will load the saved phase data and count up from that phase number.

This chapter has introduced GaN-FET characteristics and its gate drive circuit; snubber circuit design was confirmed by a low voltage circuit test; DSP programing to compensate the counter compare submodule delay. Next chapter will present the hardware prototype test result and simulation result as a comparison.

CHAPTER 4

EXPERIMENTAL TESTING AND RESULTS

4.1 Objective

Experimental testing of the hardware prototype that was described in Chapter 3 was conducted to verify correct operation and validate the control algorithms that were described in Chapter2. First, open loop operation was conducted to verify the correct operation of the gating signals, gate drivers, and power stage. Next, the whole control algorithm was demonstrated on the hardware. After that, the DC input voltage was increased to test stability of control system. All testing was conducted under low power conditions (50W). This was due to the fact that there was not a suitable high power load bank capable.

4.2 Hardware Testing and Results

Firstly, the hardware prototype was tested under the following conditions and reference

$$\begin{cases} V_{in} = 100V \\ r = 150V \\ V_{AC-ref} = 120V_{peak} \\ R_{Load} = 150\Omega \end{cases} \tag{4.1}$$

and the testing result was shown at Figure 4.1. The qZSI network output voltage was exactly at 150V and the AC output voltage was purely sinusoidal, which confirmed the controller's function.

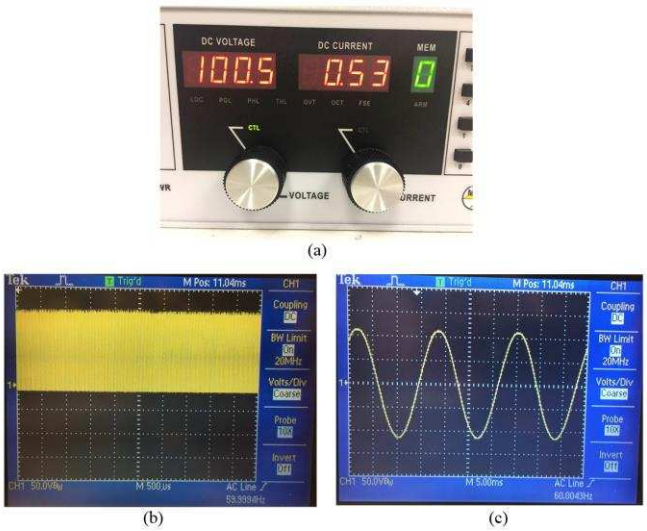
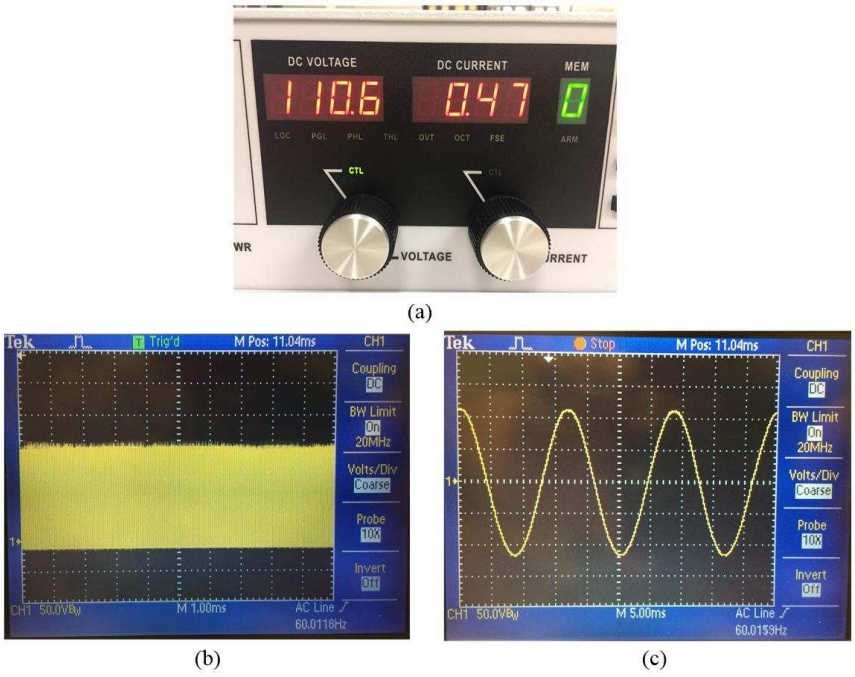


Figure 4. 1 qZSI working at 100V, 50W (a) DC input voltage (b) Quasi-Z-Source network output voltage (c) Quasi-Z-Source inverter output AC voltage.

Secondly, the input DC voltage was increased from 100V to 110V to test the DC network gain

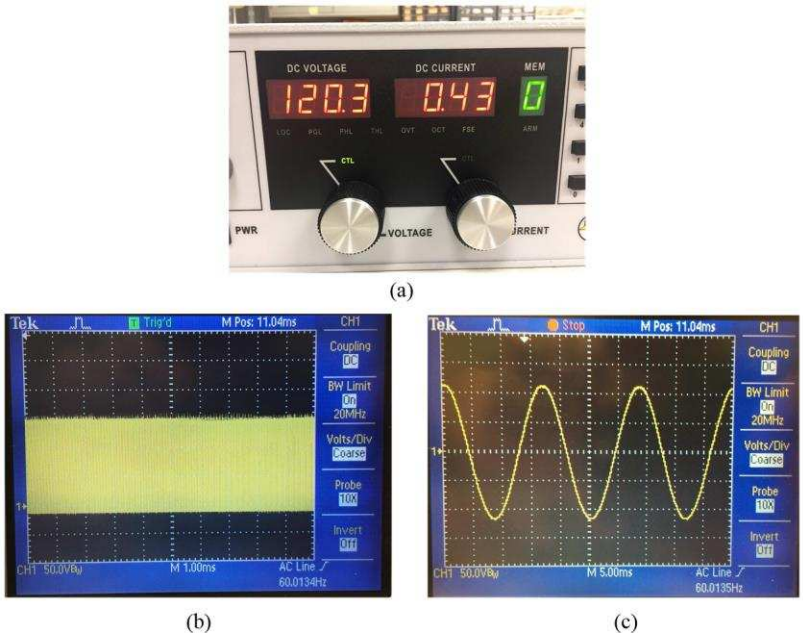
scheduling controller. Figure 4.2 further confirmed the stability of hardware prototype.



(a)

(b) (c)

Figure 4. 2 qZSI working at 110V, 50W (a) DC input voltage (b) Quasi-Z-Source network output voltage (c) Quasi-Z-Source inverter output AC voltage.



(a)

(b) (c)

Figure 4. 3 qZSI working at 120V, 50W (a) DC input voltage (b)Quasi-Z-Source network output voltage (c) Quasi-Z-Source inverter output AC voltage.

Thirdly, the input DC voltage was increased from 110V to 120V. Figure 4.3 revealed that both the Quasi-Z-Network output DC voltage and qZSI AC output voltage were the same as the reference.

4.3 Conclusion

These experiments successfully demonstrated all control algorithms for the Quasi-Z-Source inverter under low power conditions. Three working conditions were programed into DSP, and then each condition was tested one by one. The DC network output voltage and AC output voltage did not change under these three conditions. Boosted DC voltage does not have any voltage spikes which demonstrated the snubber circuit design. AC output voltage was sinusoidal and smooth, which proved the PCB design.

CHAPTER 5
CONCLUSION AND FUTURE WORK

5.1 Conclusion

This thesis presents complete design and implementation of an experimental prototype of single-phase Quasi-Z-Source inverter. The objectives for this master thesis have been successfully realized through analysis, simulation and experimental investigations. As a part of this research activity, a 1 kW prototype of single-phase Quasi-Z-Source inverter has been built and tested with all necessary interface circuits. I have derived a control-oriented model for the Z network of a voltage-fed quasi Z-source inverter (qZSI) and designed a gain scheduling state feedback integral control method in z domain based on this model. For the H-Bridge inverter output voltage control, I developed a robust digital control method which could fit into DSP based system. A real time control method also developed inside DSP to compensate for the counter compare submodule delay.

The entire control algorithms are programmed in C implemented by TMS320F28335-DSP. The hardware prototype was tested under three working conditions and testing results full demonstrate proposed control method. These experiments successfully demonstrated all control algorithms for the Quasi-Z-Source inverter under low power conditions. During the experimental work, the high voltage spikes appeared on the GaN-FETs was solved by a RC snubber circuit design. Possible suggestions for improvements of this research will be given in next section.

5.2 Future work

This single-phase Quasi-Z-Source inverter project has been fully developed at low power in the island mode. Future extension of the project will need to test this hardware prototype at high power condition. After that, I would like to develop my hardware into working for specific PV application for both island mode and grid connected mode, with MPPT included. For the grid connected mode, I will utilize conservative power theory technique to make it work as a active power filter once connected to the grid.

Future work of the present project includes:

- High efficiency single-phase Quasi-Z-Source inverter design;
- High power testing of single-phase Quasi-Z-Source inverter;
- Quasi-Z-Source inverter design for PV application in island mode;
- Quasi-Z-Source inverter design for PV application in grid connected mode;
- Implementing conservative power theory technique during grid connected mode

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