ANALYSIS AND DESIGN OF A SMART-INVERTER FOR RENEWABLE ENERGY INTERCONNECTION TO THE GRID

by
Aleksandr Reznik

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Golden, Colorado

Date _____

Signed: _____

Aleksandr Reznik

Signed: _____

Dr. Marcelo G. Simões
Thesis Advisor

Signed: _____

Dr. Ahmed Aldurra
Thesis Advisor

Golden, Colorado

Date _____

Signed: _____

Dr. R. Haupt

Professor and Head

Department of Electrical Engineering

and Computer Science

ABSTRACT

This Master thesis presents a three phase grid connected DC/AC inverter with active and reactive power (VAR) control for medium size renewable and distributed DC energy sources. The inverter, based on a voltage sourced inverter (VSI) configuration, allows the local residential energy generation to actively supply reactive power to the utility grid, at the same time, this topology allows to work this installation in stand alone (grid disconnected) mode maintaining nominal and clean voltage at nominal power. A low complexity grid synchronization method was introduced to generate direct and quadrature components of the grid voltage in a simple and computationally efficient manner in order to generate a synchronized current reference for the current loop control.

The main goal of this project is to study and to implement the control system of a grid-tied with LCL filter. The objectives of the project are divided in two parts: theoretical and experimental work. In the theoretical part, harmonics, inverter topologies, filter topologies, the design and the performance of the system will be discussed. Simulations were performed on Matlab/Simulink platform and a prototype was also developed in the lab to prove the effectiveness of the designed filter, controllers and grid synchronization method. The dSPACE hardware in the loop (HIL) was used, providing a good solution for laboratory implementation.

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NOMENCLATURE

X_d	Direct component of three phase voltage/current
X_q	Quadrature component of three phase voltage/current
X_α	α component of three phase voltage/current
X_β	β component of three phase voltage/current
f_g	Grid frequency
f_{res}	Resonant frequency
f_s	Sampling frequency
f_{sw}	Switching frequency
i_g	Grid line current
i_i	Inverter output line current
v_{LL}	Line to line voltage
v_g	Grid phase voltage
v_i	Inverter output phase voltage
v_l	Phase voltage at load terminals
$FACTS$	Flexible AC transmission system
PLL	Phase locked loop
PV	Photo voltaic
THD	Total harmonic distortion
VSI	Voltage source inverter
θ	Grid voltage phase angle
ω	Angular velocity

CHAPTER 1
INTRODUCTION

1.1 Objective

This thesis deals with the design, analysis and implementation of a three-phase grid-connected DC/AC inverter, where the input is a typical renewable energy source such as a photovoltaic array. This inverter has an advanced control that allows active and reactive power (VAR) control, focusing residential low power distributed applications. The main contributions in this work are the developments of harmonic filtering analysis plus the design and control of the inverter with grid synchronization techniques that may contribute for the state-of-art in interconnected grid inverter technology.

Initially the principles of three-phase grid connected inverter are presented in order to understand the basis for this work. A broad literature review is presented in order to cover system configurations, voltage and current controls, active and reactive power controls and grid synchronization methods. At the end of this chapter, the motivation and novel contributions derived in this work are presented, supporting the goals and procedures taken in this research.

1.2 Background and Motivation

The penetration of renewable and distributed energy sources is increasing exponentially all over in developed and developing countries. More stringent grid requirements imposed by utility operators are aimed in maintaining grid stability because of random nature of such non-dispatchable and dispersed small power plants. Distributed energy sources are connected to the grid through power converters which besides transferring the generated dc power to the ac grid should also be able to exhibit advanced functions like: dynamic control of active and reactive power, stationary operation within a range of voltage and frequency, voltage ride-through, reactive current injection during faults, participation in grid balancing act like primary frequency control, and so on [1].

The application for higher power must be managed by the distributed generation system; and such, usually leads to the use of more voltage levels in the inverter, leading to more complex structures based on a single-cell converter (like neutral point clamped multilevel converters) or a multicell converter (like cascade H-bridge or interleaved converters). In the design and control of the grid converter the challenges and opportunities are related to the need of using a lower switching frequency to manage a higher power level as well as to the availability of a more powerful computational control hardware and

more distributed intelligence, e.g. sensors and in the PWM drivers, Interconnections with the protection system, participation of multiple users and their decision constrains [1]. In addition, applications of high-power converter systems in electric power systems were in the past limited to high-voltage DC (HVDC) transmission systems and to some conventional static VAR compensator (SVC) and electronic excitation systems of synchronous machines. However, since the late 1980s, the application of high power electronic converters in electric power systems, for generation, transmission, distribution, and delivery of electric power, have been continuously advancing and finding further applications [2]. The main reasons are:

- Ongoing advancements in microelectronics technology have enabled realization of sophisticated signal processing and control strategies and the corresponding algorithms for a wide range of applications;
- Restructuring trends in the electric utility sector require power-electronic-based equipment to deal with issues such as improved reliability under power transmission and distribution congestion;
- Continuous growth in energy demand has resulted in close-to-the-limit utilization of the electric power utility infrastructure, calling for the employment of electronic power apparatus for stability enhancement;
- Deeper utilization of green energy as a response to the global warming and environmental concerns, associated with centralized power generation, caused a momentum with economic and technical viable solutions for renewable energy resources interfaced with the electric power system through power electronic converters;
- Development of new operational concepts and strategies, for microgrids, active networks, and smart grids [3]. Such applications require extensive use of intelligent based control for power electronic converters;
- Need of enhanced high efficiency and reliable converters for the existing power generation, transmission, distribution, and delivery infrastructure;
- Integration of large-scale renewable energy resources and storage systems in electric power grids;
- Integration of distributed energy resources, both distributed generation and distributed storage units, primarily, at sub-transmission and distribution voltage levels;
- Maximization of the depth penetration of renewable distributed energy resources;
- Avoidance of approximately 825 million metric tons of CO_2 emissions in the electric sector.

Therefore, all the reasons detailed above are supporting the motivation of the current work, where a real-time control of a grid-connected power electronic converter will be analyzed, designed and

implemented in order to support further developments of renewable energy integration with the utility grid.

1.3 Literature Review

This section details the background and literature on different approaches for VSI controls such as controls implemented in synchronous reference frame, rotating and natural reference frames, grid synchronization possibilities for these control techniques and harmonic filtering.

1.3.1 Harmonic Filtering

When a power converter is in grid-tied mode, the injected power quality must comply with interconnection standards [4], [5], which becomes a design concern with inverter - grid interface design as well as a controller design specification. The most common power converter is the voltage-source-inverter (VSI) which produced a modulated output voltage that must be filtered in order to parallelize a voltage output with the utility voltage grid. The most common type of filter is a pure inductance (L), which serves as an impedance for absorbing the voltage variation. Although a LC filter could potentially be used with transformer based interconnection (since the transformer has leakage inductance), the most recommended filter has a LCL (inductor-capacitor-inductor) topology. LCL filters seem to be a good solution for this problem, since they offer a higher harmonic attenuation with reduced power consumption. even with smaller inductances when compared to simple L filters [6]. The grid presents an unknown grid impedance which may cause instability by the dramatic changes of the resonant frequency in grid tie mode with an LC filter [7], [8]. There are different approaches to design LCL filter. Some authors propose iterative solution for parameters calculation and optimization using sophisticated algorithms like Particle Swarm Optimization (PSO) and Genetic Algorithm (GA) [9], [10]. However it has been observed that there is a gap in the analysis and evaluation of the LCL filter for systematic design methodology [11], [12]. So the comprehensive and detailed design procedure for the LCL filter and stability of the overall system will be provided.

1.3.2 VSI Controls

The control strategy applied to the stand-alone and grid connected inverter usually consists of two cascaded loops, i.e. a fast internal current loop, which regulates the grid active and reactive current, and an external voltage loop, which controls DC link voltage [13], [14], [15]. The current loop is responsible for power quality issues and current protection; thus harmonic compensation and dynamics are the important properties of the current controller [16]. The DC link voltage controller is designed for balancing the power flow in the system. Usually, the design of this controller aims for system stability

having slow dynamics. Some authors propose a grid-side control based on the fact that the dc-link voltage loop can be cascaded with an inner power loop instead of a current loop, so the current is not controlled directly [17].

There are three ways to implement current and voltage control for VSI as described next.

1.3.2.1 Synchronous Reference Frame control

Synchronous reference control is also known as dq control, it uses reference frame transformation $abc \rightarrow dq$ (see Appendix A), to transform the grid current and voltage waveforms into a reference frame that rotates synchronously with the grid voltage instantaneous angular frequency. After such transformation, the control variables become dc variables, thus control and filtering can be achieved relatively simple. This control method has been adopted from the electric machinery theory [18], [19], [21]. The dq control structure is usually associated with a proportional-integral (PI) strategy since they have a satisfactory performance when regulating dc variables. The controlled current must be in phase with the grid voltage, so the phase angle used by the $abc \rightarrow dq$ transformation module has to be extracted from the grid or reference voltage model. Phase-locked-loop (PLL) became a state of the art in extracting the grid voltage phase angle for grid synchronization [21], [22]. Synchronous Reference Frame PLL (SRF-PLL) is the most extensively utilized technique for frequency-insensitive grid synchronization in three-phase system. It has disadvantage in precise grid synchronization under unbalanced grid faults and low-voltage ride through [1]. Another more sophisticated option is Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL), for which two synchronous reference frames, rotating with positive and negative synchronous speed respectively are used. The fundamental variable estimated by this method is the grid phase angle. This technique needs more computation time, however presents smoother response during the transient faults [1].

1.3.2.2 Stationary Reference Frame Control

Another possible control implementation can be implemented using the stationary reference frame [2]. In this control structure, the grid currents are transformed to stationary reference frame using the $abc \rightarrow \alpha\beta$ transformation (see Appendix A for explanation). Here the control variables are sinusoidal and because of known drawback of PI controller in failing to remove the steady-state error when controlling sinusoidal waveforms, other controller types are required. One of the most popular and wide spread controller is the proportional resonant (PR) controller for current regulation of grid-tied systems [23], [24]. The main advantage of this controller is that it achieves a very high gain around the resonant frequency, thus being able ideally to eliminate the steady-state error between the controlled signal and its

reference [25]. The infinite gain that is possible in theory for a PR controller is not possible in practice. There are other modification of this kind of control like model predictive resonant controller described in [26]. The PR controller does not work well for variable frequency operation such as in machine drive systems or weak-grid utility systems.

1.3.2.3 Natural Reference Frame Control

The idea of abc control is to have an individual controller for each grid current. However, the different types of three phase configuration, i.e., delta, star with or without isolated neutral must be considered when designing the controller. In the situation of isolated neutral systems, the phases interact between each other, hence, only two controllers are necessary since the third current is given by the Kirchhoff's current law. Most often, having three independent controllers is possible by incorporating extra considerations in the controller design, as usually is the case for hysteresis and dead-beat based control [16].

Normally, the abc based control is has nonlinear controllers (hysteresis or dead beat) because of their good dynamic performance. The hysteresis control has been very popular because of its simple implementation, fast transient response, direct limiting of device peak current, and practical insensitivity of dc link voltage ripple that permits a lower filter capacitor. However, there are a few drawbacks of this method. It can be shown that the PWM frequency is not constant (varies within a band) and, as a result, non-optimum ripple is generated in the current [27]. The dead-beat current control has some limitation: bandwidth limitation due to the inherent plant delay and sensitivity to plant uncertainties [28].

In natural frame control three current references are generated using the phase angle of the grid voltages provided by a PLL. Each of them is compared with the corresponding measured current, and the error feeds the controller. If hysteresis or dead-beat controllers are employed in the current loop, there is no need of a modulator scheme. The output of these controllers gives the switching states for the transistors in the power converter. On the other hand, when three PI or PR controllers are used, the modulator is necessary to create the duty cycles for the PWM pattern. In summary, the three controllers have the following characteristics:

1) PI Controller: PI controller is widely used in conjunction with dq control, but its implementation in abc frame is also possible as described in [29]. This type of controllers due to the off-diagonal terms representing the cross coupling between the phases are very complex and hard to implement in real application.

2) PR Controller: The implementation of PR controller in abc is straightforward since the controller is already in stationary frame and implementation of three controllers is possible. It should be noticed that in this case, the influence of the isolated neutral in the control has to be accounted. However, it is worth emphasizing that the complexity is considerably reduced compared to previous case.

3) Deadbeat control is a predictive control which calculates the derivative of control variables to predict the system action. This controller has very fast theoretical response which makes it suitable for high-band-width applications, such as active filter or motor drive. This method, is prone to stability issues due to model and parameter time variation [30].

4) For the nonlinear control schemes, hysteresis control should be the simplest one which changes the switching state whenever the feedback signals exceed the preset bands [31]. This control has the advantage of fast response, inherent current-limit capability and no need of the plant parameters. This control scheme, has a variable switching frequency operation, which makes it very hard to design filters, difficult to perform frame transformation, not easy to perform interleaving technique, and could introduce over-heat and electromagnetic interference (EMI) issues. In [32], [33], [34] different methods and algorithms to obtain fixed switching frequency are presented.

1.4 Thesis Scope and Contributions

The research conducted to support this thesis is focused on making improvements of the behavior of grid converter connected to the utility grid through a LCL filter, where the following three attributes are fully developed and considered for improving grid-connected inverters for renewable energy applications:

1) Practical and clear directions for LCL filter modeling and physical design for VSI output harmonic mitigation. A comprehensive and detailed design procedure for the LCL filter has been provided and stability and dynamics of the overall system have been studied. It is found that the design meets the industry standards keeping the THD within the given range.

2) Robustness analysis and design of current and voltage controllers when connected to the grid and in standalone mode respectively. In order to control the inverter there are two major control strategies, current control and voltage control (VC). Current control is the most common way to control grid connected VSI's. A current controller has the advantage of being less susceptible to voltage phase shifts and to distortion in the grid voltage, thus it reduces the harmonic currents to a

minimum. If operated in standalone mode, voltage control would be a natural choice, but when operated in grid connected mode, current control is the most robust control.

3) Physical prototype implementation and proof of all theoretical conclusions. The real physical model of inverter with appropriate control systems was built for grid connected and stand-alone mode operation also ride through the grid connection and disconnection modes is performed.

1.5 Project Outline

This thesis is structured in 6 chapters:

Chapter 1 is an introduction to the project, containing short background, the project motivation and the goals of the project.

Chapter 2 contains the study and development of inverter control system, design of control loops, PLL implementation, LCL filter design, its transfer function derivation and parameters calculation.

Chapter 3 and Chapter 5 describes the results of simulations and the experimental work which have been done. The tests have focus on verifying the developed control system models and results verifications through experiments.

Chapter 4 describes the electronic circuits and computational hardware used for the experimental evaluation of the inverter system.

Chapter 6 is the conclusion, which includes also future work.

CHAPTER 2

MATHEMATICAL AND ENGINEERING ANALYSIS

2.1 Introduction

This chapter presents the inverter control design, with optimized LCL output filtering and grid synchronization through a PLL. Initially, the PLL is described and feeds the signals for the current loop, which is implemented based on a proportional-integral (PI) controller, capable of running in both stand-alone and grid-connected modes. The last section of this chapter shows the design procedure for a LCL filter, emphasizing their performance analysis based on rigorous mathematical modeling. The block diagram of the inverter control considered in this project is shown on Figure 2.1.

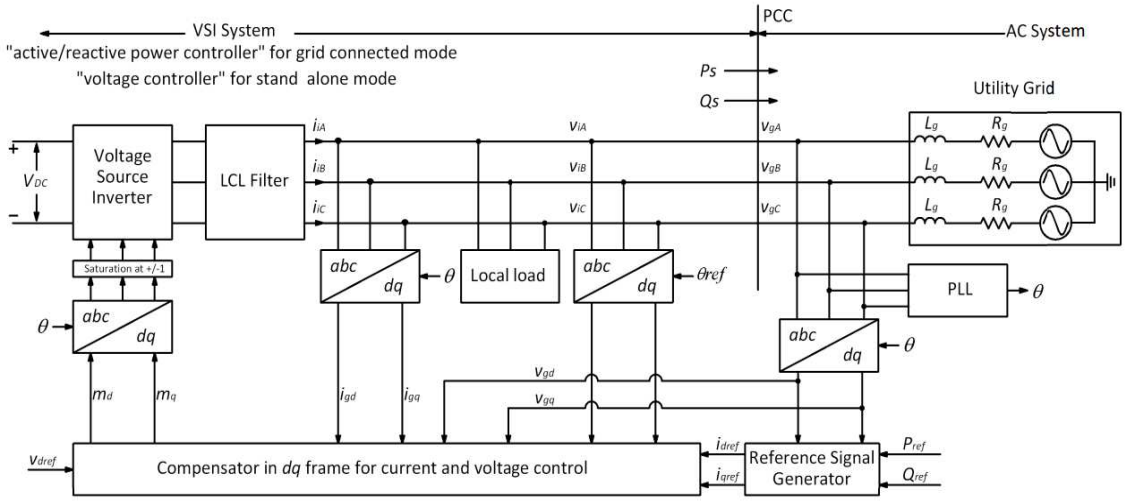

Figure 2.1 Block diagram of the three phase inverter control system.

The current is oriented along the active voltage component (V_d), this is why this strategy is called voltage oriented control. A PLL algorithm detects the phase angle of the grid, the grid frequency and the grid voltage. The frequency and voltage are needed for monitoring the grid conditions and for dynamic stability of the system. The phase angle of the grid is required for reference frame transformations (see Appendix A). If a PI current control is implemented, then the currents are transformed into the synchronous reference frame, and the algorithm also implements the decoupling between the two axes.

For stand alone mode, a standard PI controller is used to maintain constant voltage at output terminals of inverter. The algorithm for inverter output voltage control in stand-alone mode is very similar to PLL algorithm, both will be discussed in following sections.

The modulation block calculates the proper states of the inverter switches in order to obtain the reference input voltage.

2.2 PLL for Inverter Synchronization with the Utility Grid

A PLL system is commonly used for various signal applications such as in radio and telecommunications, electrical motor control and in the last few years for power electronic applications. PLL techniques can be adapted to work in a wide frequency spectrum from a few hertz to orders of gigahertz.

There are mainly three types of phase locked loop (PLL) systems for phase tracking: (i) zero crossing, (ii) stationary reference frame and (iii) synchronous rotating reference frame (SRF) based PLL [1]. The SRF PLL is the one with good performance under distorted and non-ideal grid conditions, also it is applicable for single-phase and three-phase applications [35]. The reason of superior performance of SRF PLL in synchronization will be discussed later.

2.2.1 PLL Theory

A basic PLL configuration is depicted in Figure 2.2. The phase voltages v_{gA}, v_{gB}, v_{gC} are obtained from sampled phase voltages. These stationary reference frame voltages are then transformed to voltages V_d, V_q (in a frame of reference synchronized to the utility frequency) using $\alpha\beta$ and dq transformation.

The angle θ^*used in these transformations is calculated by integrating a frequency signal ω^* and the initial angle must be carefully setup as initial condition in this integrator. If the frequency command $\omega^*$is identical to the utility frequency, the voltages V_d and V_q appear as DC values depending on the angle θ^* [21].

The $\alpha\beta$ transformation (Clarke transformation, see Appendix A), allows to represent three phase system v_{gA}, v_{gB}, v_{gC} as two phase $V_\alpha$and V_β. The control in $\alpha\beta$ frame has the feature of reducing the number of required control loops from three to two. However, the reference and feedback signals are in general sinusoidal functions of time. Therefore, to achieve a satisfactory performance and small steady-state errors in magnitude and phase, the compensator design is not straight forward task [2]. The dq frame based control offers a solution to this problem. In dq frame (Park transformation, see Appendix A), the signals assume DC waveform under steady-state conditions. This, in turn, permits the utilization of compensators with simpler structures and lower dynamic orders. The dq and $\alpha\beta$ transformations and control in dq frame are discussed in the following subsections.

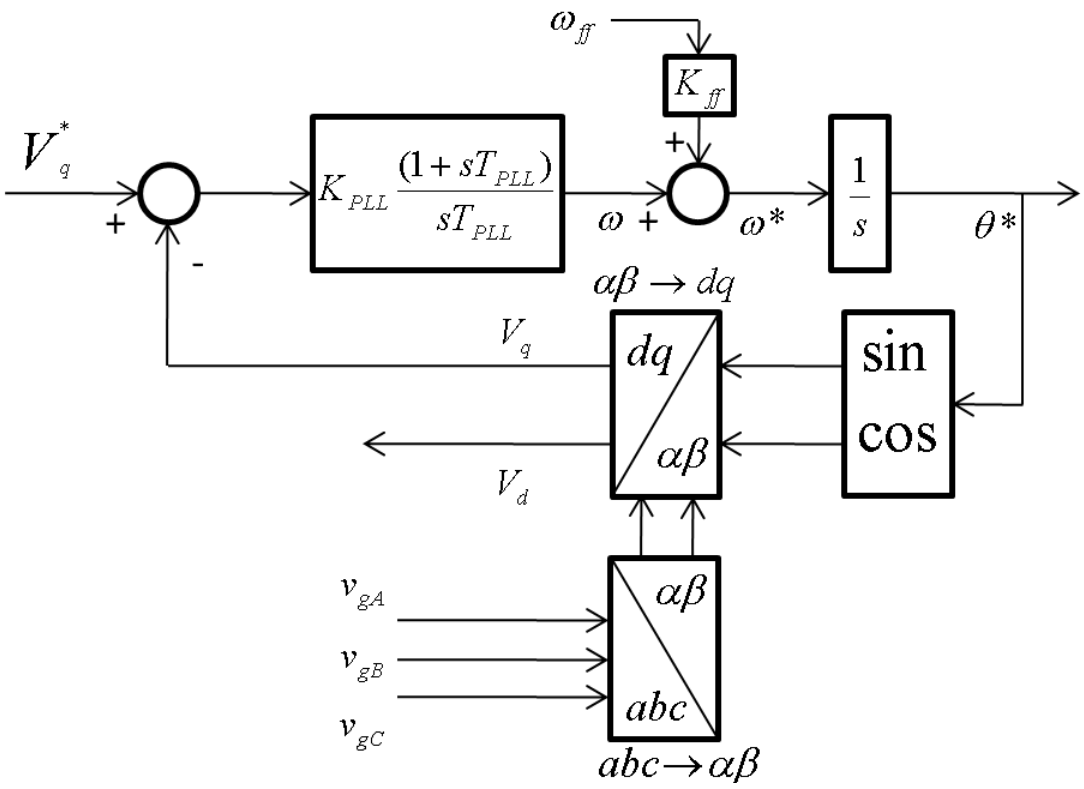

Figure 2.2 PLL block diagram.

A feed-forward reference ($\omega_{ff} = 2\pi f_g$) is included to improve the initial dynamic performance, where f_g - is the grid nominal frequency [35]. Adding ω_{ff} helps to decrease the starting time of the PLL [36].

2.2.2 Phase Deviation

The utility grid is typically a very stiff system as regards to the supply frequency. A deviation in the supply frequency will cause the phase angle error to increase. The PI regulator naturally works to bring this error to zero. The reaction to frequency fluctuations is thus completely predictable by the closed-loop response of the PLL system. The feed-forward term ω_{ff} applied through the gain K_{ff} facilitates the function of the regulator to a large extent. If the supply frequency is inclined to change (e.g., stand-alone power systems as diesel generators which are not very stiff), there will be tracking error in the phase angle θ as long as the frequency is changing. If the change in frequency is known, the tracking error can be eliminated by the feed-forward term. If the change in frequency is not predictable, an additional integral term may be used in the PI regulator to achieve the same result [21].

2.2.3 Positive Sequence Detector

Almost as old as the AC power systems utilization, is the issue of positive sequence identification. Most approaches and algorithms have been based on the Symmetrical Components method presented by Fortescue in 1918, which is basically a frequency domain approach. Nevertheless, considering modern power conditioning controllers and real time power quality evaluation, the instantaneous (time domain) calculation of the positive sequence components is becoming an interesting application. Different algorithms have been proposed to achieve such objective and the most frequent techniques are based on some time domain adaptation of the Fortescue's decomposition or on some kind of voltage peak detector. However, most of them are derived assuming purely sinusoidal voltages or currents and do not work properly if facing distorted waveforms. Some techniques also propose filtering the measured voltages in order to identify the fundamental component and then, calculate the positive sequence [37].

Figure 2.3 shows the positive sequence detector presented in [37]. This paper presents full and informative analysis of proposed algorithm, its performance and advantages, proved by simulation and experimental data. The need of this positive sequence detector was discovered during the experimental work. Unfortunately power distribution system in our building represents a weak with distorted and unbalanced three phase system, which will be detailed in Chapter 5.

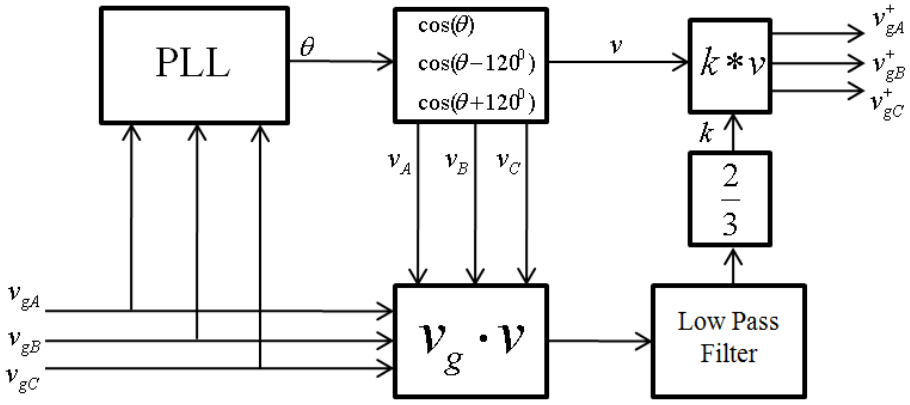

Figure 2.3 Algorithm of the positive sequence detector.

Here positive sequence detector takes θ phase angle (phase A synchronization) and generates unitary signals $v = [v_A v_B v_C]$, which are in phase with fundamental of the input voltages $v_g =$

$[v_{gA} v_{gB} v_{gC}]$. The dot product of the measured voltages and in phase with unitary signals $v_g \cdot v$ yields an instantaneous variable represented by the constant value $\bar{x}$ and oscillatory part $\tilde{x}$:

$$v_g \cdot v = v_{gA} \cdot v_A + v_{gB} \cdot v_B + v_{gC} \cdot v_C = \bar{x} + \tilde{x}, \tag{2.1}$$

where the constant value $\bar{x}$, if multiplied by $2/3$ results the instantaneous magnitude of the positive sequence, as defined be Fortescue for steady state conditions [37].

2.2.4 Transfer Function

Since this system will be working with sampled data one has to consider the delay due to sampling. The transfer function for the plant on Figure 2.2 is just a time lag and an integrating element such as the following equation:

$$G_{plant} = \left(\frac{1}{1 + sT_s}\right)\left(\frac{1}{s}\right) \tag{2.2}$$

where T_s is the sampling period. The open loop transfer function for the system is described as follows:

$$G_{ol} = \left(K_{PLL}\frac{1 + sT_{PLL}}{sT_{PLL}}\right)\left(\frac{1}{1 + sT_s}\right)\left(\frac{V_m}{s}\right) \tag{2.3}$$

When going from the open loop system to the closed loop system the relation between the transfer function is

$$G_{cl} = \frac{G_{ol}}{1 + G_{ol}} \tag{2.4}$$

2.2.5 Designing the PI Controllers Gains

There are several different methods for designing the PI-regulator gains [38], [39]. In this work it is considered an approximation by a second order system and it is used the symmetrical optimum method (SO). The SO method has been investigated and used for similar PLL grid connecting applications before [21].

2.2.5.1 Symmetrical Optimum Method

The SO method optimizes the phase margin to have its maximum at a given crossover frequency ω_c. The phase margin is defined as the number of degrees the frequency response may be phase shifted without losing stability; this corresponds to the distance from the point -1 in a plot of frequency response

on the complex plane. The amplitude and phase plot will also be symmetric around ω_c [21], see the Figure 2.4.

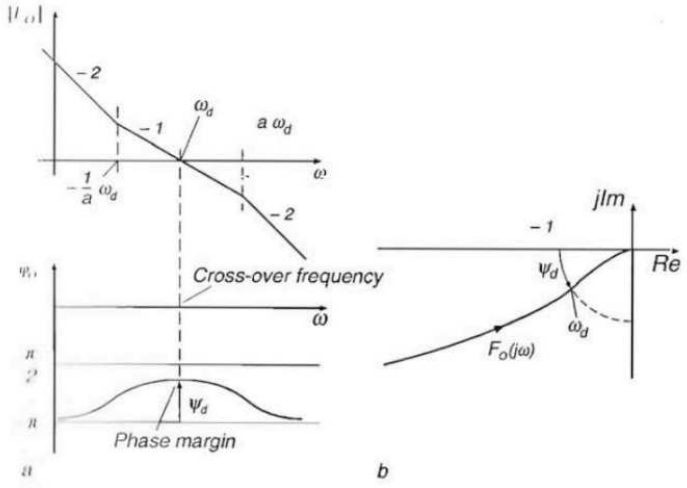

Figure 2.4 The characteristics of a system and a PI controller designed with the SO method: a) The Bode plot with its symmetrical shape at the crossover frequency. b) The frequency response locus with phase margin ψ_d.

The transfer function

0
$$F = \frac{\omega_0^2(ks + \omega_o)}{s^2(s + k\omega_0)} \tag{2.5}$$

where k is the constant, will be symmetric around crossover frequency $\omega = \omega_c$. Rewriting the transfer function for the PLL system:

$$G_{ol} = \left(K_{PLL}\frac{1 + sT_{PLL}}{sT_{PLL}}\right)\left(\frac{1}{1 + sT_s}\right)\left(\frac{V_m}{s}\right)$$
$$= \frac{\frac{K_{PLL}V_m}{T_s}\left(s + \frac{1}{T_{PLL}}\right)}{s^2\left(s + \frac{1}{T_s}\right)} = \frac{\frac{K_{PLL}V_m}{aT_s}\left(as + \frac{a}{T_{PLL}}\right)}{s^2(s + \frac{1}{T_s})} \tag{2.6}$$

where a is a normalization factor. Comparing two previous equations gives the following identifications:

$$\begin{cases} \frac{1}{T_s} = a\omega_c \\ \frac{a}{T_{PLL}} = \omega_c \\ \frac{K_{PLL}V_m}{aT_s} = \omega_c \end{cases} \tag{2.7}$$

After simplifying:

$$\begin{cases} \omega_c = \dfrac{1}{aT_s} \\ T_{PLL} = a^2 T_s \\ K_{PLL} = \dfrac{1}{aV_m T_s} \end{cases} \tag{2.8}$$

which is the result for the regulator gains using the SO method. For a given sample period T_s the crossover frequency can be chosen by adjusting the normalization factor a. Finally the regulator gains is calculated with the resulting normalization factor a [21]. For a second order system the quotient between crossover frequency ω_c and the bandwidth ω_B for the closed loop system is approximately constant and:

$$0.6 < \frac{\omega_c}{\omega_B} < 0.8 \tag{2.9}$$

for different values of K_{PLL}.When designing the gains the following constrains must be considered for the step response:

- Higher phase margin gives less oscillatory response
- Lower value of τ decreases settling time
- Value of K_{PLL} effects both phase margin and bandwidth

This implies that a good value for a crossover frequency ω_c would be around the utility frequency of $60Hz$ that gives maximal margin at $60Hz$. The closed loop system will also have the characteristics of a low pass filter with bandwidth $\omega_B \approx \frac{\omega_c}{0.7} \approx 85.71Hz$. The PLL system will then be able to reduce harmonics from the output without the need of an external filter, which is a very desirable property.

In practice the designing process is an iterative process. First calculate the gains with SO method and from bode plots or simulations determine phase margin, bandwidth, settling time, etc. Change K_{PLL} or T_{PLL} and plot again and so on until the system is fulfilling the specifications.

Choice of sampling frequency is a trade-off between resolution and losses. Higher sampling frequency will give better representation of the grid voltages but on the other hand it will cost more computational capacities and greater power losses in the switchers.

Any utility instantaneous over-voltage or under-voltage will generate harmonics which will enter the PLL loop through the sampled phase voltages v_{gA}, v_{gB}, v_{gC}. While the notches normally will not affect the locking capability of the PLL, they will cause harmonics in the PLL output, propagating to the

associated control utilizing θ^*. The obvious method would be to eliminate the harmonics with filters; either applied for the sampled voltages or for the error term of the control loop. However, it must be noted that the PLL system inherently has strong filtering properties due to the two integrators in series in the forward path [1]. The factor a provides a simple handle to modify the inherent filtering properties of the system without the use of any additional filters.

Because the amplitude of the utility voltage shows as a gain term in the forward path, any dip or unbalance in the line voltage will cause a loss of gain V_m for the control system. This effect can be eliminated by normalizing the feedback term V_d for the utility magnitude V_m. Calculation of an accurate value of V poses interesting problems if the utility is distorted. As a first approximation: if $V_d^* = 0$, the feedback term V_q, could be substituted for V_m. Alternatively, the gains of the PI regulator should be changed to accommodate variations in V_m [21].

2.2.5.2 Parameters Calculation and System Characteristics

The parameters which are used to design PLL controller are the following:

$V_{max} = \sqrt{2}\,120 = 170V$-peak value of the phase grid voltage
$f_g = 60Hz$ - grid frequency
$f_s = 10kHz$ - sampling frequency
$fc = 60Hz$ - crossover frequency

Using these parameters:

$$\begin{cases} a = \dfrac{1}{\omega_c T_s} = \dfrac{10000}{2\pi 60} = 25.54 \\ \tau = \dfrac{a}{\omega_c} = \dfrac{25.54}{2\pi 60} = 0.0704 \\ K_{PLL} = \dfrac{1}{a V_m T_s} = \dfrac{10000}{25.54 * 120\sqrt{2}} = 2.31 \end{cases} \tag{2.10}$$

Using the values of Equation (2.10) in Equation (2.3) gives the transfer function for the open loop system, and a Bode plot of the transfer function is presented in Figure 2.5. From the Bode plot the symmetrical shape is confirmed and the phase margin $\psi = 87.8$ degrees at the crossover frequency $\omega_c = 377\ rad/s$, see Figure 2.5.

The transfer function of the closed loop system can be calculated using Equation (2.4). A Bode plot on Figure 2.6 of closed loop system confirms the low pass filter behavior of the system.

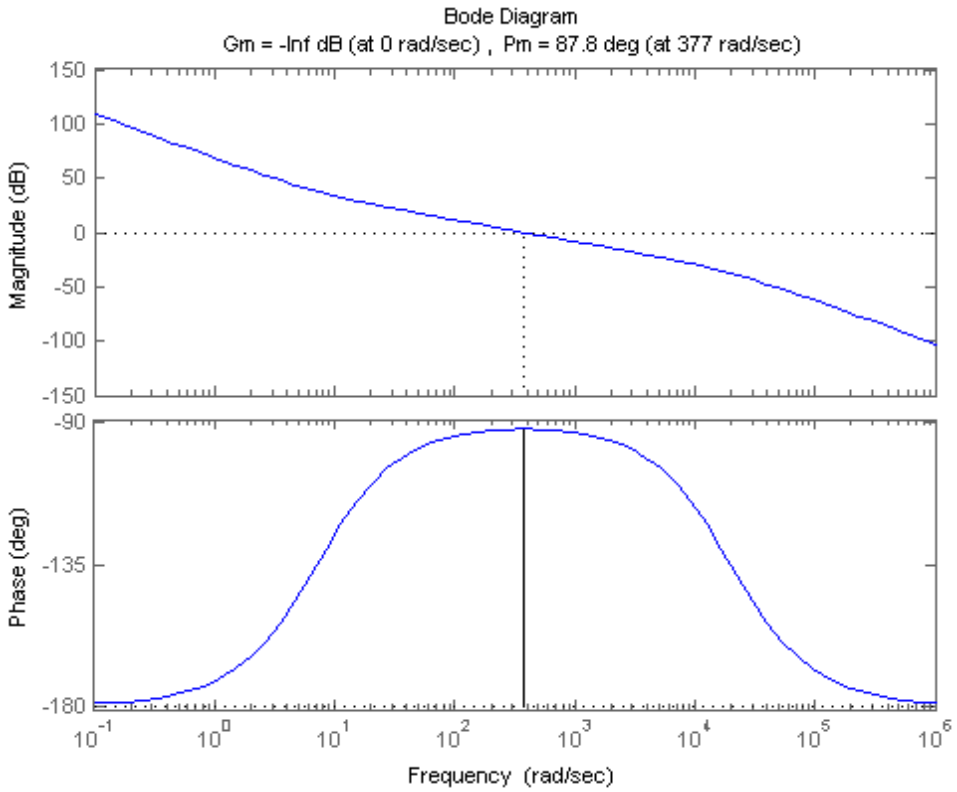

Figure 2.5 Open loop frequency response.

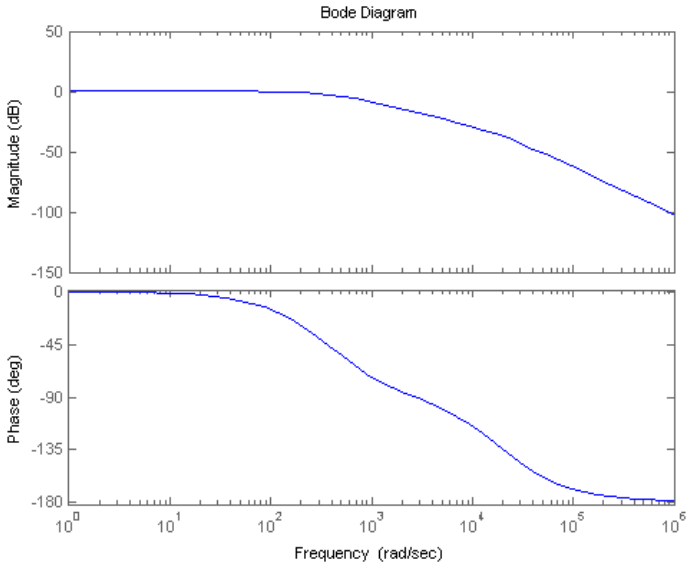

Figure 2.6 Closed loop system frequency response.

The bandwidth can be calculated with the Matlab built-in command BANDWITH and is equal 62.135 Hz.

2.3 Pulse Width Modulation(PWM)

The PWM modulators are open-loop voltage controllers, and the most common methods for PWM modulation is carrier based PWM, space vector modulation and random PWM. The main differences between these methods are described in [27]. Here only sinusoidal carrier based PWM technique will be described, since only this PWM is utilized in the project.

2.3.1 Sinusoidal PWM (SPWM)

The sinusoidal PWM techniques is easy for implementation and very popular for industrial converters. The PWM principle to control the output voltage is explained in Figure 2.7.

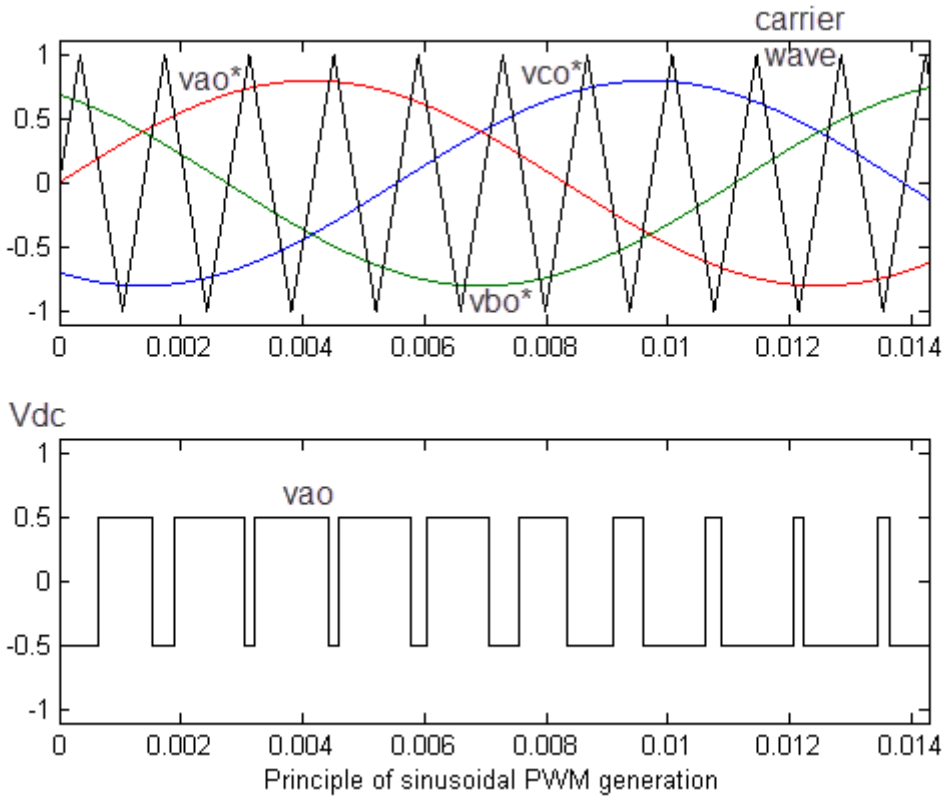

Figure 2.7 Principle of sinusoidal PWM for three phase VSI.

Figure 2.8 explains the general principle of SPWM, where isosceles triangle carrier wave is compared with fundamental frequency sinusoidal modulating wave, and the points of intersection determine the switching points of power devices. This method is also known as triangulation, subharmonic or suboscillation method. The notch and pulse widths of v_{ao} wave vary in a sinusoidal manner so that the average of fundamental component frequency is the same as the frequency of

modulating signal and its amplitude is proportional to the command modulating voltage. The same carrier wave can be used for all three phases, as shown on Figure 2.7

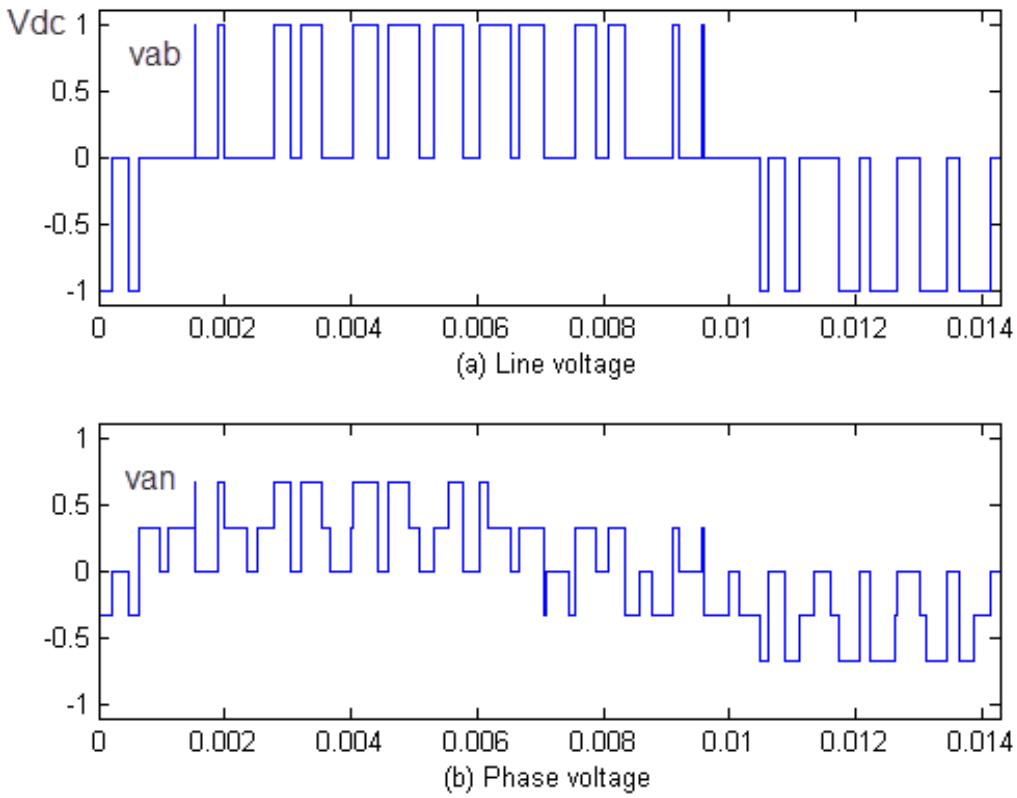

Figure 2.8 Line and phase voltage waves of PWM voltage source inverter [27].

The maximum output voltage in the linear region when modulation index m is between 0 and 1 for SPWM is:

$$V_{LL} = \frac{\sqrt{3}}{2\sqrt{2}} = 0.612 V_{DC} \tag{2.11}$$

and

$$m = \frac{V_P}{V_T} \tag{2.12}$$

where V_P peak value of the modulating wave and V_T peak value of the carrier wave.

2.4 Inverter Control Approaches

In a voltage source inverter (VSI) system the active power P and reactive power Q can be controlled based on two distinct methods. The first approach is schematically illustrated in Figure 2.9 and is commonly referred to as voltage-mode control. The voltage-control mode has been mainly utilized in high voltage/power applications such as in Flexible Alternating Current Transmission System (FACTS) controllers, although industrial applications have also been reported. In this work, as an approximation we consider an infinite bus or a stiff voltage AC system. Thus, the AC system is modeled by an ideal three-phase voltage source. It is also assumed that grid voltages are sinusoidal and balanced (sometimes not really true in industrial and commercial installations) and of a relatively constant frequency. The VSI system of Figure 2.9 exchanges the real and reactive power components P_S and Q_S with AC system, at the point of common coupling (PCC).

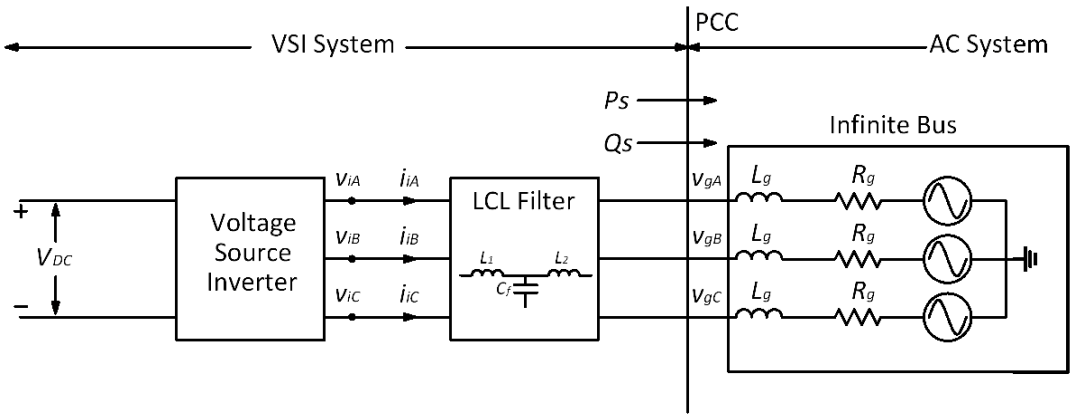

Figure 2.9 Schematic diagram of a grid-imposed frequency VSI system.

In voltage-controlled real/reactive power controller, the real and reactive power are controlled, respectively, by the phase angle and amplitude of the VSI AC-side terminal voltage relative to those of the PCC voltage. If the amplitude and phase angle of V_{ABC} are close to those of V_{gABC}, the real and active power are almost decoupled and two independent compensators can be employed for their control. Thus the voltage-mode control has the merit of being simple and having a low number of control loops. However, since there is no control loop dedicated to the VSI line current, the VSI is not protected against overcurrents, and the current can undergo large excursions if the commands are changed rapidly or the AC system is subjected to a fault.

The second approach to control the real and reactive power in the VSI system of Figure 2.10 is referred to as current-mode control. In this approach, initially the VSI AC-side current is controlled by a dedicated control scheme, through the VSI terminal voltage. Then, both real and reactive power are

controlled by the phase angle and the amplitude of the VSI line current with respect to the PCC voltage. Thus, due to current regulation scheme, the VSI is protected against overload conditions. Other advantages of the current-mode control include the robustness against variations in parameters of the VSI and AC system, superior dynamic performance, and higher control precision [2].

Compared to the abc-frame, the $\alpha\beta$-frame control of a grid-imposed frequency VSI system reduces the number of plants to be controlled from three to two. Moreover, instantaneous decoupled control of the real and reactive power, exchanged between the VSI system and the AC system, is possible in $\alpha\beta$-frame. However, the control variables, that is, feedback signals, feed-forward signals, and control signals are sinusoidal functions of time. It is shown here that the dq-frame control of a grid-imposed VSI system features all merits of the $\alpha\beta$-frame control, in addition to the advantage that the control variables are DC quantities in steady state. This feature remarkably facilitates the compensator design, especially in variable-frequency scenarios. Figure 2.10 shows a schematic diagram of a current-controlled real/reactive power controller, illustrating that the control is performed in dq frame. Thus, P_s and Q_s are controlled by the line current components i_{gd} and i_{gq}. The feedback and feedforward signals (voltages and currents) are first transformed to the dq frame. Finally, the control signals are transformed to the abc frame and fed to the VSI (Figure 2.10). To protect the VSI, the reference commands i_{dref} and i_{qref} are limited by the corresponding saturation blocks (not shown in the Figure 2.10).

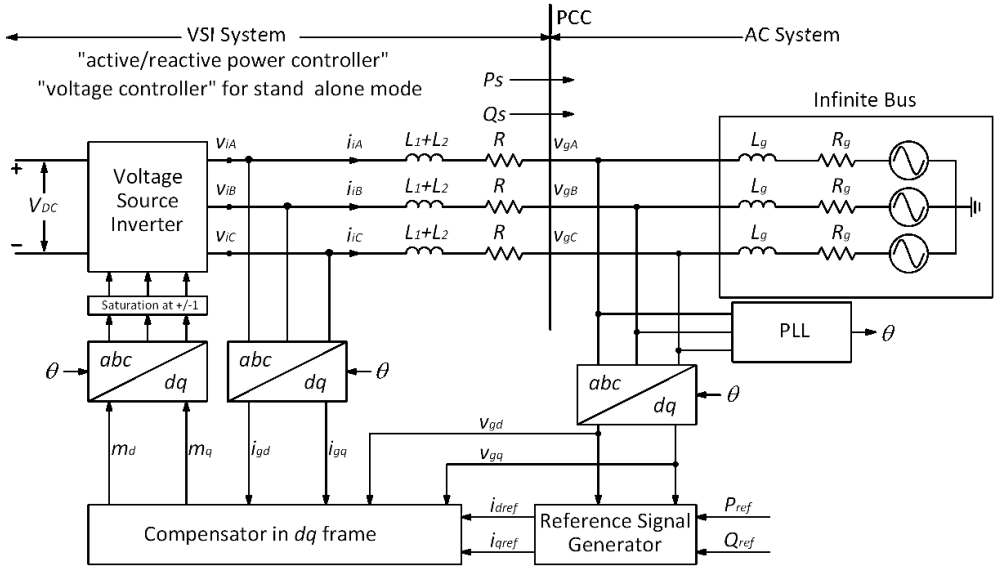

Figure 2.10 Schematic diagram of a current-controlled active/reactive power controller in dq frame.

In order to achieve zero-steady-state error in $\alpha\beta$-frame control, the bandwidth of the closed-loop system must be adequately larger than the AC system frequency; alternatively, the compensators can include complex-conjugate pairs of poles at the AC system frequency and other frequencies of interest, to increase the loop gain. In dq - frame control, however zero steady state error is readily achieved by including integral terms in the compensators since the control variables are DC quantities. The dq-frame representation and control of a grid-imposed VSI system is also consistent with the approach used for the dynamic analysis of the large power system. The small-signal dynamics of the power system is conventionally modeled and analyzed in dq-frame.

2.4.1 Dynamic Model of Active/Reactive Power Controller

In a VSI system the active (P) and reactive (Q) powers can be controlled based on two distinct methods. The first approach is schematically illustrated in Figure 2.9. In order to design the control system some simplifications can be done. For example, the filter term with the capacitor and damping resistor can be neglected. The dynamics of the full LCL circuit including the specification for a damped resonance will be discussed later.

Assume that the AC system voltage in the VSI system of Figure 2.9 is expressed as

$$\begin{aligned} v_{gA} &= V_g \sin(\theta) \\ v_{gB} &= V_g \sin(\theta - \frac{2\pi}{3}) \\ v_{gC} &= V_g \sin(\theta + \frac{2\pi}{3}) \end{aligned} \tag{2.13}$$

where V_g is the peak value of the line-to-neutral voltage, $\theta = \omega_g t$, ω_g is the AC system (source) frequency. Dynamics of the AC side of voltage source inverter system on Figure 2.9 are described by the following differential equations:

$$(L_1 + L_2)\frac{di_g}{dt} = -Ri_g + v_i - v_g \tag{2.14}$$

for our three phase system:

$$\begin{aligned} v_{iA} &= (L_1 + L_2)\frac{di_{ga}}{dt} + Ri_{ga} + v_{gA} \\ v_{iB} &= (L_1 + L_2)\frac{di_{gb}}{dt} + Ri_{gb} + v_{gB} \end{aligned} \tag{2.15}$$

$$v_{iC} = (L_1 + L_2)\frac{di_{gc}}{dt} + Ri_{gc} + v_{gC}$$

or in matrix form

$$\frac{d}{dt}\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} = \frac{1}{L}\begin{bmatrix} v_{iA} \\ v_{iB} \\ v_{iC} \end{bmatrix} - \frac{R}{L}\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} v_{gA} \\ v_{gB} \\ v_{gC} \end{bmatrix} \tag{2.16}$$

For simplicity, it is considered that $L = L_1 + L_2$, $R = R_1 + R_2$, where R_1 and R_2 resistances of first and second inductor respectively.

A common and often adopted approach in analyzing three-phase systems is to use a stationary or rotating frame [1]. In the first case the frame will be denoted as $\alpha\beta$ and in second as dq and it is also called synchronous. In fact the dq frame is synchronized with the angular speed ω_g. The space vectors that express the inverter electrical quantities are projected on the α axis and β axis or on d axis and q axis.

The mathematical model in the $\alpha\beta$ frame is

$$\begin{cases} \dfrac{dI_{g\alpha}}{dt} = \dfrac{1}{L}[V_{i\alpha} - V_{\alpha g} - RI_{\alpha g}] \\ \dfrac{dV_{g\beta}}{dt} = \dfrac{1}{L}[V_{i\beta} - V_{\beta g} - RI_{\beta g}] \end{cases} \tag{2.17}$$

It should be noted that the particular feature of the dq frame is that if a space vector with constant magnitude rotates at the same speed of the frame, it has constant d and q components while if it rotates at a different speed it has a time-variable magnitude (pulsating components). In the dq frame, differential equations for the current are dependent due to the cross-coupling terms $\omega_g I_{gq}$ and $\omega_g I_{gd}$, and the equations also have feed forward terms V_{gd} and V_{gq}.

Thus a dq frame rotating at the angular speed ω_g becomes

$$\begin{cases} \dfrac{dI_{gd}}{dt} = \dfrac{1}{L}\left[V_{id} - V_{gd} - RI_{gd}\right] + \omega_g I_{gq} \\ \dfrac{dI_{gq}}{dt} = \dfrac{1}{L}\left[V_{iq} - V_{gq} - RI_{gq}\right] - \omega_g I_{gd} \end{cases} \tag{2.18}$$

or in matrix form

$$\begin{bmatrix} V_{id} \\ V_{iq} \end{bmatrix} = \underbrace{R\begin{bmatrix} I_{gd} \\ I_{gq} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} I_{gd} \\ I_{gq} \end{bmatrix}}_{Filter\ dynamics} + \underbrace{L\omega_g \begin{bmatrix} -I_{gq} \\ I_{gd} \end{bmatrix}}_{Decoupling} + \underbrace{\begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix}}_{feedforward\ term} \tag{2.19}$$

2.4.2 Dynamic Model of Active/Reactive Power Controller

The power control of the grid inverter is based on the dq-frame power theory and as a consequence on the definition of the power in a reference frame, as discussed earlier. Typically the voltage oriented control is based on the use of a dq frame rotating at ω_g speed and oriented such that the d axis is aligned on the grid voltage vector. The space vector of the fundamental harmonic has constant components in the dq frame while the other harmonics space vectors have pulsating components. The main purpose of the grid inverter is to generate or to absorb sinusoidal currents; thus the currents reference components in the dq frame are DC quantities [2].

The reference current component i_d^* is controlled to manage the active power control; while the reference current component i_q^* controls the reactive power exchange and it is typically used to impress a desired power factor:

$$P_{dq} = \frac{3}{2}(V_d I_d + V_q I_q) \tag{2.20}$$

$$Q_{dq} = \frac{3}{2}(V_q I_d - V_d I_q) \tag{2.21}$$

Assuming that the d axis is perfectly aligned with the grid voltage $v_{qg} = 0$, the active power and the reactive power will therefore be proportional to i_d and i_q respectively [2]:

$$P_{dq} = \frac{3}{2}V_d I_d \tag{2.22}$$

$$Q_{dq} = -\frac{3}{2}V_d I_q \tag{2.23}$$

The control block diagram is shown in Figure 2.11.

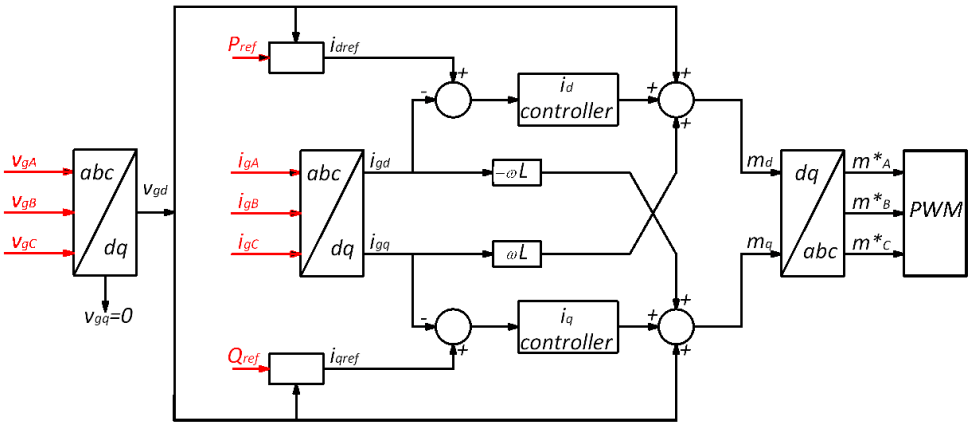

Figure 2.11 Control block diagram.

2.4.3 Current Regulator with a PI Control

The block diagram of the PI regulator is shown on Figure 2.12 and the transfer function is given by Equation (2.14)

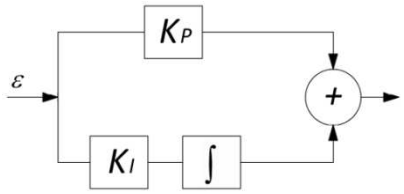

Figure 2.12 Block diagram of PI controller.

The d and q control loops have the same dynamics (in ideal case of DC values), so the tuning of the PI controller for the current is done only for the d axis. For the q axis the parameters are assumed to be the same. As it can be seen from the current control block diagram in Figure 2.13, the voltage feed forward and the decoupling between the d and q axes has been neglected as they are considered as disturbances.

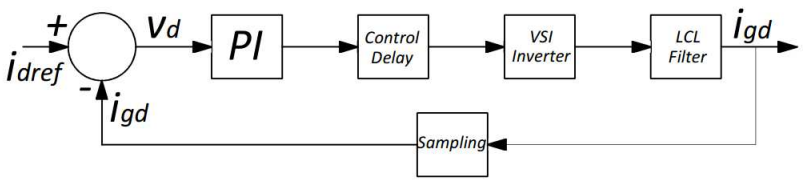

Figure 2.13 Block diagram of the current control loop.

This block diagram contents the following blocks:

- PI controller with transfer function:

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{2.24}$$

- Control time delay block with transfer function:

$$G_{control}(s) = \frac{1}{1 + sT_s} \tag{2.25}$$

where $T_s = \frac{1}{f_s}$ - sampling time for the control system

- Inverter block with transfer function:

$$G_{inverter}(s) = \frac{1}{1 + 0.5sT_{sw}} \tag{2.26}$$

where $T_{sw} = \frac{1}{f_{sw}}$ - switching period.

- Filter block is a simplified transfer function of the filter, that takes into account only the values of inductances and parasitic resistances:

$$G_{filter}(s) = \frac{1}{Ls + R} \tag{2.27}$$

- Sampling block with transfer function:

$$G_{samping}(s) = \frac{1}{1 + 0.5sT_s} \tag{2.28}$$

The transfer function of the current loop can be calculated as:

$$G_{cl} = G_{PI} * G_{control} * G_{inverter} * G_{filter} * G_{sampling} \tag{2.29}$$

The transfer function of the current loop can be written in a simplified manner as:

$$G_{cl} = \frac{K_p s + K_i}{s} \frac{1}{1 + sT_{\Sigma 1}} \frac{K_e}{(sT_e + 1)} \tag{2.30}$$

where $K_e = \frac{1}{R}$, $T_e = \frac{L}{R}$ and $T_{\Sigma 1} = T_s + 0.5T_{sw} + 0.5T_s$.

Using optimal modulus criterion [1], the following relation can be written:

$$\frac{K_p s + K_i}{s} \frac{1}{1 + sT_{\Sigma 1}} \frac{K_e}{sT_e + 1} = \frac{1}{2sT_{\Sigma 1}(1 + sT_{\Sigma 1})} \tag{2.31}$$

From Equations (2.32) and (2.33) K_p and K_i can be identified and their values calculated, as:

$$K_p = \frac{T_e}{2K_e T_{\Sigma 1}} = 11 \tag{2.32}$$

$$K_i = \frac{K_p}{T_e} = 170 \tag{2.33}$$

These values are used to start the analysis using Matlab toolbox, SISOtool. The Bode plot of the open-loop current control depicted in Figure 2.15. The step response is plotted in Figure 2.14. It can be seen that for continuous control system settling time of 0.00881s. is obtained.

2.4.4 Voltage Loop Control in Stand-Alone Mode

The previous section discussed the control and operation of a grid-imposed frequency VSI system in which the operating frequency can be predetermined and imposed by the AC system. In the absence of the utility grid, renewable energy systems could be used to provide energy to the local loads assuming and adequate supply of energy for the inverter to draw upon. The control structure on the DC and AC sides are changed to accommodate the needs of the local loads.

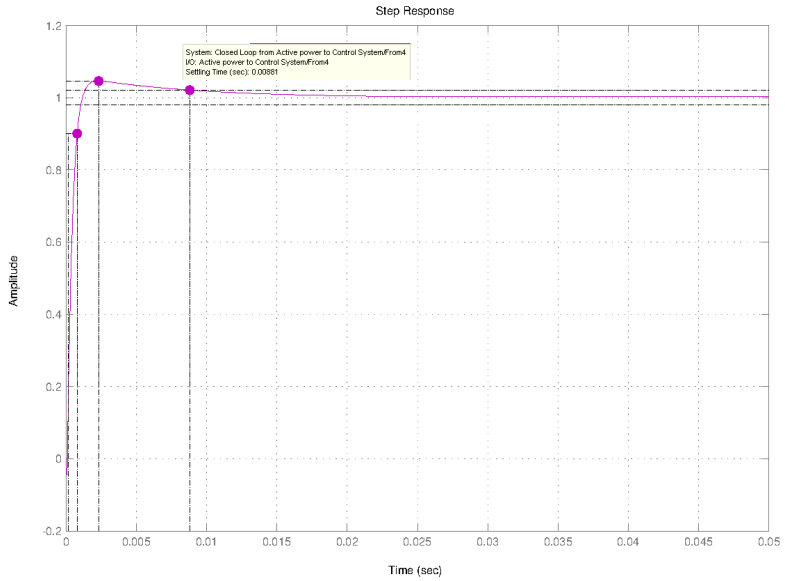

Figure 2.14 Step response of the PI current control loop.

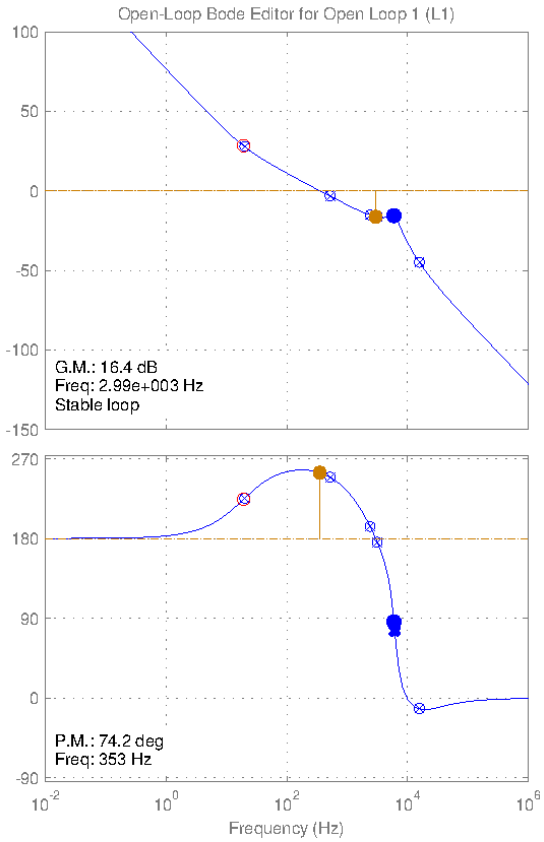

Figure 2.15 Open-loop Bode plot of the PI current control.

Unless there is battery backup in the system, the system cannot work on the principle of maximum power extraction from the source since this would lead to a sustained power imbalance. In stand-alone operation, the power transfer is dedicated primarily by the needs of the local loads. This section will translate the control of the grid-imposed frequency VSI system into the control of inverter output voltage and frequency, the system is shown on Figure 2.16.

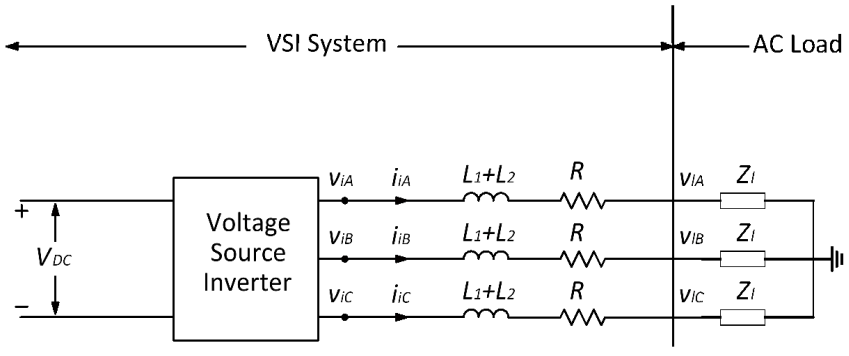

Figure 2.16 VSI in stand alone mode.

Typical situations when a controlled-frequency VSI system is encountered include:

- An electronically coupled distributed generation (PV/Wind/Fuel Cell) or distributed energy storage unit that supplies a dedicated load, or a cluster of loads, under islanded (off-grid) condition;
- An uninterruptible power supply (UPS) system that adopts a VSI system to regulate the frequency and voltage of a sensitive load, for example under emergency conditions.

The voltage and frequency of the AC side is set by the inverter. One of the attractive methods used is presented in [40]. The inverter output voltage is controlled by a PI compensator. The output of the compensator adjusts modulation index of the $60\,Hz$ sine SPWM. This type of control provides stable output in the steady state but transients performance may not be adequate for aggressive load transients [41], such as starting compressor-drive loads. Figure 2.17 shows the block diagram for the voltage control of the stand alone inverters.

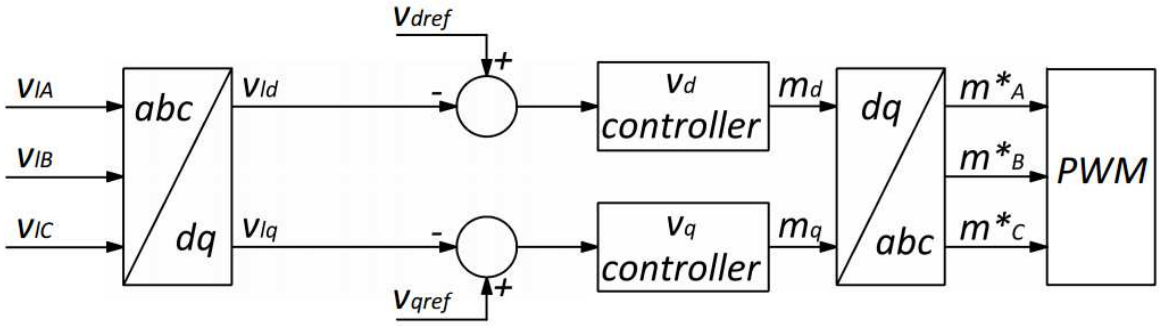

Figure 2.17 Inverter output voltage controller.

Figure 2.17 shows a dq frame model for the controlled-frequency VSI system that does not require prior knowledge of the load model. This system was tuned using Matlab Simulink, SISO toolbox.

The Bode plot of the open-loop voltage control is depicted in Figure 2.19. The step response is plotted in Figure 2.18. It can be seen that for continuous control system settling time of 0.00244s. is obtained.

The main principle of the operation for such system is very similar to the PLL system philosophy, i.e. there are two different signals V_d and V_q responsible for the voltage magnitude and phase shift respectively. In this particular system, the voltage V_d will be regulated near magnitude $170\,V$ and V_q near 0.

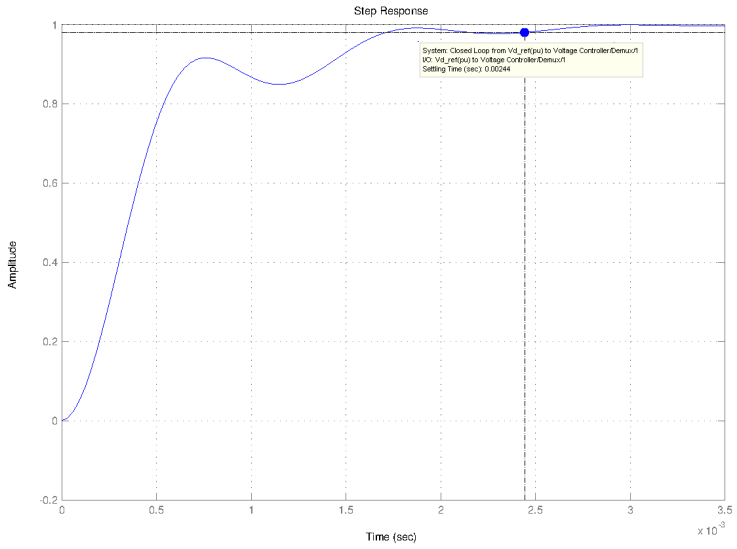

Figure 2.18 Step response of the PI voltage control loop.

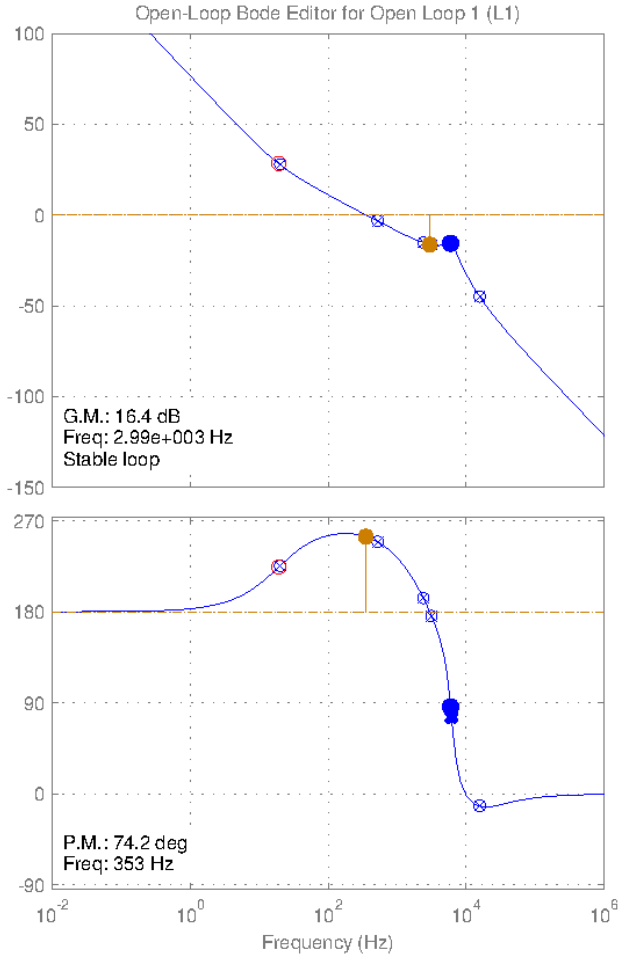

Figure 2.19 Open-loop Bode plot of the PI voltage control.

2.5 Grid Interconnection Requirements

When studying the grid compatibility of a device, the following issues need to be addressed: average and maximum power produced, reactive power level, grid short circuit current (weak or stiff grid conditions), voltage fluctuations, synchronization with the grid, and harmonics. The Table 2.1 shows the required interconnection standards for distributed energy resources.

Table 2.1 Interconnection standards.

	Requirements
Voltage regulation	Maintain service voltage within ANSI C84 Range A (+/-5%)
Voltage control	Not permitted (IEEE 1547)
Flicker	Maximum Borderline of Irritation Curve (IEEE 1543)
Harmonics	<5% THD; <4% below 11th; <2% for 11th – 15th, <1.5% for 17th– 21st; 0.6% for 23rd – 33rd; <0.3% for 33rd and up (IEEE 519)
Power factor	Output power factor 0.85 lead/lag or higher(equipment typically designed for unity power factor)
Direct current injection	<0.5% current of full rated RMS output current (IEEE 1547)
Synchronization and protection	Dedicated protection & synchronization equipment required, except smaller system with utility-interactive inverters
Safety	NFPA NEC, IEEE NESC

2.5.1 Anti-Islanding

Islanding can be defined as the continued operation of a distributed generation unit while the grid are tripped due to fault conditions or for maintenance purposes [42]. Unintentional islanding of the inverter system is not desirable because it can damage equipment which remains connected to the inverter, and it can lead to dangerous situations since the grid may be assumed de-energized. It is also a problem if the supply system is reconnected, because then inverter system is likely to be out of phase and large currents can be injected into inverter system.

A non-islanding inverter is defined as an inverter that ceases to operate a certain time after an islanding situation has occurred. In order to detect the islanding situation, different algorithms can be implemented in the inverter control. In [43] these algorithms are divided into two major groups: remotely controlled (communication based) and locally built-in detection schemes. In this project inverter is locally controlled, so the communication based detection schemes are of no interest. The local detection schemes

can be further divided into two groups, active and passive. Table 2.2 shows the clearing time IEEE 1547 standard for distributed generation less than 30 kW [4].

Table 2.2 IEEE 1547 voltage and frequency requirements.

Parameter	Limit(% of pu)	Clearing time
V	$88 \leq V \leq 110$	Operating range
	$V \leq 50$	0.16s
	$50 \leq V \leq 88$	2s
	$110 \leq V \leq 120$	1s
	$V \geq 120$	0.16s
f	$59.3 \leq f \leq 60.5$	Operating range
	$f \leq 59.3$	0.16s
	$f \geq 60.5$	0.16s

2.5.1.1 Passive Detection

The passive methods are based on local measurements, and most common methods are:

- Frequency limitations:
  - Magnitude change;
  - Rate of change;
  - Phase shift;
- Voltage variations
- Power
  - Change of active power
  - Change of reactive power
  - Power factor (P/Q) index
- Harmonic content changes

These methods are usually easy to implement and they work without affecting the stability of the system and power quality, unless the limits are too strict and inverter trips without being on islanded mode. One of main limitations with these methods is that each of the methods have operating region where they are not able to detect an islanding situation within given limits. The region is called the non-detection zone (NDZ). The impact of these zones can be very important, especially during the balanced

load conditions, when the load matches the power produced by the inverter [44]. Combinations of these methods sometime can reduce the NDZ.

2.5.1.2 Active Detection

In these methods disturbances are injected into the supply system in order to detect islanding conditions based on the system response. The most common methods are based on one of the following principles:

- Impedance measurement
- Voltage variation
- Frequency variation
- Output power variation

One of the advantages of these methods is the increased ability to detect islanding even during balanced load conditions, and thus decrease or even remove the NDZ completely. The main disadvantage of active methods, is interference of the disturbances introduced by multiple distributed resources connected to the same grid. Moreover these methods can reduce power quality of the operated inverter. Active methods of islanding detection is area of growing research activity.

2.5.1.3 GE Anti-Islanding concept [44]

The proposed GE anti-islanding schemes are based on two concepts: one is positive feedback, the other is dq implementation. Combining these two concepts leads to a family of new anti-islanding schemes.

2.5.1.4 Voltage Scheme

Figure 2.20 shows one of the voltage feedback schemes, called V_d to I_{dref}. The scheme is implemented with highlighted (red) path - V_d is passed by a band-pass filter (BPF), a gain, and a limiter, and becomes a current variation Δi adding to I_{dref}. There are other ways to implement voltage scheme: from V_d to I_{qref}, from V_q to I_{dref}, V_q to I_{qref}.

There are two critical design criteria for the gain. First, when inverter is grid connected, the gain should be small enough so that system is stable. When islanded, the gain should be large enough so that the islanded system is unstable, otherwise, the system may run into another steady state that may still be within nominal ranges, thus resulting in a NDZ. In this design project a gain of 2 is assumed.

The reason for using band-pass filter (BPF) is to avoid noise injection (low-pass needed) and DC offset (high-pass needed) caused by anti-islanding loop. The noise will cause power quality problems, while DC offset will affect the steady state reference tracking. Because of these two conflicting requirements, an appropriate band with both high-frequency noise and low frequency offset performance must be trade off. Given 2-second anti-islanding protection requirement [4] a 500 to 1000 Hz band bass filter is chosen for design. The limiter function is to specify the maximum allowable current injection. Two factors determine the limiter settings. One is the inverter over-current capability. The other is the maximum allowable power factor, if injecting the current to I_{qref}. Performance of proposed anti-islanding detection scheme will be discussed later in Chapter 3.

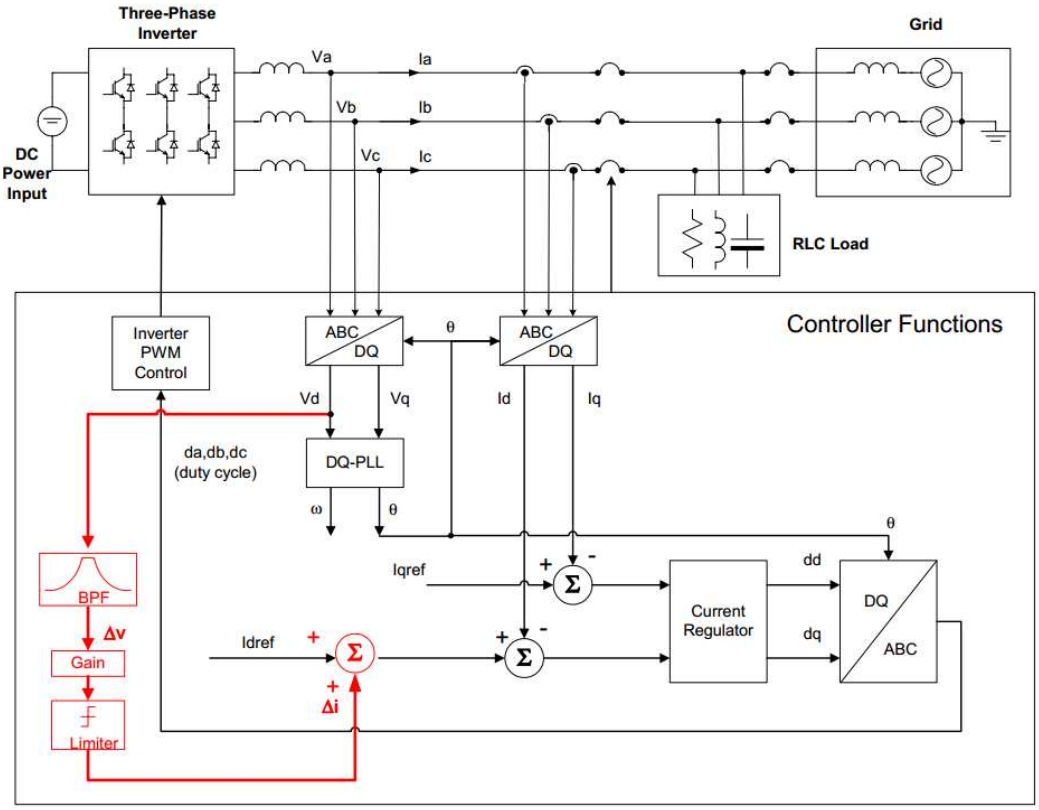

Figure 2.20 Voltage scheme: from V_d to I_{dref}.

2.6 LCL filter Modeling and Design

Some important constraints must be taken in consideration in the design of LCL filters, such as current ripple, filter size, switching ripple attenuation The reactive power variation seen by the grid because of the capacitor may gave a resonance that could lead to unstable operation of the system.

Therefore, passive or active damping is proposed by either adding a resistor in series with capacitor or changing the controller design [45].

A LCL filter is more efficient than a simple inductor (L) because the latter has only attenuation of 20 dB/decade for all the range of frequency [46]. The switching frequency of inverter must be high enough for a correct attenuation of high current harmonics. The higher the switching frequency there are more losses. LC filters suffer from variability of resonance frequency over time like the grid inductance. Therefore, they are not appropriate for a weak grid [47].

2.6.1 Dynamic Analysis of the LCL filter

The following mathematical model can be used for the analysis of a LCL filter [48].The LCL filter per-phase model is shown in Figure 2.21, where L_1 is the inverter-side inductor, L_2 is the grid-side inductor, C_f is the capacitor of LCL filter, R_f is the damping resistor, R_1 and R_2 are inductors resistances, v_i and v_g are inverter input and grid voltages.

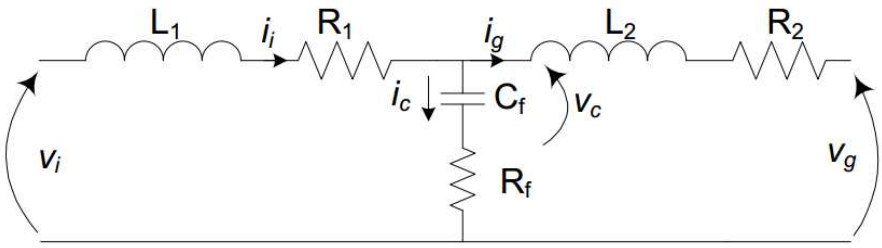

Figure 2.21 LCL filter per phase model.

The currents i_i, i_c, i_g are inverter output current, capacitor current, and grid current, respectively. There are two possible configuration of LCL filter which will be discussed in next sections.

2.6.1.1 Wye Connected Capacitors

The LCL filter state space model with wye connected capacitors is derived from per-phase model as shown on Figure 2.21

$$\begin{cases} \dfrac{dv_c}{dt} = \dfrac{i_i - i_g}{C_f} \\ \dfrac{di_i}{dt} = \dfrac{1}{L_1}\left(v_i - v_c - R_f\left(i_i - i_g\right) - R_1 i_i\right) \\ \dfrac{di_g}{dt} = \dfrac{1}{L_2}\left(v_c + R_f\left(i_i - i_g\right) - v_g - R_2 i_g\right) \end{cases} \tag{2.34}$$

There are no cross couplings between the phases, and thus the equations are equal for all phases. If expressed in matrix form they become Equation (2.35):

$$\begin{bmatrix} \frac{di_i}{dt} \\ \frac{di_g}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_1+R_f}{L_1} & \frac{R_f}{L_1} & -\frac{1}{L_1} \\ \frac{R_f}{L_2} & -\frac{R_2+R_f}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_g \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & -\frac{1}{L_2} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_i \\ v_g \end{bmatrix} \tag{2.35}$$

2.6.1.2 Delta Connected Capacitors

A LCL filter with delta connected capacitors can be analyzed in the abc stationary frame with the circuit of Figure 2.22. Voltages and currents can be formulated as in Equations (2.36) and (2.37):

$$v_{AB} + v_{BC} + v_{CA} = 0 \tag{2.36}$$

$$\frac{dV_{AB}}{dt} = \frac{1}{3C_f} i_{iAB} - \frac{1}{3C_f} i_{gAB} \tag{2.37}$$

where $i_{iAB} = i_{iA} - i_{iB}$ and $i_{gAB} = i_{gA} - i_{gB}$.

Equation (2.36) is the voltage balance around the capacitor bank, and the load side equations are supported by Equations (2.38), (2.39) with corresponding matrix form in Equation (2.40).

$$\frac{di_{iAB}}{dt} = -\frac{v_{AB}}{L_1} + \frac{v_{iAB}}{L_1} - \frac{i_{iAB}R_1}{L_1} \tag{2.38}$$

$$\frac{di_{gAB}}{dt} = -\frac{R_2}{L_2} i_{gAB} + \frac{1}{L_2} v_{AB} - \frac{1}{L_2} v_{gAB} \tag{2.39}$$

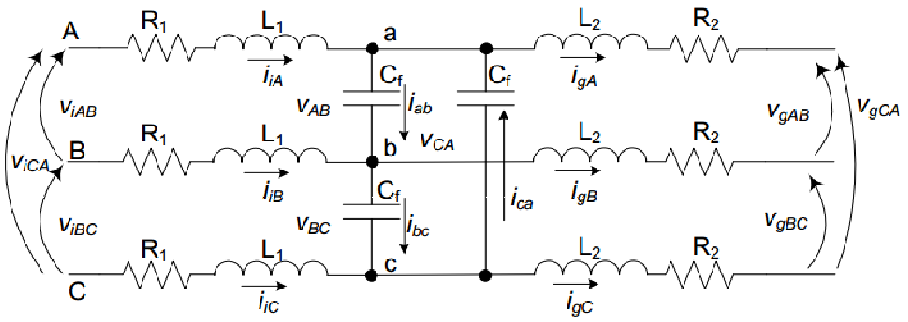

Figure 2.22 LCL filter with delta connected capacitors.

$$\begin{cases} \dfrac{dv_c}{dt} = \dfrac{1}{3C_f} i_i - \dfrac{1}{3C_f} i_g \\ \dfrac{di_i}{dt} = \dfrac{1}{L_1}\left(v_i - v_c - R_f\left(i_i - i_g\right) - R_1 i_i\right) \\ \dfrac{di_g}{dt} = \dfrac{1}{L_2}\left(v_c + R_f\left(i_i - i_g\right) - v_g - R_2 i_g\right) \end{cases} \tag{2.40}$$

where $v_c = [v_{AB} v_{BC} v_{CA}]^T, i_i = [i_{iAB} i_{iBC} i_{iCA}]^T,\ v_i = [v_{iAB} v_{iBC} v_{iCA}]^T,$

$i_g = [i_{gAB} i_{gBC} i_{gCA}]^T.$

Finally, the plant model as a continuous state-space equation:

where

$$A = \begin{bmatrix} 0_{3x3} & \dfrac{1}{3C_f} I_{3x3} & -\dfrac{1}{3C_f} I_{3x3} \\ -\dfrac{1}{L_1} I_{3x3} & -\dfrac{R_1 + R_f}{L_1} I_{3x3} & \dfrac{R_f}{L_1} I_{3x3} \\ \dfrac{1}{L_2} I_{3x3} & 0_{3x3} & -\dfrac{R}{L_2} I_{3x3} \end{bmatrix}_{9x9} \tag{2.41}$$

$$B = \begin{bmatrix} 0_{3x3} \\ \dfrac{1}{L_1} I_{3x3} \\ -\dfrac{1}{L_2} I_{3x3} \end{bmatrix}_{9x3} \tag{2.42}$$

$$u = \begin{bmatrix} V_i \\ V_g \end{bmatrix}_{9x1} \tag{2.43}$$

$$X = \begin{bmatrix} V_c \\ I_i \\ I_g \end{bmatrix}_{9x1} \tag{2.44}$$

2.6.1.3 Frequency Response and Transfer Function

From the developed mathematical models, transfer functions of LCL filter can be derived. Transfer functions are derived based on the three phase differential equations derived earlier, but in these equations the inductors resistances are not considered. One of the extracted transfer function from derived state space equations is $H_{LCL} = \frac{i_g}{v_i}$. The grid voltage is assumed to be an ideal voltage source and it represents a short circuit for harmonic frequencies, and for the filter analysis is set to zero: $v_g = 0$. So, the transfer function of LCL filter without damping is:

$$H_{LCL}(s) = \frac{1}{L_1 C_f L_2 s^3 + (L_1 + L_2)s} \tag{2.45}$$

and for damped filter:

$$Hd_{LCL}(s) = \frac{C_f R_f s + 1}{L_1 C_f L_2 s^3 + C_f (L_1 + L_2) R_f s^2 + (L_1 + L_2)s} \tag{2.46}$$

The Bode plots of LCL filter without and with damping are shown in Figure 2.23.

2.6.1 Design Procedure

In this study, the filter design approach has been explained step-by-step and if correctly damped, it is possible to avoid resonance problems passively [49] or actively [46]. The procedure for choosing the LCL filter parameters requires the power rating of the converter, the grid frequency, and the switching frequency as inputs. Algorithm of LCL filter design is shown in Figure 2.24, each step of which will be described in following sections and will be supported by filter design example.

The following parameters are needed for the filter design: V_{LL} - line to line RMS voltage (inverter output), V_{ph}-phase voltage (inverter output), P_n - rated active power, V_{DC} - DC bus voltage, f_g-grid frequency, f_{sw}-switching frequency, f_{res}-resonance frequency.

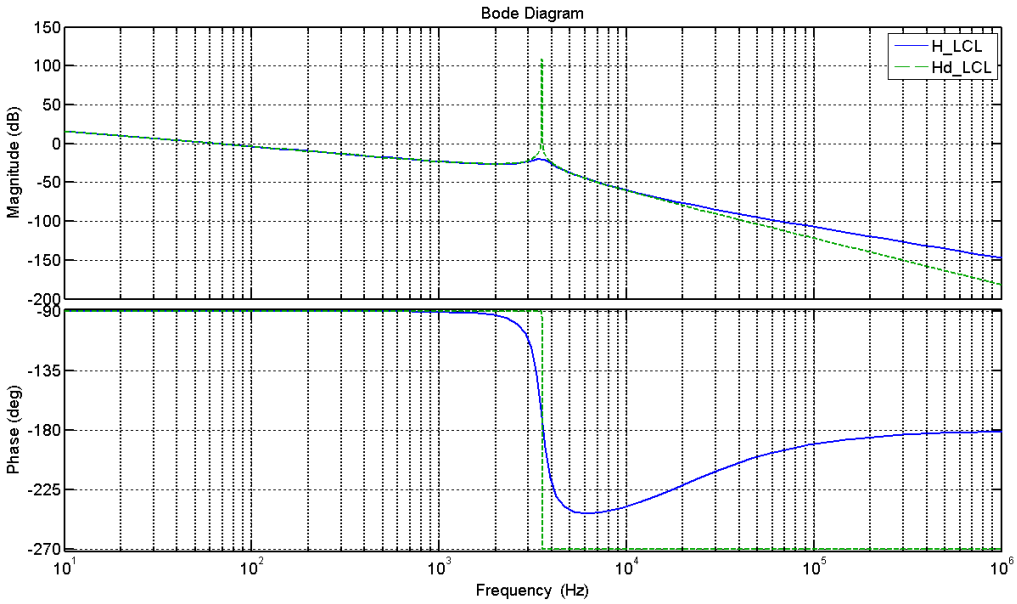

Figure 2.23 Bode diagram for damped and undamped LCL filter.

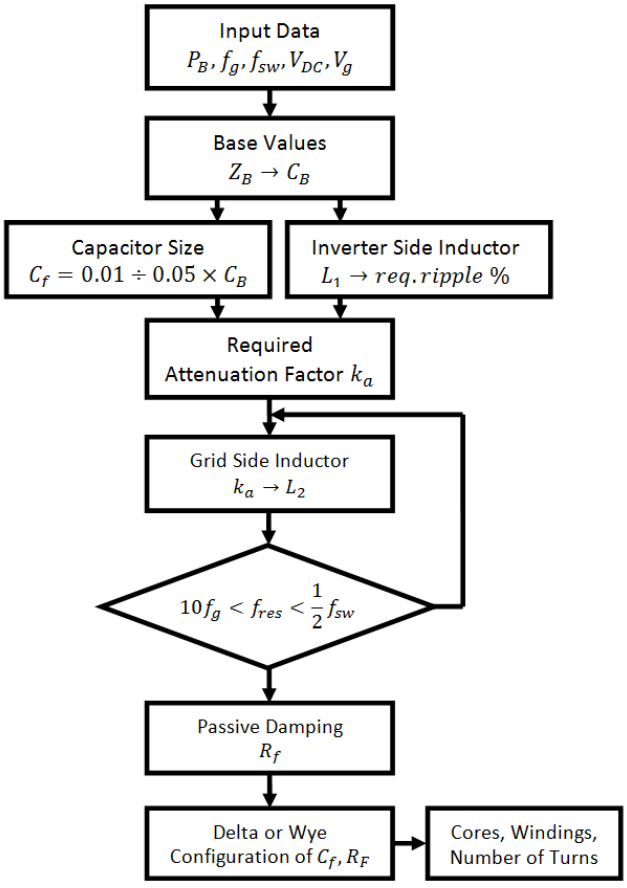

Figure 2.24 LCL filter design algorithm.

The base impedance and base capacitance are defined by Equations (2.47) and (2.48). Thus, the filter values will be referred in % of the base values:

$$Z_b = \frac{V_{LL}^2}{P_n} \tag{2.47}$$

$$C_b = \frac{1}{\omega_n Z_b} \tag{2.48}$$

For the design of the filter capacitance, it is considered that the maximum power factor variation seen by the grid is 5%, as it is multiplied by the value of base impedance of the system: $C_f = 0.05C_b$. It is important to notice that factors higher than 5% can be used, since they will compensate the inductive reactance of the inductors on the filter and therefore the influence at the power factor of the system will be lesser than expected. The maximum current ripple at the output of DC/AC inverter is [50]:

$$\Delta I_{Lmax} = \frac{2V_{DC}}{3L_1}(1-m)mT_{sw} \tag{2.49}$$

where, m - modulation factor.

It can be observed that maximum peak to peak current ripple happens at $m = 0.5$, then

$$\Delta I_{Lmax} = \frac{V_{DC}}{6f_{sw}L_1} \tag{2.50}$$

where L_1 is inverter side inductor. A 10% ripple of the rated current for the design parameters is given by:

$$\Delta I_{Lmax} = 0.1I_{max} \tag{2.51}$$

where

$$I_{max} = \frac{P_n\sqrt{2}}{3V_{ph}} \tag{2.52}$$

$$L_1 = \frac{V_{DC}}{6f_{sw}\Delta I_{Lmax}} \tag{2.53}$$

The main objective of the LCL filter design is in fact to reduce the expected 10% current ripple limit to 20% of its own value, resulting in a ripple value of 2% of the output current [49], [5]. In order to

calculate the ripple reduction, the LCL filter equivalent circuit is firstly analyzed considering the inverter as a current source for each harmonic frequency, see Figure 2.21.

Equations (2.54) and (2.55) give the relation between the harmonic current generated by the inverter and the once injected in the grid:

$$\frac{i_g(h)}{i_i(h)} = \frac{1}{|1 + r[1 - L_1 C_b \omega_{sw}^2 x]|} = k_a \tag{2.54}$$

or

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f w_{sw}^2} \tag{2.55}$$

where, k_a is desired attenuation. $C_f = 0.01 \div 0.05 C_b$.

The constant r is defined as the relation between the inductance at the inverter side and the one at the grid side:

$$L_2 = r L_1 \tag{2.56}$$

Plotting for different values of rone can help to evaluate the transfer function of the filter at a particular resonant frequency that depends on the nominal grid impedance [51]. A resistor in series (R_f) with the capacitor attenuates part of the ripple on the switching frequency in order to avoid the resonance. The value of this resistor should be one third of the impedance of the filter capacitor at the resonant frequency [52] and the resistor in series with the filter capacitance is given by Equation (2.59).

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{2.57}$$

$$10 f_g < f_{res} < 0.5 f_{sw} \tag{2.58}$$

It is necessary to check resonant frequency to satisfy Equation (2.58). If it does not, the parameters should be re-chosen.

$$R_f = \frac{1}{3 \omega_{res} C_f} \tag{2.59}$$

2.6.1.1 Delta and Wye Configurations

After defining all parameters for LCL filter two configuration are possible for implementation. Parameters defined in Section A are valid for wye capacitors connection, however using simple and well known wye delta transformation for balanced system wye configuration can be transformed to delta:

$$Z_{AB} = \frac{Z_A}{3} \tag{2.60}$$

It is evident from Equation (2.60), that for delta configuration size of capacitor should be three times smaller than for wye configuration and vice versa for damping resistance:

$$R_{f_\Delta} = 3R_{f_Y} \tag{2.61}$$

$$C_{f_\Delta} = \frac{C_{f_Y}}{3} \tag{2.62}$$

It is a common practice to ground neutral, or central point of wye connection [53]. In most cases, this grounding is required by the U.S. National Electric Code (NFPA-70). By grounding a wye system, the voltages to ground are stabilized and controlled. This makes system much less susceptible to impulses, and faults that cause high voltages to ground. In case of delta configuration there are no questions and problems with grounding. That's why author's propose delta connection as more convenient and less questionable way to get same good performance of LCL filter.

2.6.1.2 LCL Filter Design

A step-by-step procedure to obtain parameters of the filter with wye configuration considering the following given data, needed for the filter design: $V_{LL} = 120\sqrt{3}\,V$ - line to line RMS voltage, $P_B = P_n = 5\,kW$- rated active power,$V_{DC} = 400\,V$- DC bus voltage,$\omega_n = 2\pi 60$-grid frequency, $\omega_{sw} = 15kHz$ - switching frequency, $x = 0.05$ - maximum power factor variation seen by the grid, $k_a = 0.2$ (20%) - attenuation factor is done. Therefore, the base impedance and the base capacitance are $Z_B = 8.64\Omega$, $C_B = 307\mu F$ respectively (parameters are shown in Table 2.3).

1. Using 10% allowed ripple Equation (2.53) gives inductance $L_1 = 2.23mH$.

2. Maximum capacitor value is $16.63\mu F$ to be in limit of 5% of the base value C_B. After round to closest possible value $C_f = 15\mu F$ for wye configuration or 5μF for delta connection.

3. Setting desired attenuation $k_a = 20\%$ and using Equation (2.55) L_2 is calculated to be $0.045mH$.

4. Putting all calculated parameters from (1)-(3) to Equation (2.57) gives $f_{res} = 6450kHz$ which is meets condition from Equation (2.58).

5. Equation (2.59) gives value of damping resistance $R_f = 0.55\Omega$ for wye configuration or 1.65Ω for delta connection.

Table 2.3 Summarized parameters

f_g	Grid frequency	*60Hz*
f_{sw}	PWM carrier frequency	*15kHz*
P_n	Nominal Power	*5kW*
V_g	Phase grid voltage	*120V*
V_{DC}	DC link Voltage	*400V*
L_1	Inverter side inductor	*2.33mH*
L_2	Grid side inductor	*0.045mH*
C_f	Capacitor filter Y/Δ	*15μF/5μF*
R_f	Damping Resistor Y/Δ	*0.55Ω/1.65Ω*

2.7 Conclusion

This chapter provided a full overview and theoretical description of proposed system. It has also provided descriptive controller design, LCL filter design procedure and islanding detection methodology which are used for practical implementation and evaluation in next chapter.

CHAPTER 3

SIMULATION STUDIES

3.1 Objective

This chapter shows different scenarios that have been studied in order to support a simulation based design of an inverter system capable to operate in stand-alone and in grid-connected modes using Matlab/Simulink platform. It is composed of four sections: the first and second ones contain case studies that support the control design and the LCL filter simulation performance evaluations for the standalone mode and grid connected mode operation. The third part contains simulation for ride-through operation, and the system response when the inverter transits to standalone from grid connected mode. The last section contains further results evaluation and discussions.

3.2 Stand Alone Mode Operation

The block diagram of the simulated system is shown on Figure 3.1. The system was built using Power Systems Toolbox in Simulink. The total harmonic distortion (THD) analysis was done with Power Systems Toolbox. Figure 3.2 shows a voltage closed loop controller block diagram that was implemented for the inverter.

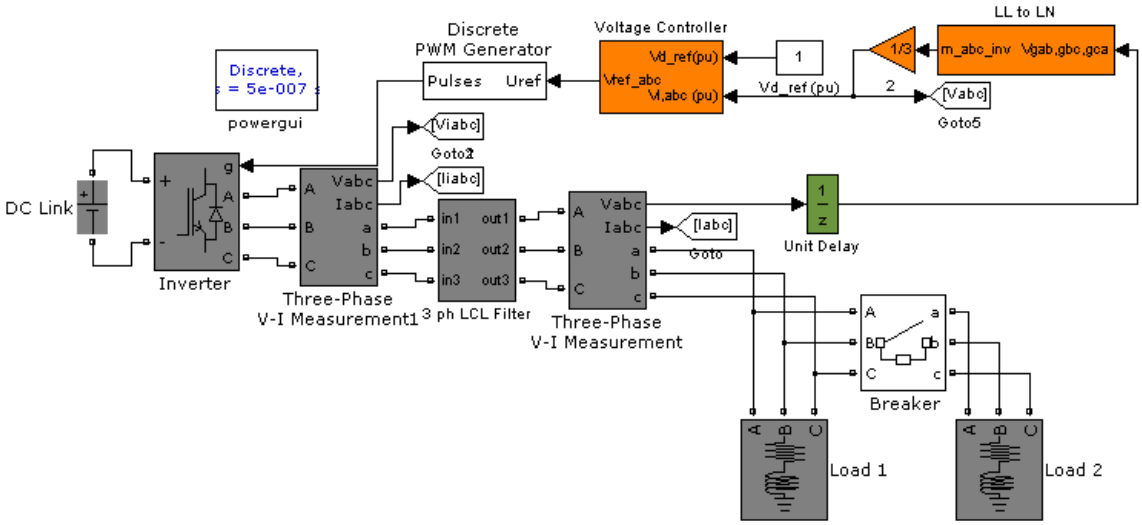

Figure 3.1 Simulink model of stand-alone inverter with load.

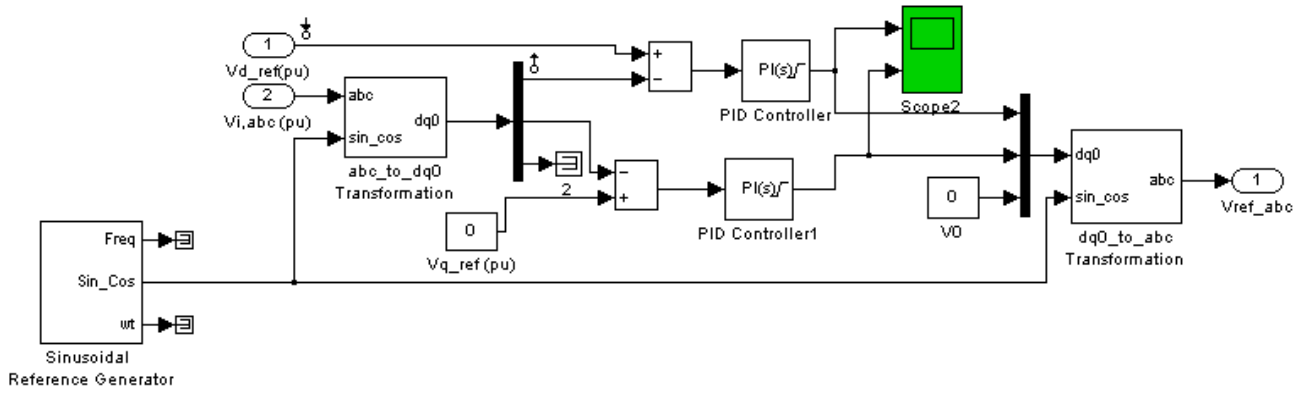

Figure 3.2 Simulink block diagram of implemented voltage controller.

3.2.1 Case 1: Active Load

A resistive load has been connected in order to provide 5000 W active load. The phase voltage v_A and line current i_A (both in p.u.) are shown on Figure 3.3.

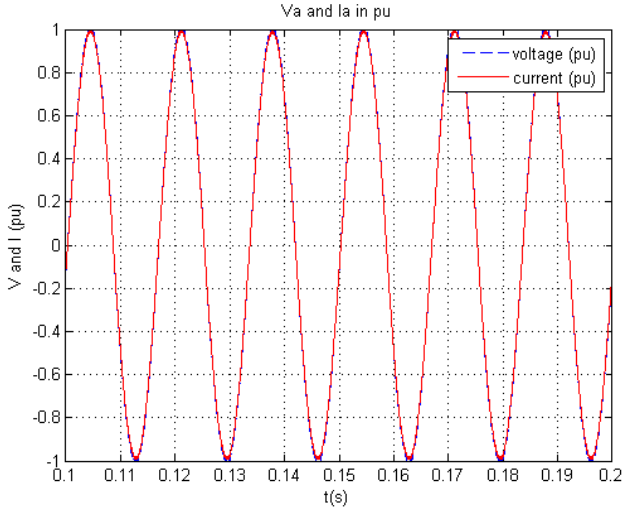

Figure 3.3 Phase voltage and line current measured at load terminals.

The inverter output voltage $v_{iA}(V)$ (just before the LCL filter) is depicted in Figure 3.4 (a); it has THD of 43.85% as indicated in Figure 3.5. The filtered phase voltage and line current can be seen on Figure 3.3 and Figure 3.4. The harmonic analysis of line current is shown on Figure 3.6 with THD of 0.88%.

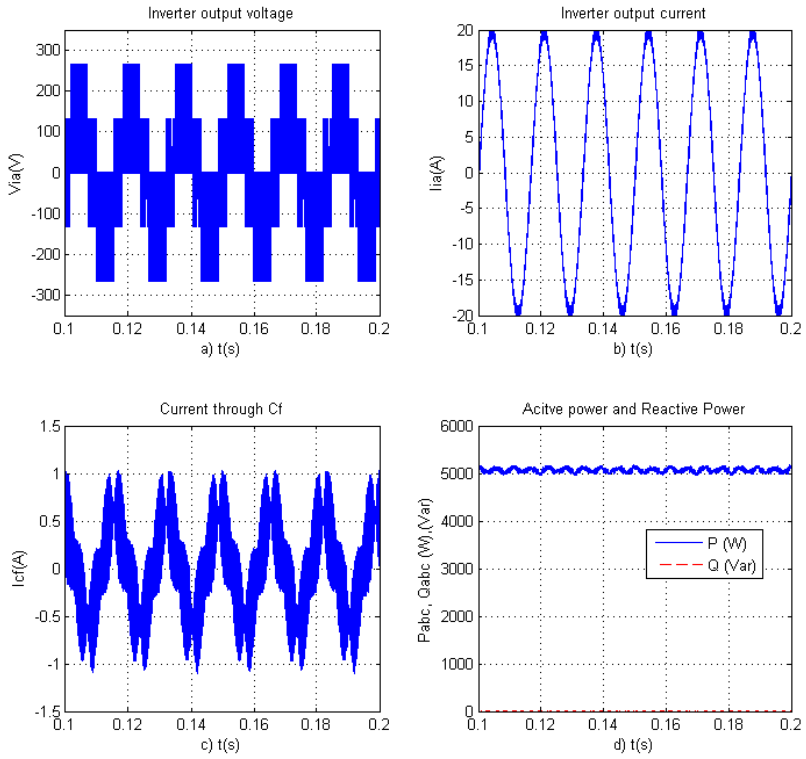

Figure 3.4 (a) Inverter output voltage; (b) Inverter output current; (c) Current through filter capacitor C_f; (d) Active and reactive power output.

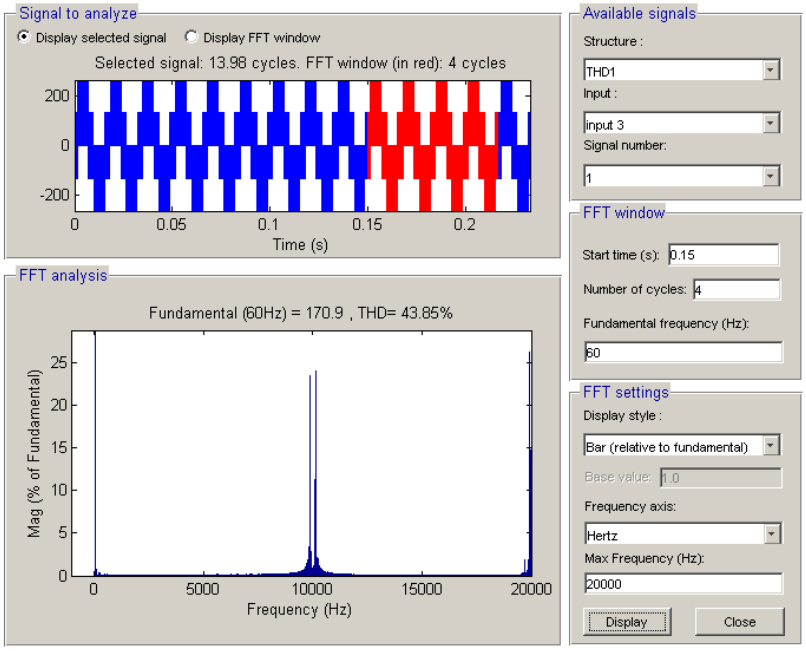

Figure 3.5 THD of inverter output phase voltage.

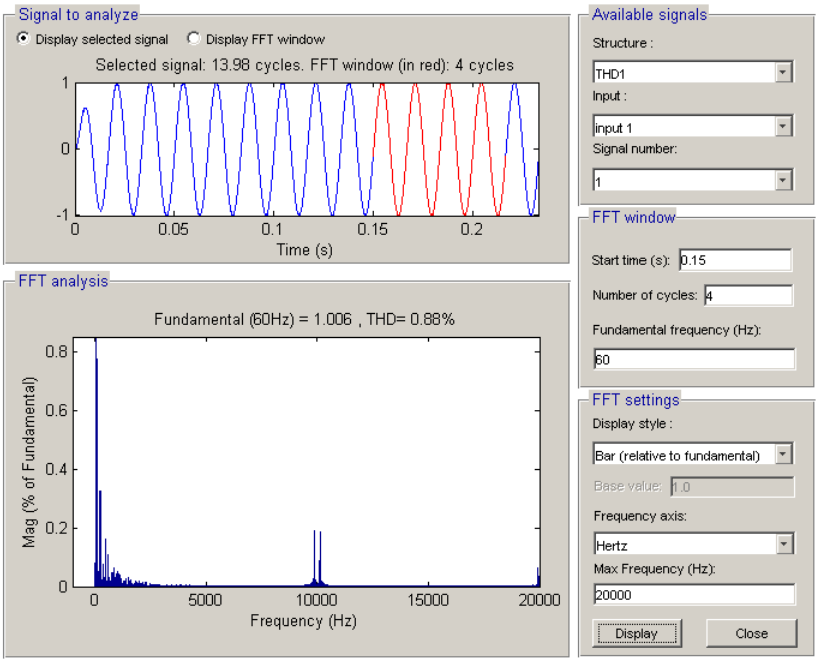

Figure 3.6 THD of line current at load terminals.

3.2.2 Case 2: Load with Lagging Power Factor

The inverter is providing 3000 W (active power) and 2000 Var reactive power for the load. Phase voltage v_A and line current i_A (in p.u.) are shown on Figure 3.3.

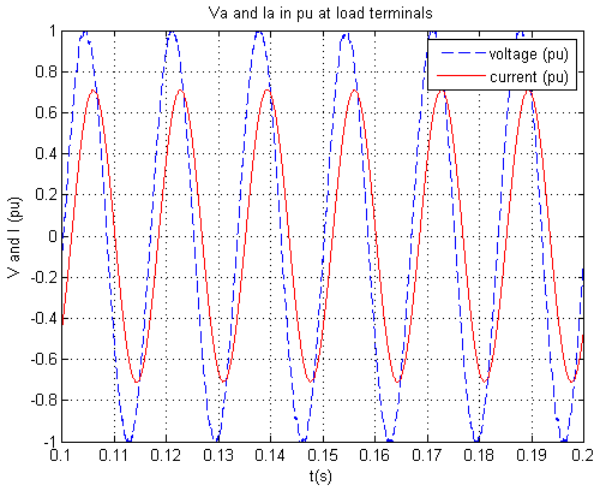

Figure 3.7 Phase voltage and line current measured at load terminals.

The inverter output voltage $v_{iA}(V)$ just before the LCL filter is seen in Figure 3.8 (a), where the THD is 41.87% (Figure 3.9). The filtered phase voltage and line current can be seen on Figure 3.7 and Figure 3.8, with harmonic analysis of line current shown on Figure 3.10 with THD of 1.27%.

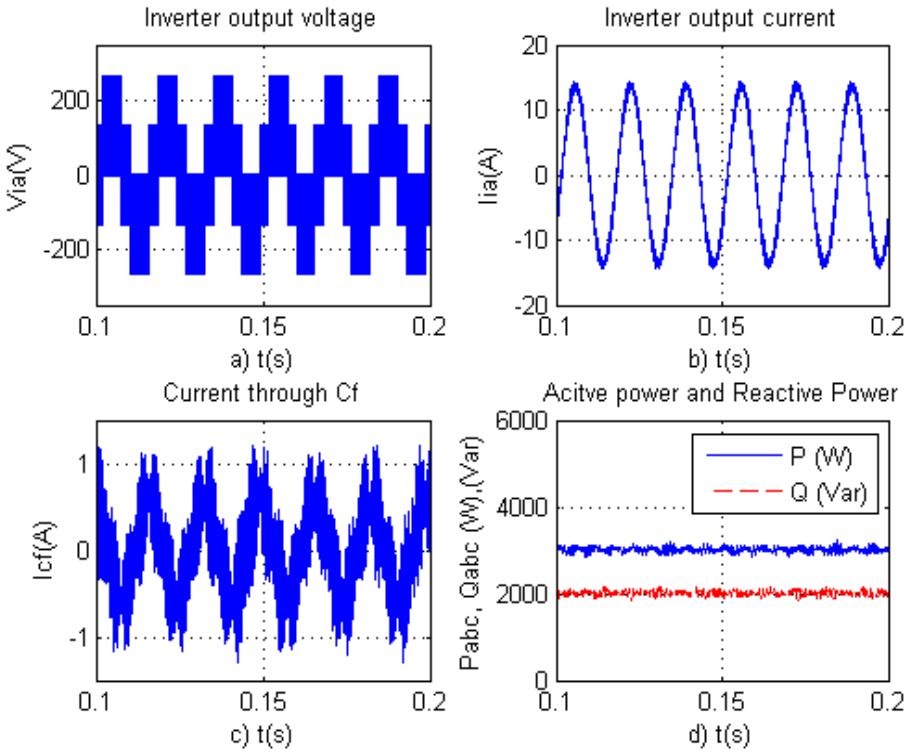

Figure 3.8 (a) Inverter output voltage; (b) Inverter output current; (c) Current through filter capacitor C_f; (d) Active and reactive power output.

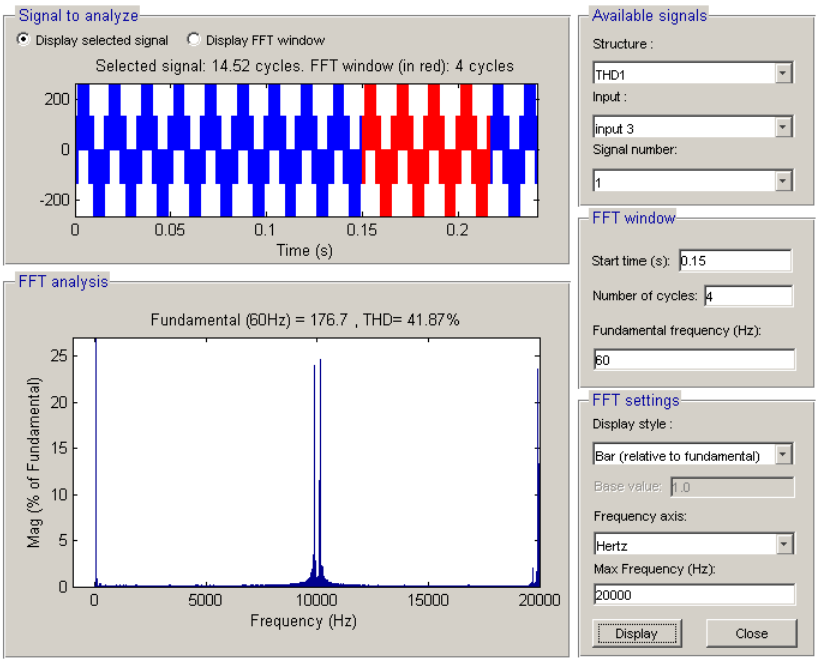

Figure 3.9 THD of inverter output phase voltage.

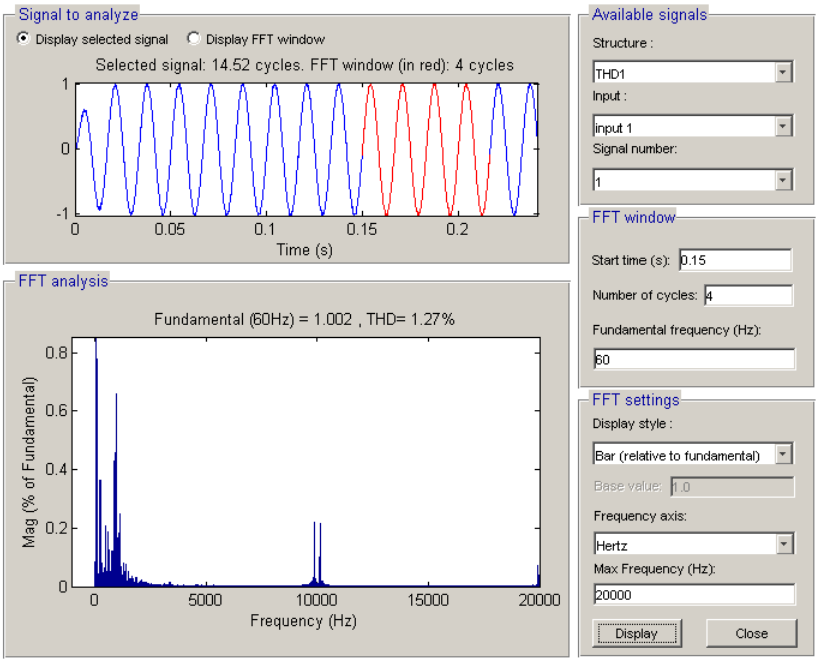

Figure 3.10 THD of line current at load terminals.

3.2.3 Case 3: Step Change in Load

The inverter is imposed a load step change, where initially it has 2000 W and 500 Var, and at time 0.15 sec. there is a step change to 4000 W and 1500 Var. The phase voltage v_A and line current i_A (in p.u.) are shown on Figure 3.11.

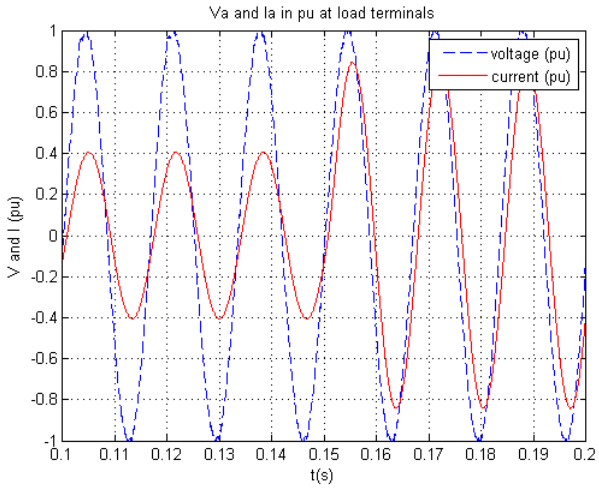

Figure 3.11 Phase voltage and line current measured at load terminals.

The inverter output voltage $v_{iA}(V)$, just before the LCL filter is seen in Figure 3.12 (a); the filtered phase voltage and line current are depicted on Figure 3.11 and Figure 3.12. Such load step change made the system PI controllers to react as seen on Figure 3.13, where the measured d and q components of voltage and errors are plotted. The figure shows a very good performance response with immediate settling time.

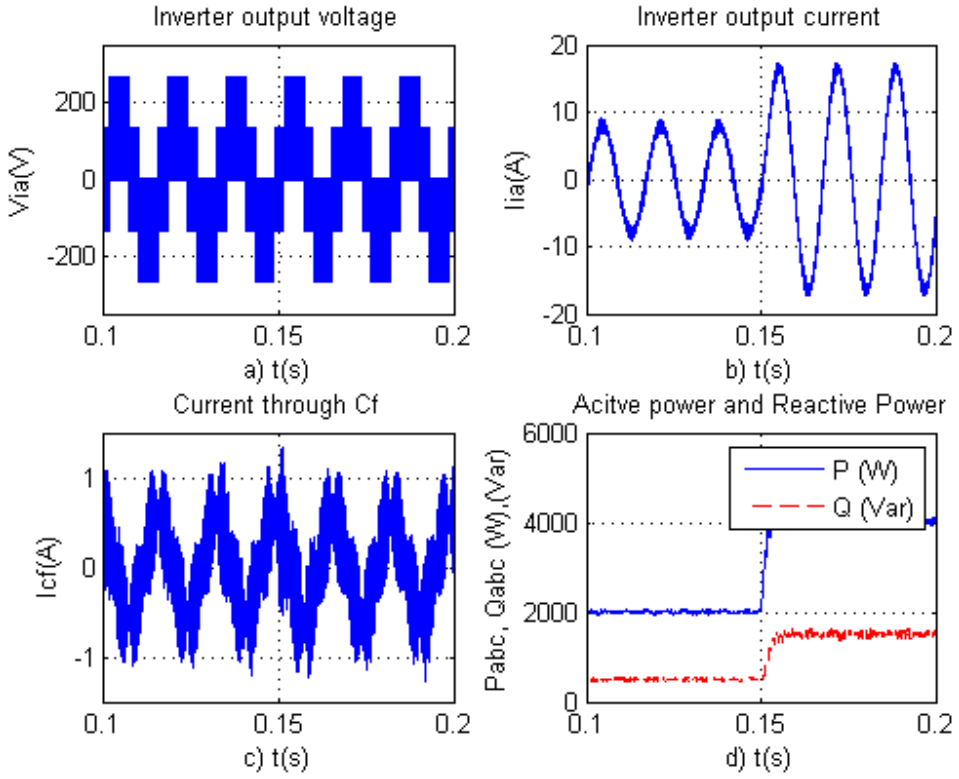

Figure 3.12 (a) Inverter output voltage; (b) Inverter output current; (c) Current through filter capacitor C_f; (d) Active and reactive power output.

3.2.4 Case 4: Stand Alone Mode in Fault Conditions

There different faults have been considered, one phase ground fault, two-phases ground fault and three-phases ground fault. The scenario is important to simulate in order to specify system protection devices. The inverter is providing half of nominal active power 2500 W and during the operation those different faults occur at time step 0.15s.: (i) ground fault of phase A (Figure 3.14), (ii) phase A and B ground fault (Figure 3.15); (iii) three phase ground fault (Figure 3.16).

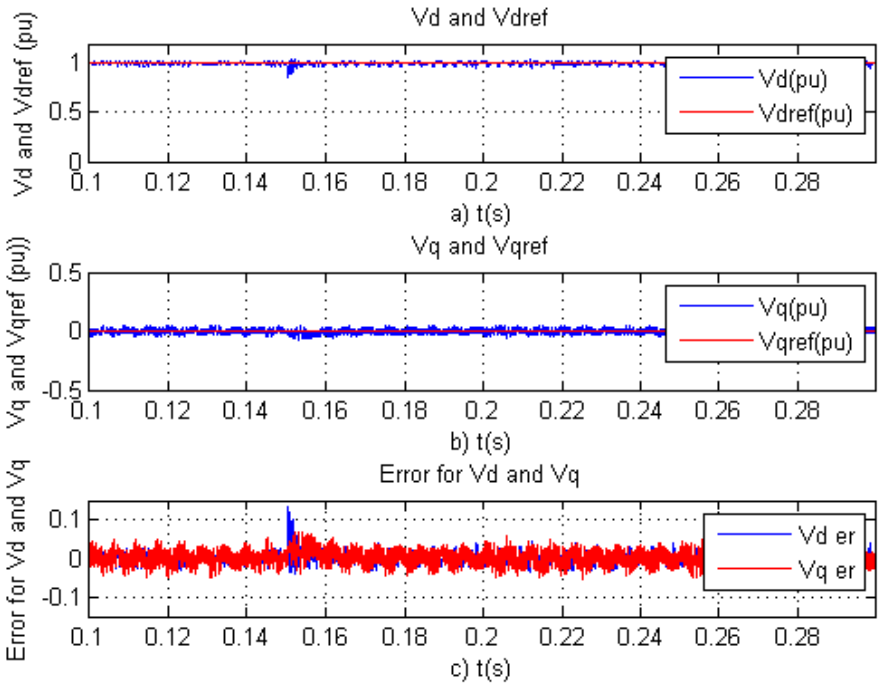

Figure 3.13 (a) V_d and V_{dref}; (b) V_q and V_{qref}; (c) V_d and V_q error.

This simulation study allows the sizing of inverter relay protection, as well as inverter built-in protection (described in Chapter 4). The systems implemented in the experimental work is operating with the Semikron provided board protection. However, for future deployment and retrofit, it might be necessary additional over current and undervoltage protection devices.

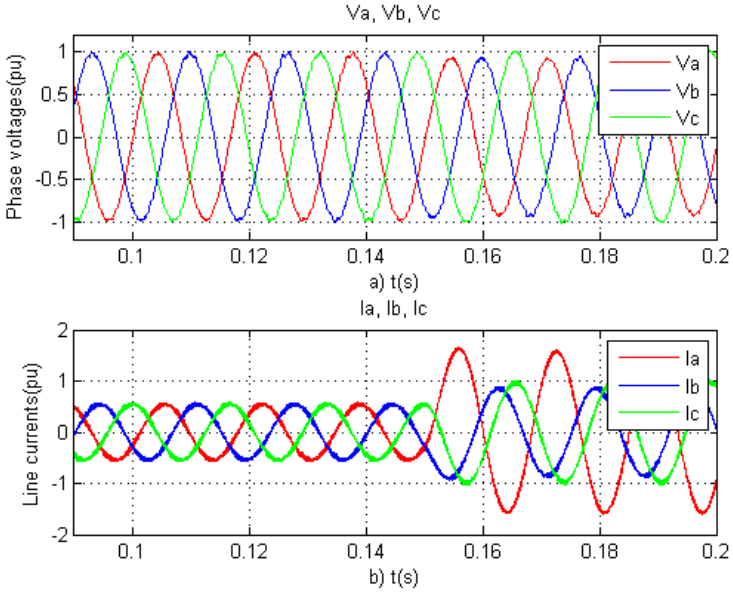

Figure 3.14 (a) Phase voltages at single phase fault conditions; (b) Line currents during single phase fault.

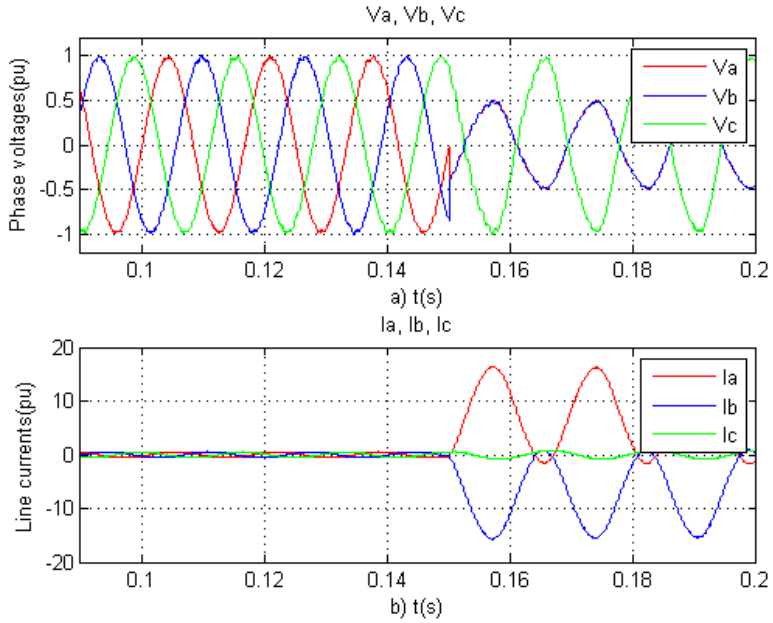

Figure 3.15 Phase voltages and line currents during two phase ground fault.

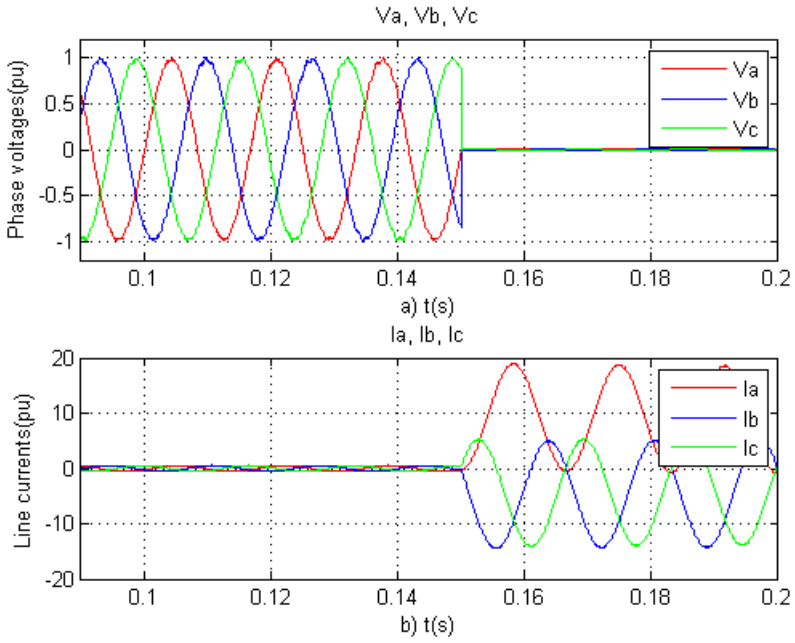

Figure 3.16 Phase voltages and line currents during three phase ground fault.

3.3 Grid Connected Mode

When the inverter is connected to the grid, capable of providing active and reactive power the system must behave in current-controlled mode.

The simulated system is shown on Figure 3.17. The implemented current control system is depicted on Figure 3.18.

Many case studies have been considered for active power injection to the grid, mixed power injection and also when the inverter takes power from the grid (for example in charging a battery in the dc-link). All those cases have been thoroughly simulated in order to observe system behavior and performance.

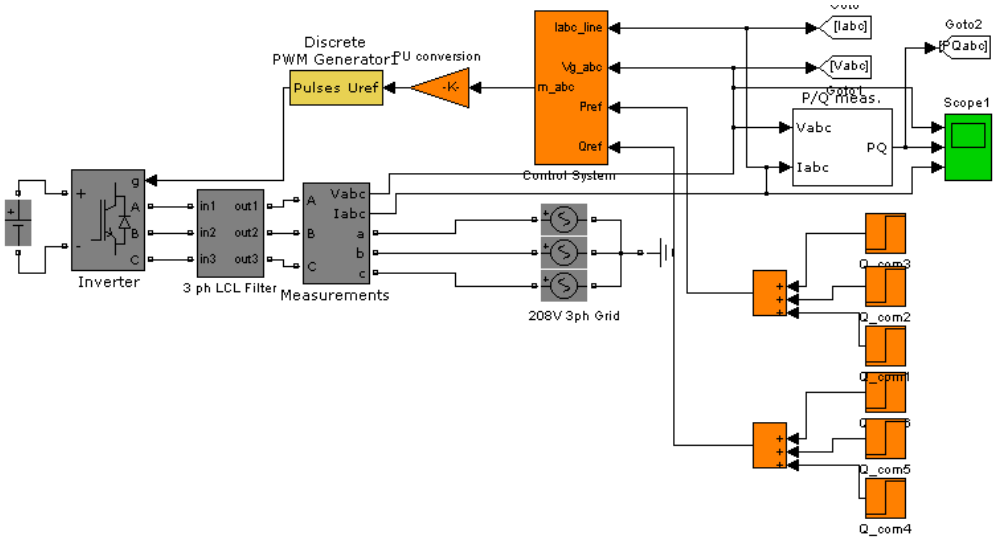

Figure 3.17 Simulink model of grid connected inverter.

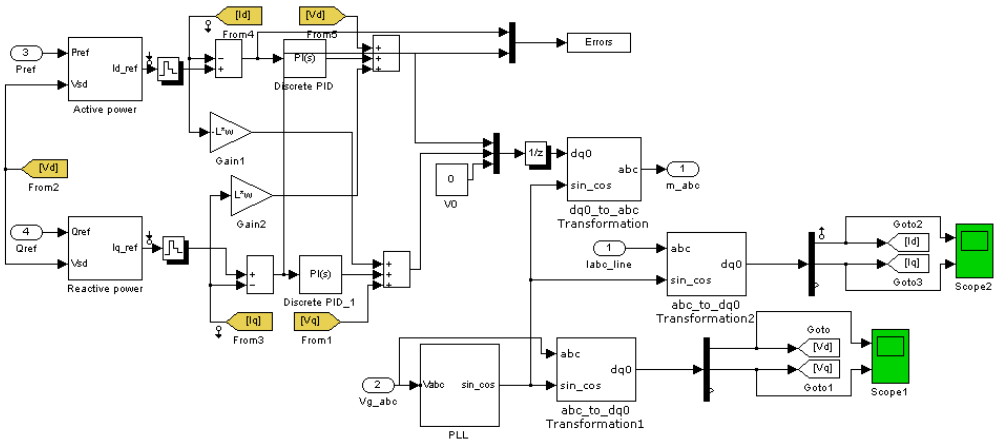

Figure 3.18 Simulink block diagram of implemented current controller

3.3.1 Power Injection to the Grid

The active power reference has been varied in three steps and the reactive power reference in two steps. In this simulation study inverter originally is providing 1500 W and 0 Var to the utility grid at nominal voltage.

Figure 3.19 shows phase voltage v_A and line current i_A, all values are in p.u..

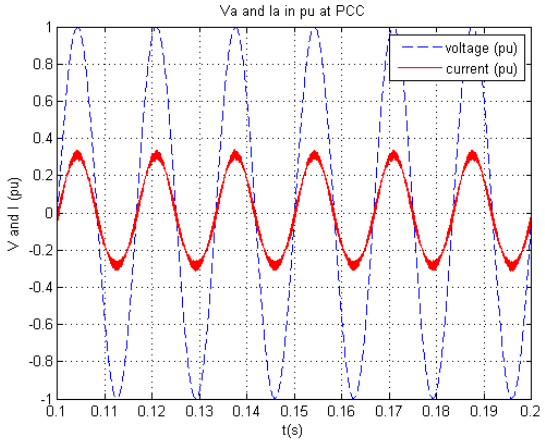

Figure 3.19 Phase voltage and line current measured at PCC.

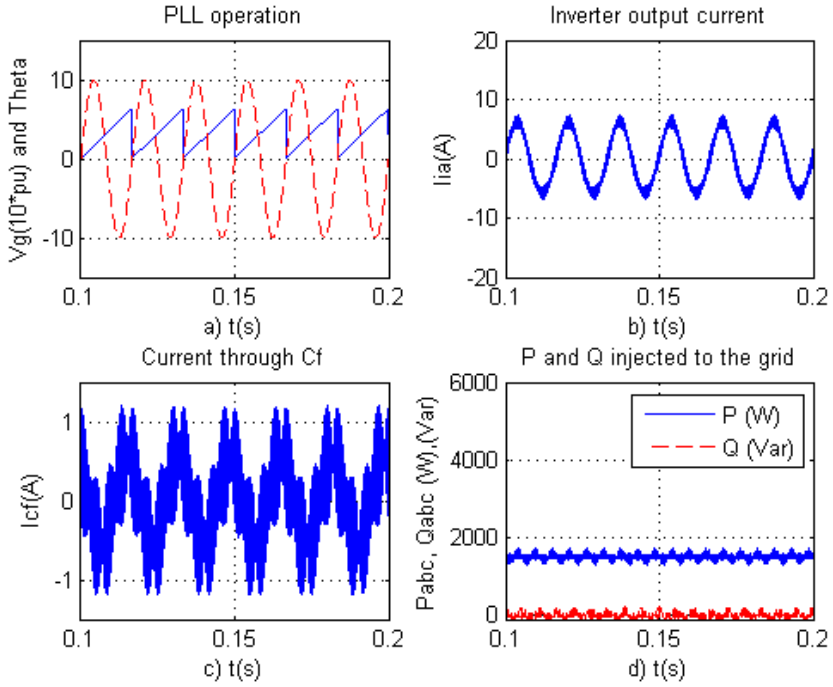

Figure 3.20 a) v_A(10*pu) and phase angle θ from PLL ; b) Inverter output line current; c) Current through filter capacitor C_f; d) Active and reactive power output.

PLL operation, filter capacitor current and active power flow to the grid can be observed on Figure 3.20.

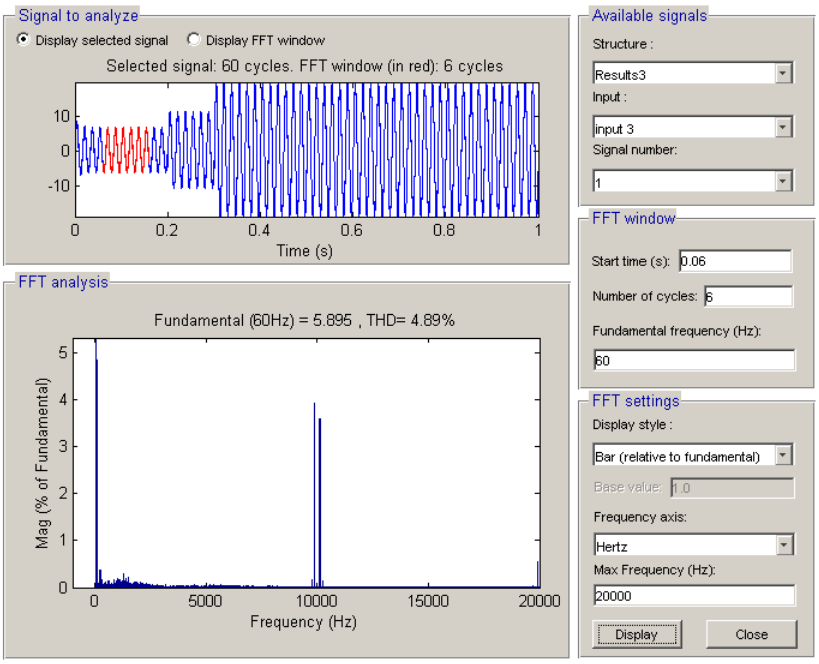

Figure 3.21 THD of line current injected to the grid.

Figure 3.21 shows the THD analysis of line current. THD of the current, when inverter injecting 1500 W to the grid is 4.89%. At 0.2s time step reference command of active power changes from 1500 W to 2500 W and for reactive power becomes 1000 Var.

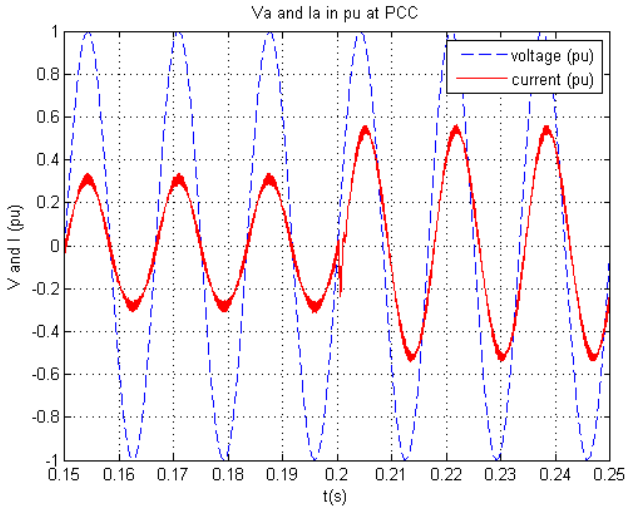

Figure 3.22 Phase voltage and line current measured at PCC.

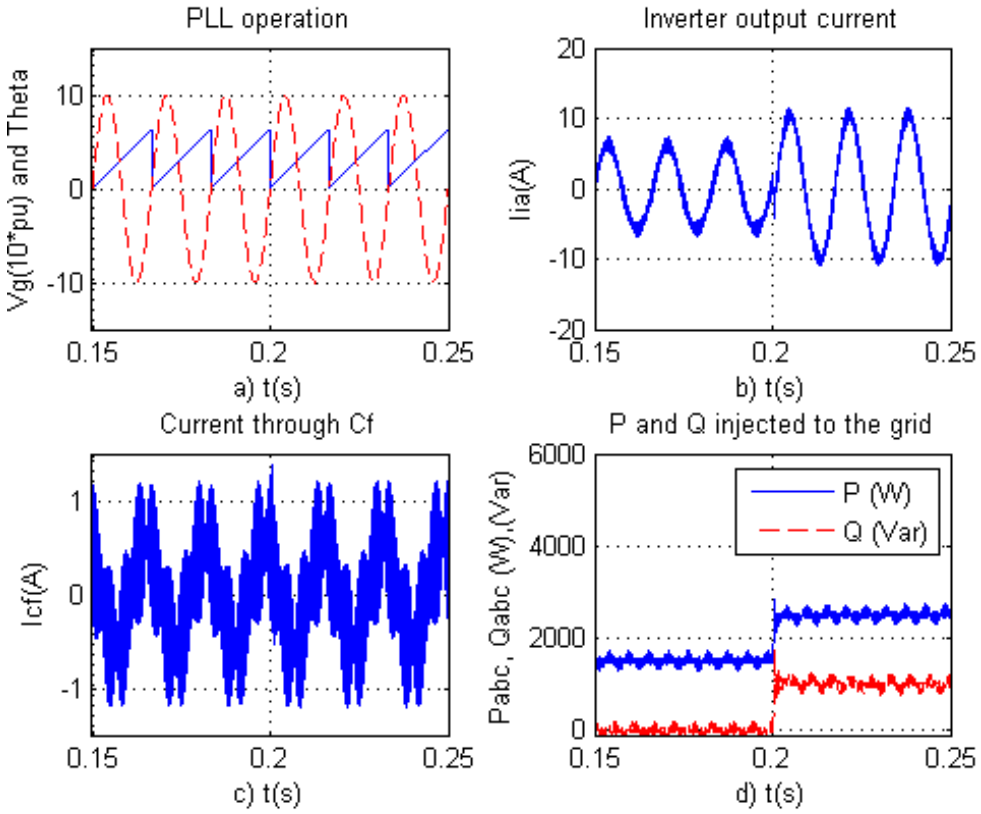

Figure 3.23 (a) v_A(10*pu) and phase angle θ from PLL ; (b) Inverter output line current; (c) Current through filter capacitor C_f; (d) Active and reactive power output.

Figure 3.22 and Figure 3.23 shows the response of line current, active and reactive power during the switch at 0.2 s. It can be noticed that the measured power tracks the reference very well. THD of current injected to the grid is shown on Figure 3.24 and equal to 3.00 %. Also it can be noticed that THD of current is less when the system is operating with higher load.

At time step 0.3s. next command occurs and inverter provides 4500 W and 1500 Var to the grid. Figure 3.25 and Figure 3.26 show the response of line current, active and reactive power during the switch at 0.3s. THD of current injected to the grid is shown on Figure 3.27 and equal to 1.65%. PLL operation, filter capacitor current and active power flow to the grid can be observed on Figure 3.26.

3.3.2 Bidirectional Power Flow from the Grid to the DC-link

This simulation shows the ability of inverter to provide backward power flow from the grid to DC link. Originally inverter provides 2500 W and 1000 Var to the grid, at time 0.3s. there is command for

reference power to consume 1000 W and 3500 Var from the grid. The process of transition can be observed from Figure 3.28. at time 0.3s.

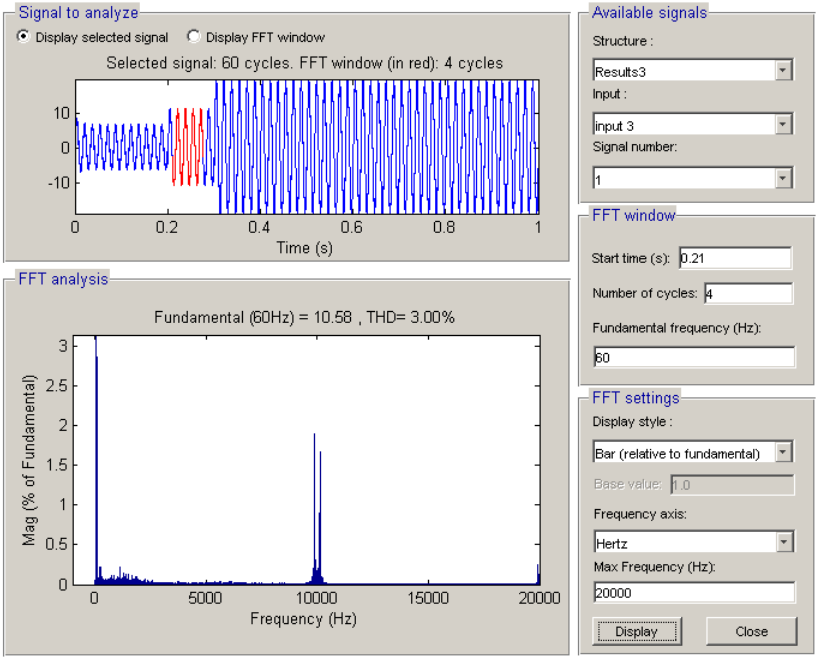

Figure 3.24 THD of line current injected to the grid.

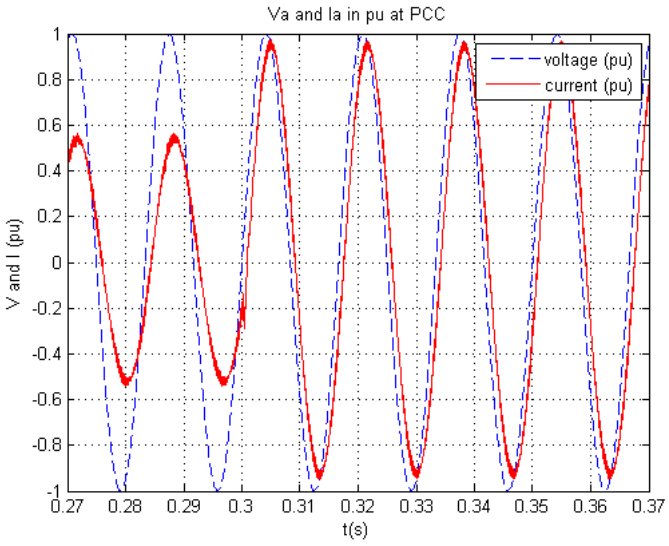

Figure 3.25 Phase voltage and line current measured at PCC

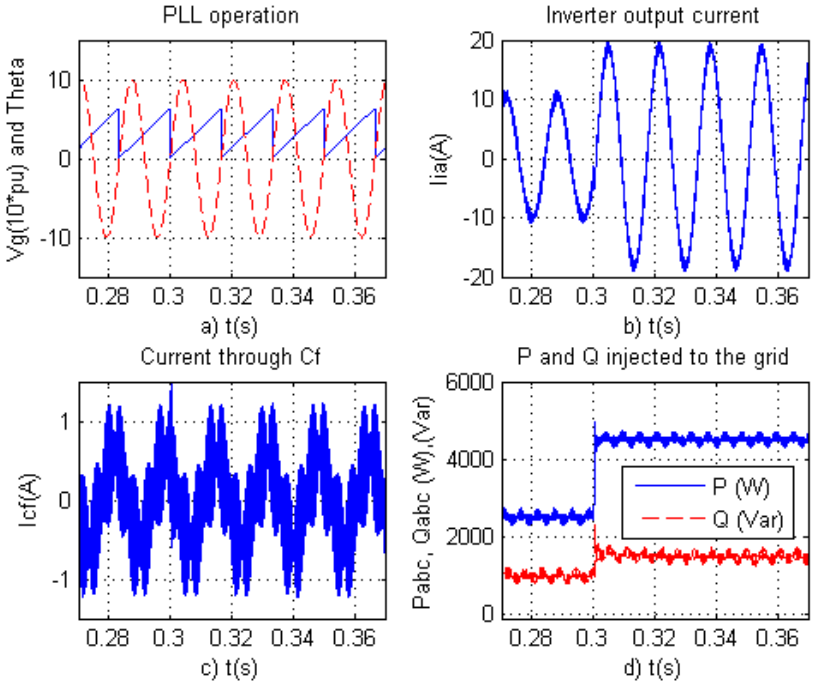

Figure 3.26 (a) v_A(10*pu) and phase angle θ from PLL ; (b) Inverter output line current; (c) Current through filter capacitor C_f; (d) Active and reactive power output.

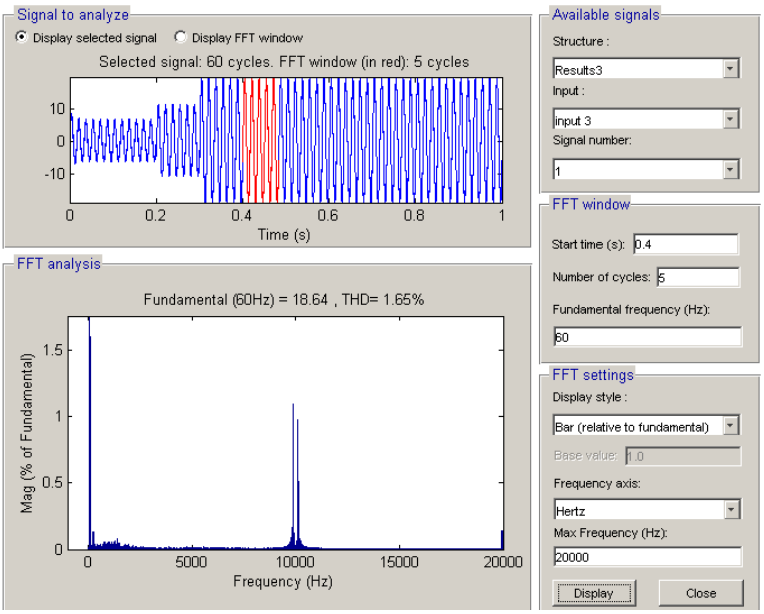

Figure 3.27 THD of line current injected to the grid.

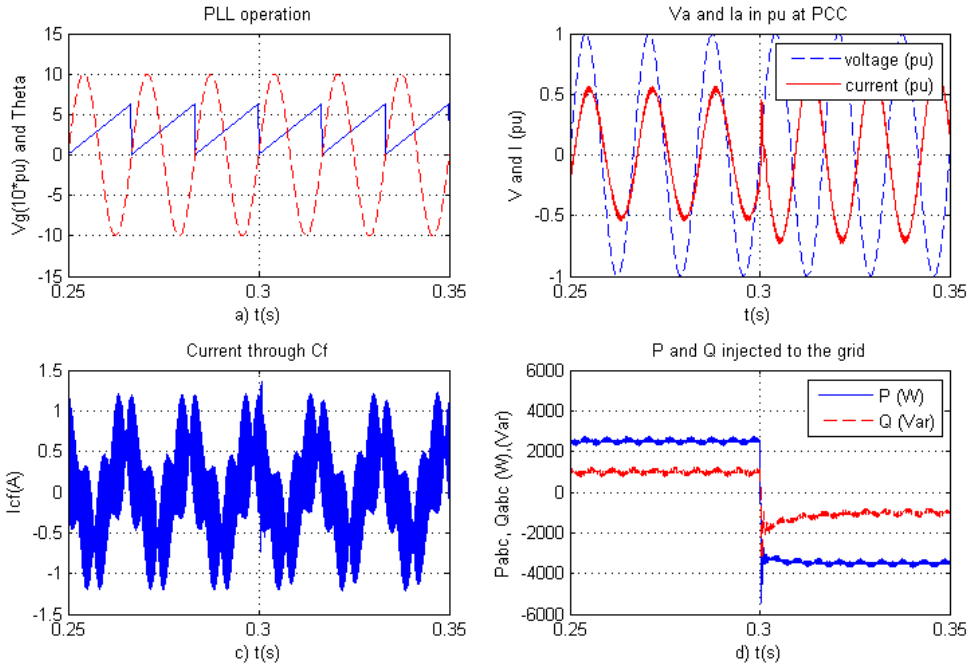

Figure 3.28 a) v_A(10*pu) and phase angle θ from PLL ; b) Inverter output line current; c) Current through filter capacitor C_f; d) Active and reactive power output.

Figure 3.29 shows the performance of PI controllers for d and q components of current in current control system, where I_d is responsible for active power and I_q is responsible for reactive power.

Figure 3.30 shows the average current in dc side of inverter. When the inverter is providing active power to the grid till 0.3s., DC link current is negative. After 0.3s. when inverter starts to provide power to DC side of inverter, current changes to positive value. For better observation DC current measurement was observed through first order low pass filter with time constant 0.01s. That is why it has exponential rise after switch of power flow direction.

3.4 Islanding Detection

In this section three different cases were simulated when the grid has black out. The most important case is when the power exchange between inverter and grid is equal to zero, e.g. local load is equal to the reference power for the inverter, in this case simple passive islanding detection in most of the cases will not work (NDZ). Islanding detection algorithm was described in Chapter 3. Here simulation of proposed algorithm is presented. The block diagrams of simulated system are shown on Figure 3.32 and Figure 3.33.

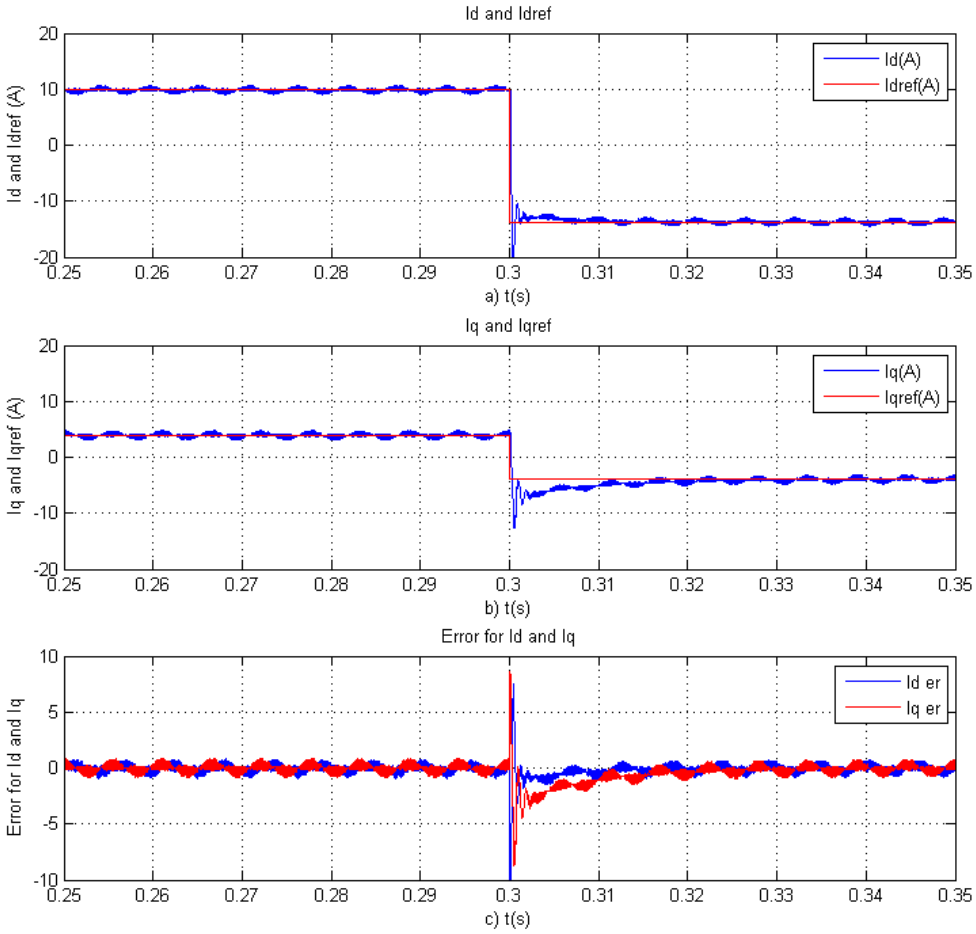

Figure 3.29 (a) I_d and I_{dref}; (b) I_q and I_{qref}; (c) Error for I_d and I_q.

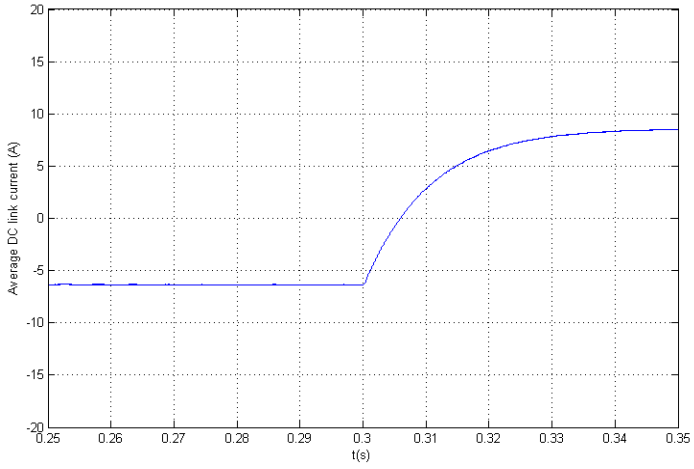

Figure 3.30 Average current in DC link.

All three cases were simulated with assumption that inverter has local load in amount 3000 W, 5000 W and 4000 W. Local load for three simulated cases assumed to be balanced.

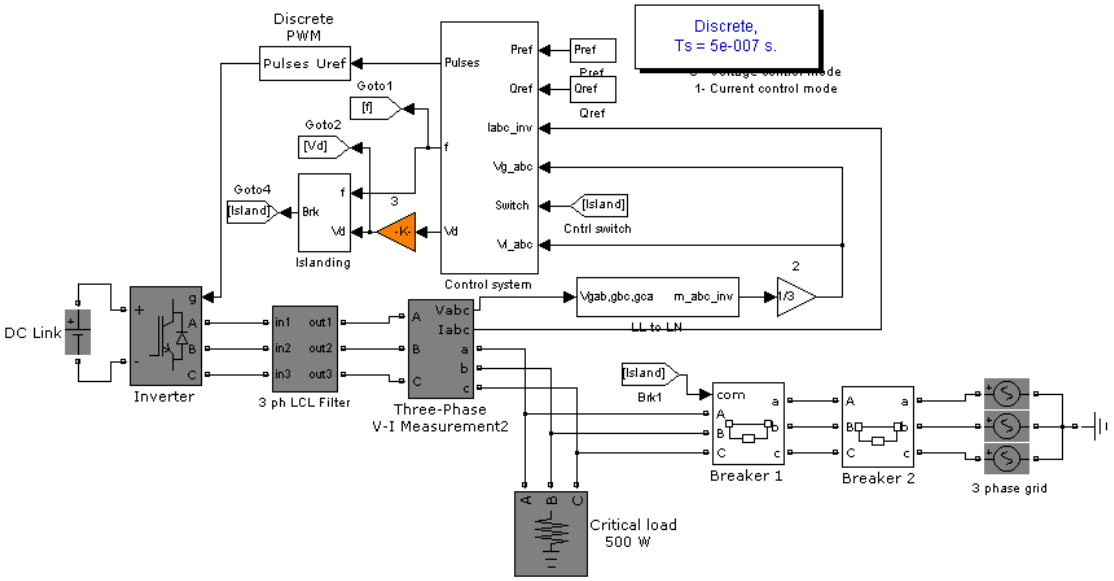

Figure 3.31 Simulink block diagram of the whole system with islanding detection.

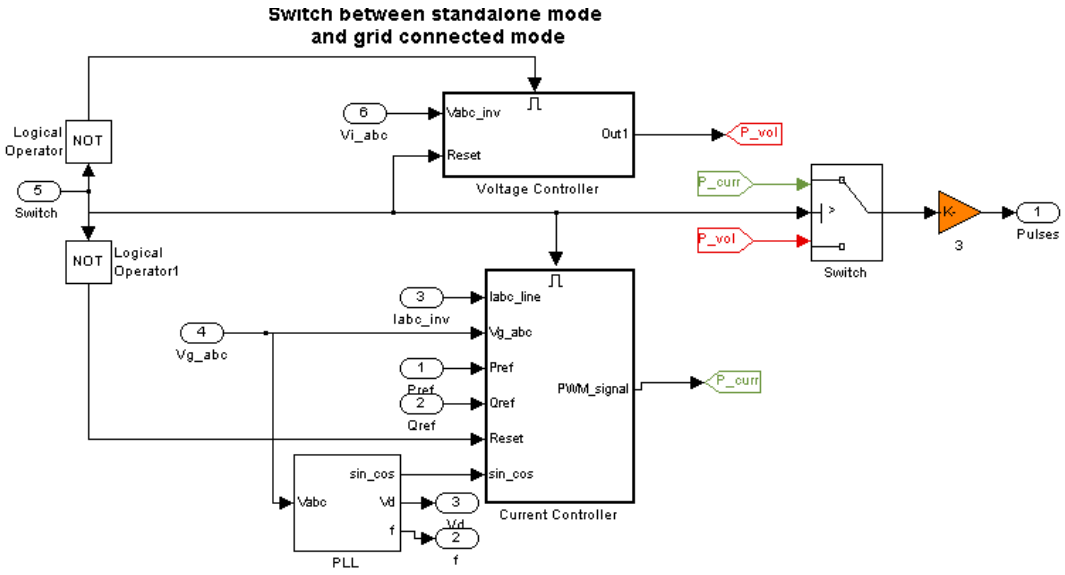

Figure 3.32 Simulink block diagram of islanding detection logic.

Figure 3.33 shows the modified current controller with additional V_d to I_d (in red color) loop for successful islanding detection.

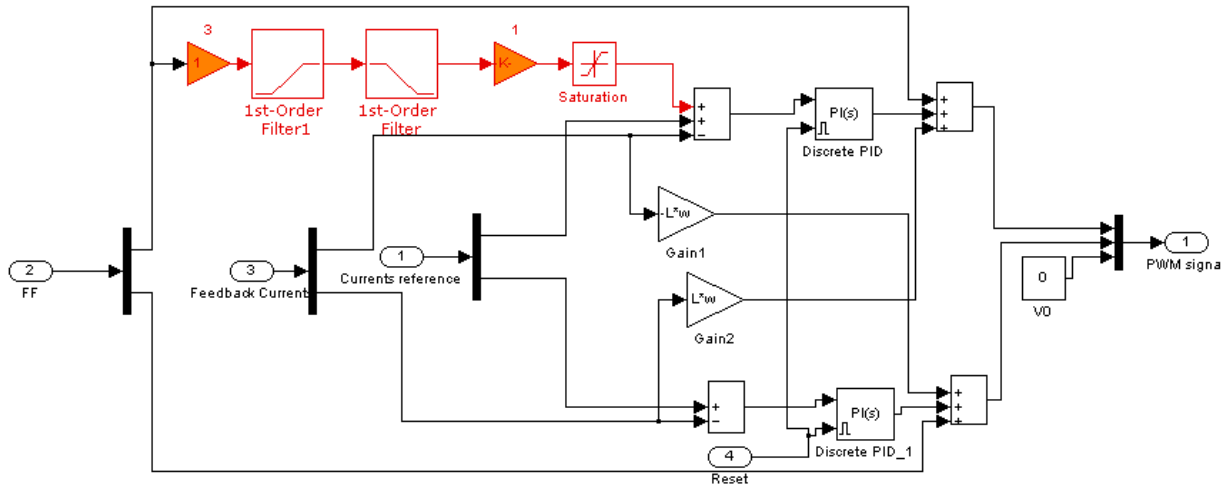

Figure 3.33 Current control system with additional V_d to I_d loop for islanding detection.

Figure 3.34 shows the pattern of phase voltages and line current when the inverter providing to the grid 5000 W, at 0.1s. grid goes away and inverter after small amount of time switches from current control mode, which was active in grid connected mode to voltage control mode, see the Figure 3.35.

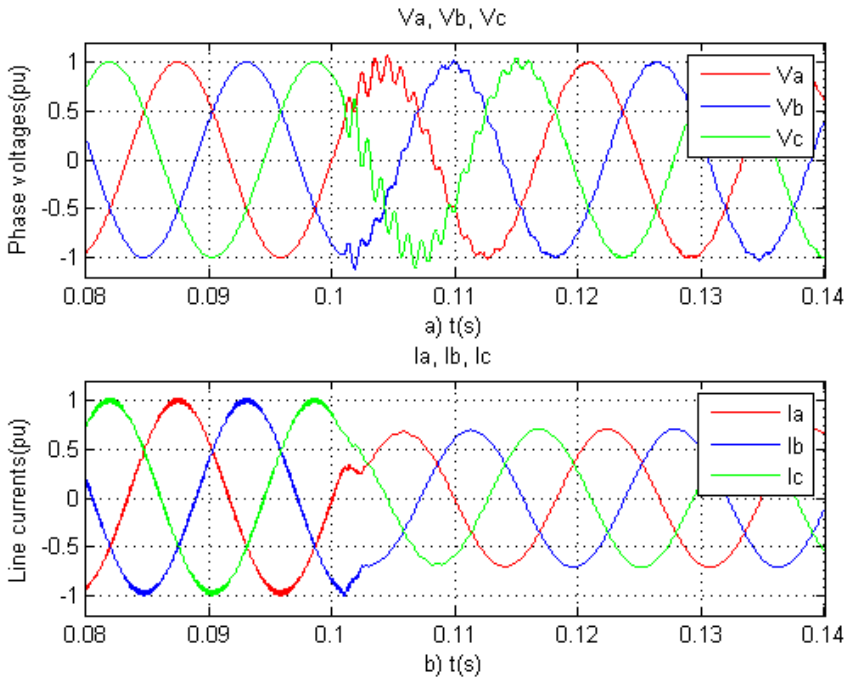

Figure 3.34 Phase voltages and line currents during the switch from current control to voltage control mode.

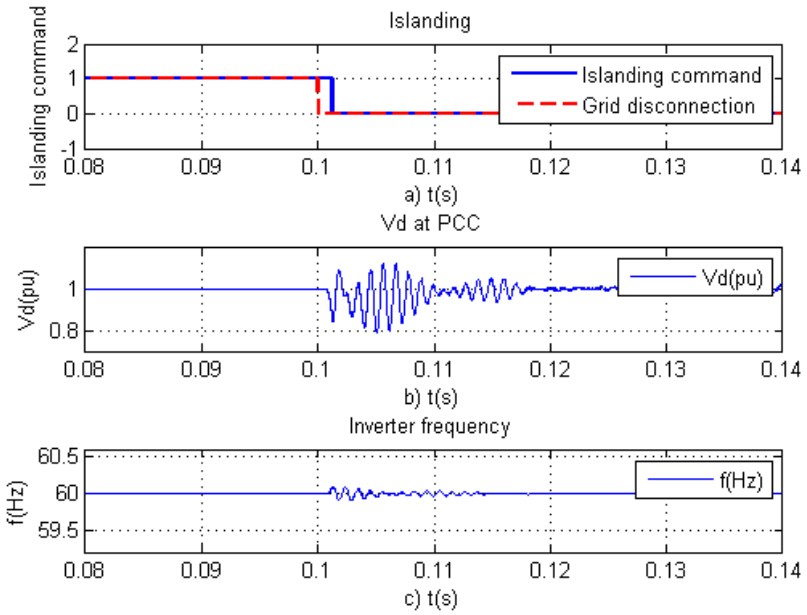

Figure 3.35 (a) Islanding detection; (b) V_d at PCC; (c) f of the inverter.

Figure 3.35 and Figure 3.36 and show the successful islanding detection and switch between control system, when the power exchange between grid and inverter is equal to zero.

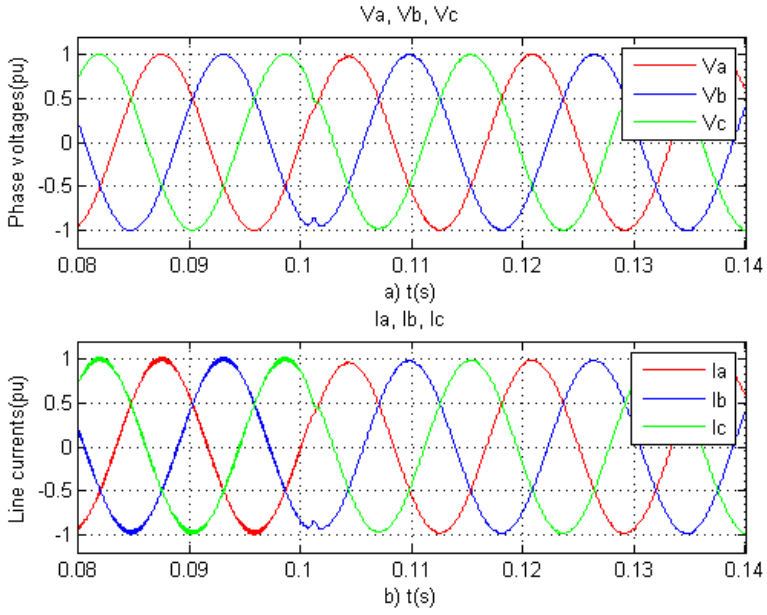

Figure 3.36 (a) Phase voltages and (b) line currents during the switch from current control to voltage control mode.

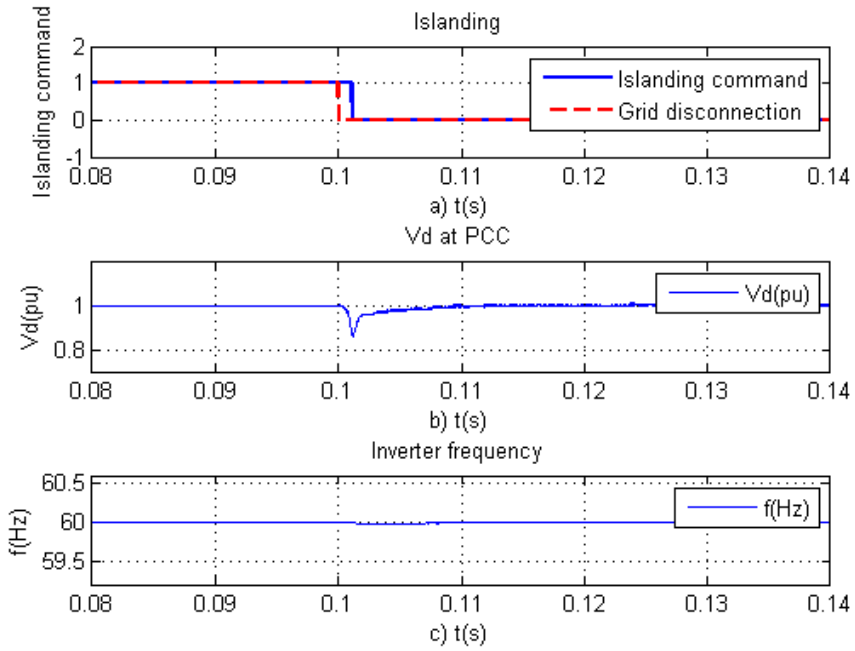

Figure 3.37 (a) Islanding detection; (b) V_d at PCC; (c) f of the inverter.

Figure 3.38 and Figure 3.39 show the successful islanding detection and switch between control system, when the inverter is set up for providing 1500 W and local load is 4000 W.

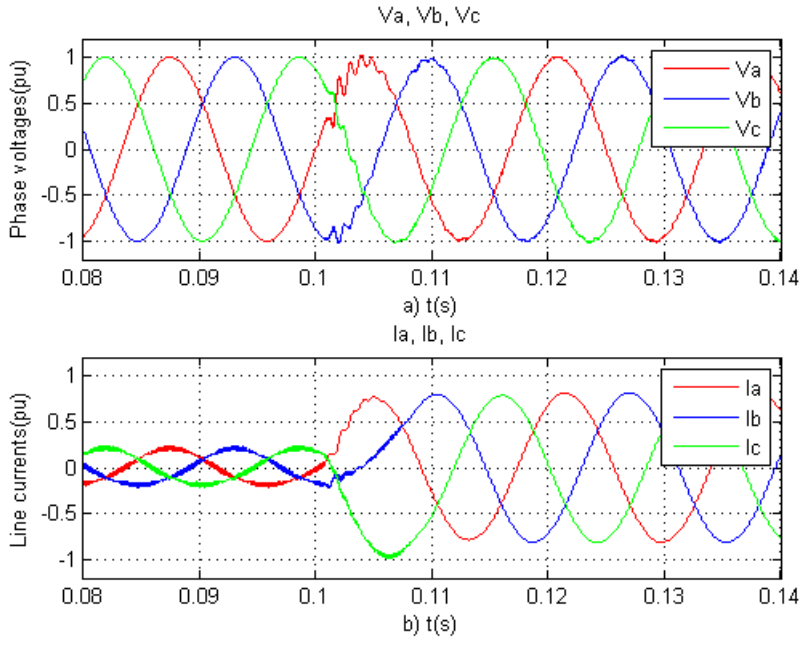

Figure 3.38 (a) Phase voltages and (b) line currents during the switch from current control to voltage control mode.

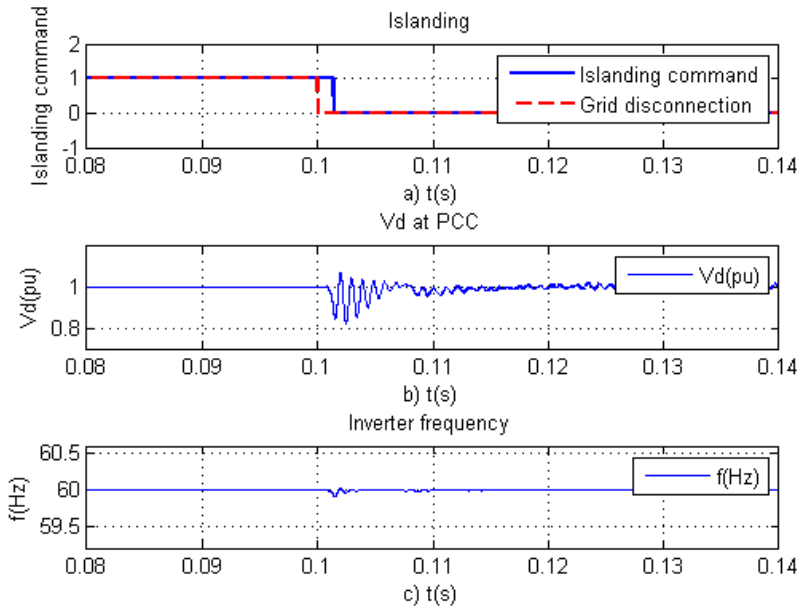

Figure 3.39 a) Islanding detection; b) V_d at PCC; c) f of the inverter.

It can be seen from three simulated cases that implemented islanding detection scheme successfully detects black out and quickly switch from one control system to another. As it was expected islanding detection algorithm in all cases was working because of V_d disturbance and fluctuations outside the limits presented in Chapter 3.

3.5 Conclusion

In this chapter the simulations of the three phase inverter system obtained using Matlab/Simulink platform are presented. First the voltage controller for standalone mode was tested by implementing step change in load. Second the current controller for grid connected mode was tested using different reference active power in both directions. The tests proved that both controllers are working in assumed conditions and have good performance.

It should be mentioned that LCL filter originally was designed for 15 kHz PWM switching frequency, as it mentioned in previous chapter, however during the experimental work was discovered that dSPACE hardware requires sampling time multiple of switching frequency. Because of that switching frequency for PWM was accepted 10 kHz and sampling time 100μs both for hardware and simulations.

Next two chapters will give detailed description of hardware setup and experimental data analysis.

CHAPTER 4
EXPERIMENTAL SETUP

4.1 Objective

This chapter describes the electronic circuits and computational hardware used for the experimental evaluation of the inverter system. The system setup comprised of a hardware-in-the-loop (HIL) based on a dSPACE rapid prototyping solution that allowed all the Simulink based solution that allowed a fair comparison of simulation and experimental results. Figure 4.1 shows the schematic of the complete experimental setup. The components include a Semikron inverter, a programmable DC power supply capable to emulate a photovoltaic array, a dSPACE 1104 real-time hardware, a LCL filter, relay circuits, current and voltage sensors to providing voltage and current feedback, one computer (PC) with the Control Desk software and the program Matlab running the real-time Simulink model developed in Chapter 3.

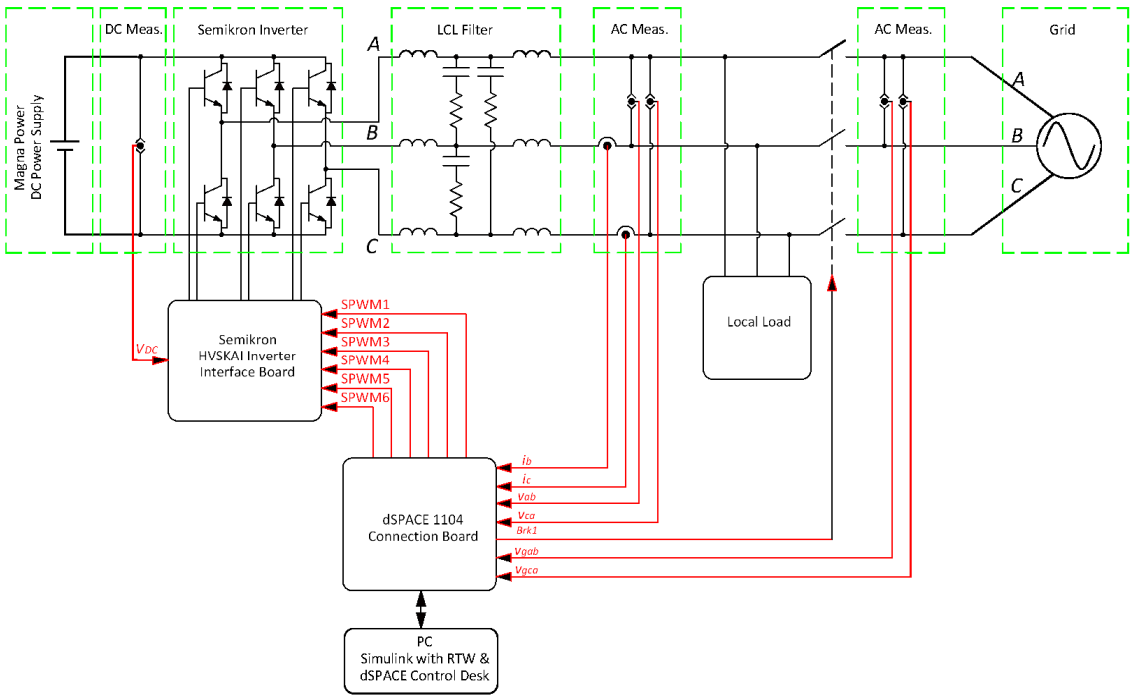

Figure 4.1 Complete experimental setup.

Figure 4.2 shows a picture of the experimental setup which has been assembled in a 19 inches rack with stacked shelves that permit future expansion of this system. A brief description of all the components in this setup is explained in the following sections.

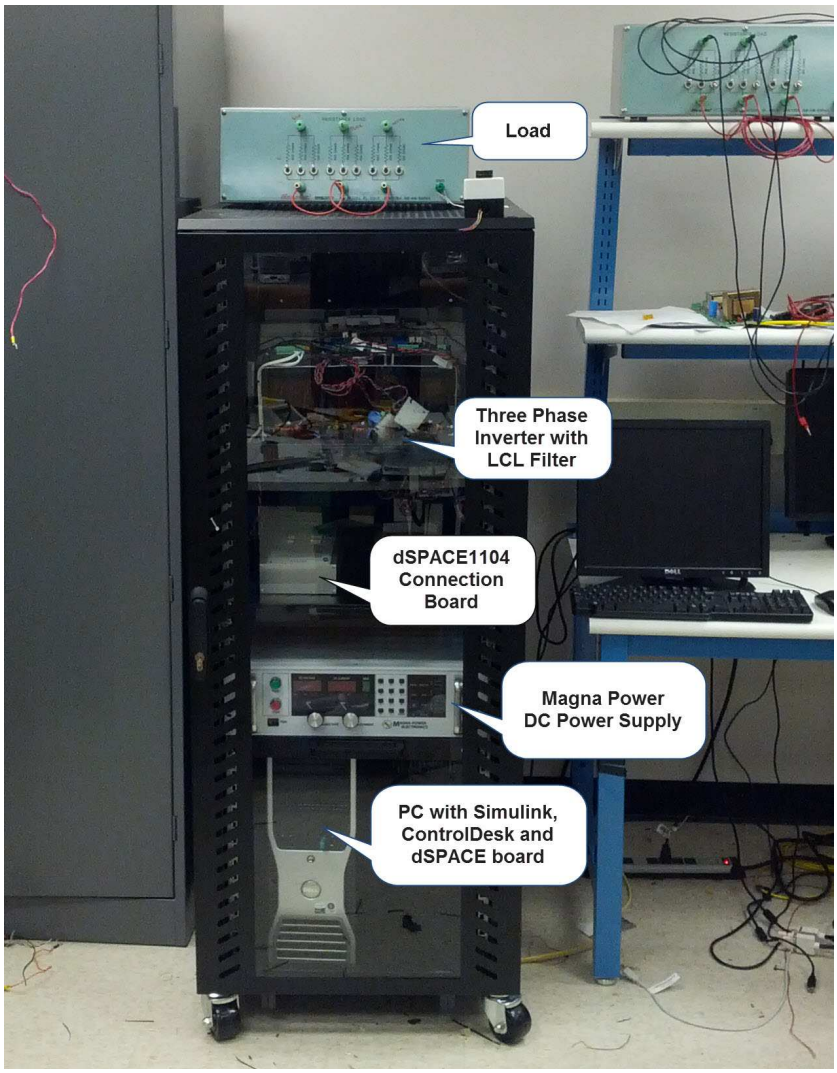

Figure 4.2 Picture of experimental setup.

4.2 Circuits

This section describes the various circuits designed to control the voltage source inverter (VSI) in stand-alone and grid-connected modes. All the circuits have their signals traced from their origin to either the inverter or the dSPACE input/output ports. Several current and voltage sensors were necessary to gather feedback signals for implementing the schemes presented in Chapter 3where a Simulink simulation study has been designed. Data from these sensors is collected by the DS1104 Connectors board, shown in Figure 4.3.

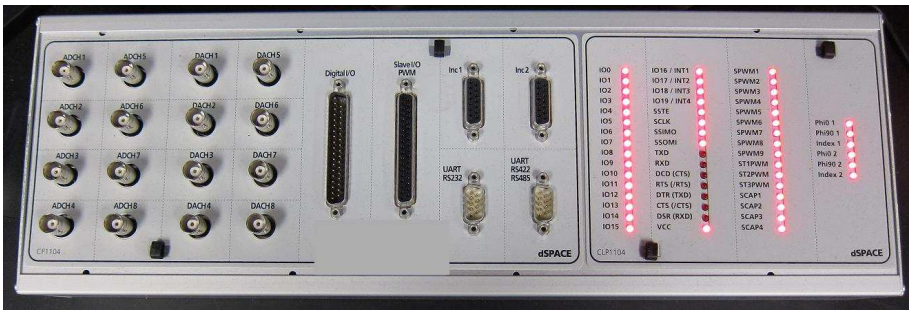

Figure 4.3 DS1104 Connectors board.

4.2.1 Current and Voltage Sensors

Two current sensors and four voltage sensors are used in this project. The quantities that are required for implementing the grid-connected and stand-alone modes of operation are: v_{gAB}, v_{gCA}, v_{iAB}, v_{iCA}, i_{iAi}, i_{iB}. Assuming a balanced load with floating neutral, only two current measurements are required ($i_{iA} + i_{iB} + i_{iC} = 0$). Also, only two line voltages are required at the point of common coupling (PCC), because the instantaneous sum of balanced line voltages is zero (v_{gAB} and v_{gCA}). The voltage at load terminals (v_{iAB} and v_{iCA}) is measured for the purpose of voltage control during stand-alone mode operation. Hall-effect LEM sensors are used to measure these variables. The transducers provide an output voltage proportional to variable that is being measured. LV-20P type sensors are used for voltage measurements and LA-55P type sensors are used for current measurements [54]. The sensors are placed at various points in the power circuit as shown in Figure 4.1.

Figure 4.4 shows the circuit of one of these two current sensors, where power supplies are applied and the signal M is the feedback, the left side shows a connector in the board, see Figure 4.6. Figure 4.5 shows the filtering circuit used for two current sensors.

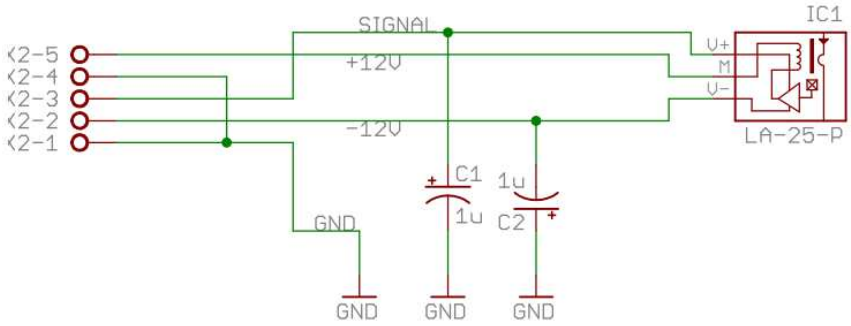

Figure 4.4 LA-55P current sensor circuit.

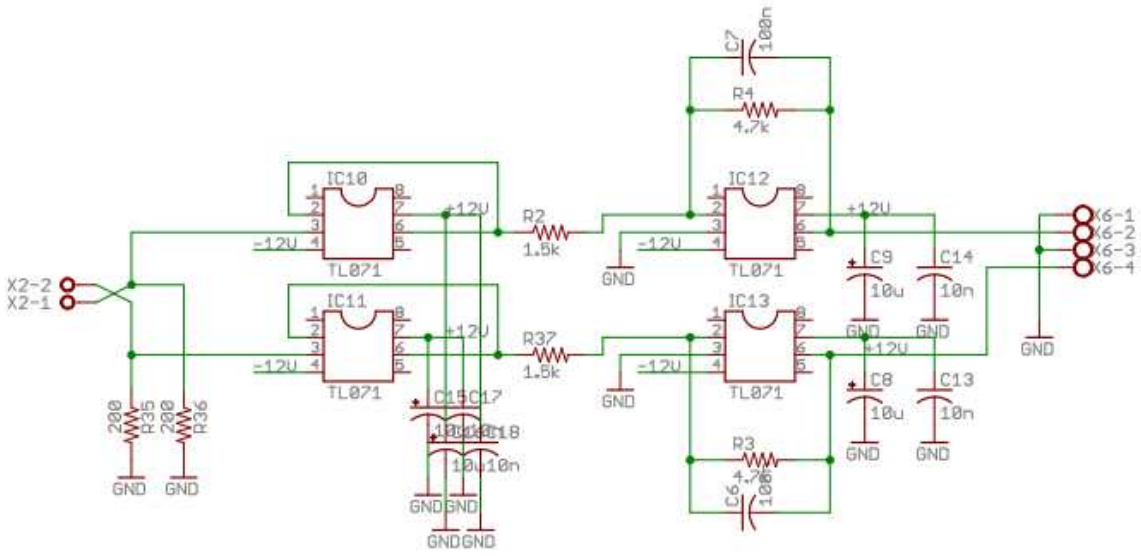

Figure 4.5 Full circuit for LA-55P current sensors with filter.

Both current and voltage signals are filtered using such first-order op-amp low-pass filters, and a gain are tuned to have a range of approximately $\pm 10V$.

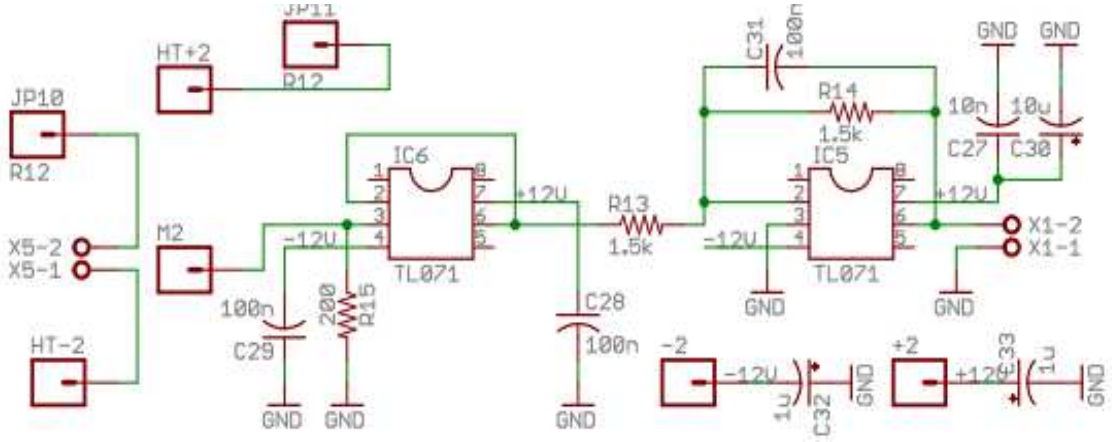

Figure 4.6 Full circuit for LV-20P voltage sensor with filter.

These measurements are then sent through the DS1104 Connectors Board and are available for the running control software in the computer. The sensors circuits have been assembled in printed-circuit-boards (PCBs) shown in Figure 4.6.

Figure 4.8 shows the relay circuit which is used to control the three 120VAC three-phase contactors used for command the inverter to operate in stand-alone or grid-interconnected modes and the critical load. This circuit comprises of integrated circuits (ULN2803AG) that interface the output TTL

signals of the Connectors Board to the voltage levels required to command the 5VDC relays (DS2E-SL2-DC5V).

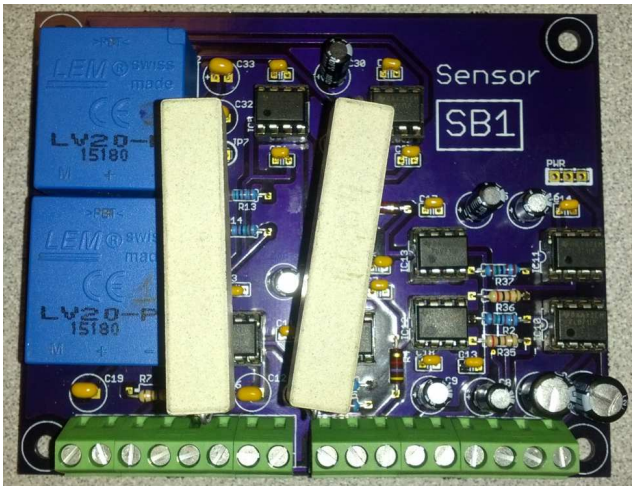

Figure 4.7 Sensors board.

The commands for closing or opening the contactor are sent from the computer using the Control Desk Interface and can also be manually imposed using push-buttons in the rack.

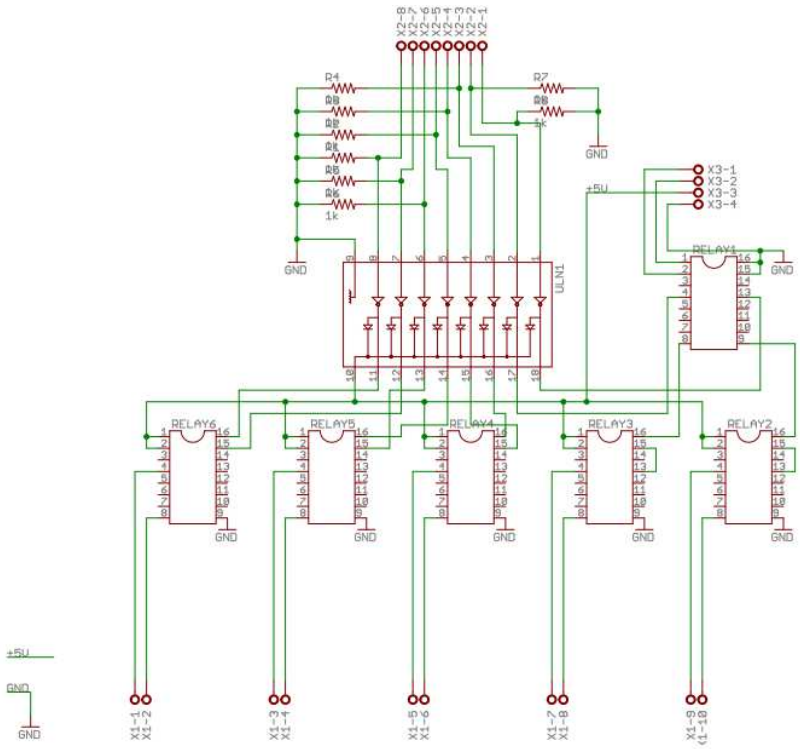

Figure 4.8 Relay circuit.

The relay circuit is assembled in the circuit board portrayed in Figure 4.9.

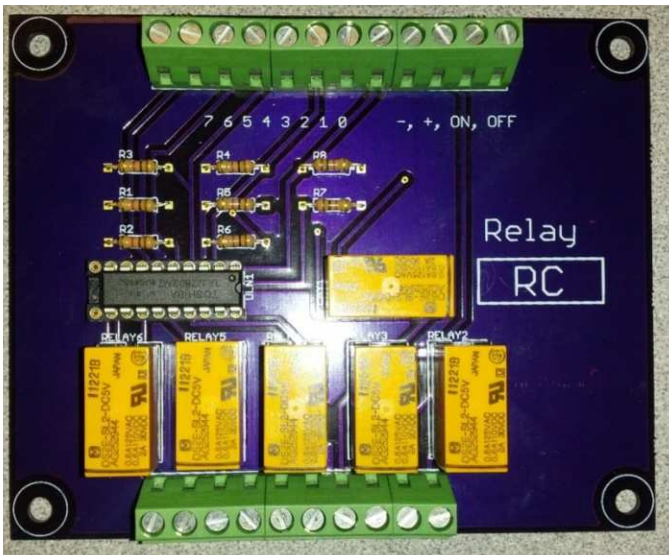

Figure 4.9 Relay circuit board.

4.3 dSPACE 1104 [55]

The DS1104 R&D Controller Board, shown in Figure 4.10, is a DSP based hardware that upgrades the PC into a powerful development system for rapid control prototyping with real-time capabilities made of a PowerPC technology with a set of I/O interfaces. The dSPACE Prototyper system provides full graphical configuration, with programming developed in Matlab Simulink and experimental control tools with state-of-the-art real-time software. The board can be installed in any PCI slot of a PC. Analog signals inputs are shown in Table 4.1.

Table 4.2 represents the output of digital signals used for PWM and relays control.

Table 4.1 Analog signal input.

Channel	Signal
1	DC Link measurement
2	v_{iAB} measurement
3	v_{iCA} measurement
4	i_{iB} measurement
5	i_{iC} measurement
6	v_{gAB} measurement
7	v_{gCA} measurement

Figure 4.10 DS1104 R&D Controller Board.

Table 4.2 Slave I/O PWM Connector (CP18).

Pin	Signal
7	SPWM1
8	SPWM3
9	SPWM5
26	SPWM2
27	SPWM4
28	SPWM6
34	Relay #1
34	Relay#2

4.3.1 Technical Details

Figure 4.11 shows the structure of the dSPACE 1104 with the bus and peripherals of this system:

- Main processor: MPC8240, PowerPC 603e core, 250 MHz, 32 kByte internal cache
- Timers: 1 sample rate timer, 32-bit downcounter, 4x32-bit general purpose timers, 64-bit time base for time measurement.
- Memory: 32 Mbyte synchronous DRAM (SDRAM), 8 MByte boot flash for applications.
- Interrupt control unit: Interrupts by timers, serial interface, slave DSP, incremental encoders, ADC, host PC and 4 external inputs, PWM synchronous interrupts.

- Analog input: 4x16-bit multiplexed, ADC inputs with 2μs sampling time, 4x12-bit ADC channels with 800ns sampling time, $\pm$10V input voltage range.
- Analog output: 8x16-bit channels, 10 μs maximum settling time, $\pm$10V output voltage range.
- Digital I/O: 20-bit digital I/O (bit-selectable direction), $\pm 5mA$ output current.
- Slave DSP subsystem: Texas Instruments DSP TMS320F240, 4 kWord of dual-port RAM, three-phase PWM output plus 4 single PWM outputs, 14 bits of digital I/O(TTL)
- Physical characteristics: Power supply 5V, 2.5A/ -12V, 0.2A/12 V, 0.3 A, requires one 32-bit PCI slot.

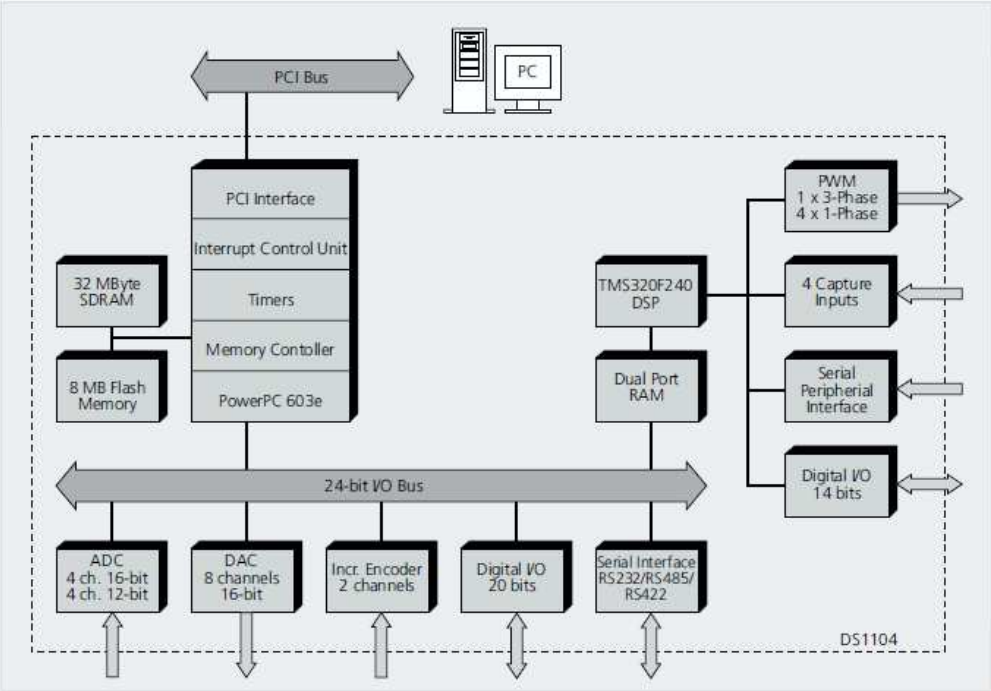

Figure 4.11 dSPACE system structure diagram.

4.4 Semikron Inverter HV SKAI Module Family [56]

The SKAI module belongs to a family of products primarily designed for driving three-phase loads from a DC source, and it is typically used for implementing motor drives, but in this project it has been adapted to operate as an inverter that can be fed by a renewable energy source such as a PV or a fuel-cell. The user manual describes the HV SKAI module explaining the available configurations and how to incorporate the module in a system. Figure 4.12 shows the block diagram of the HV SKAI with a 6 pack module with a built-in DC-link capacitor, integrated current sensors, temperature sensors,

protection logic, gate drivers and an optional DSP controller all mounted on a pre-molded heat sink. The SKAI uses Semikron latest pressure contact technology for compact design, improved thermal performance and high reliability.

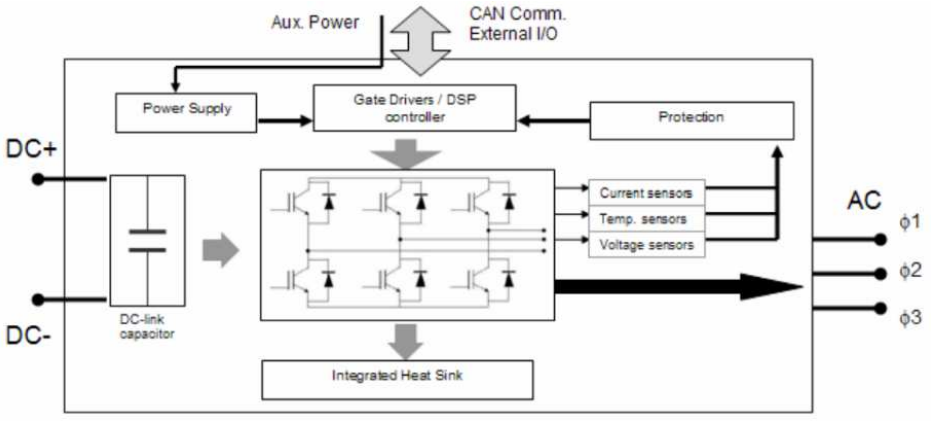

Figure 4.12 HV SKAI block diagram.

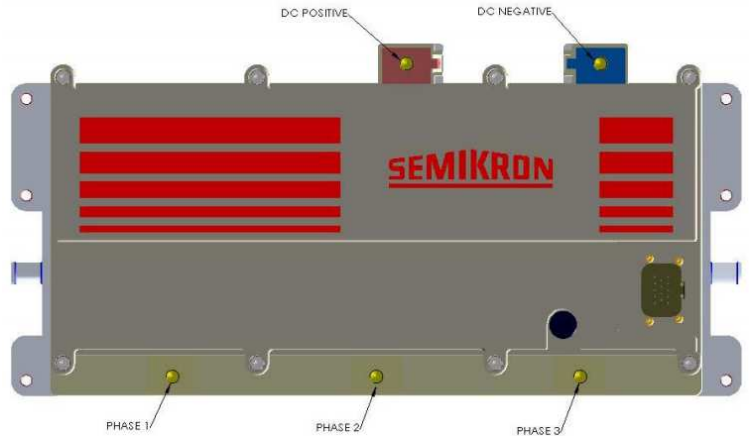

Figure 4.13 External Power Terminals.

Semikron integrated the DC-link capacitors in order to reduce stray-inductance allowing higher bus voltages and better EMC and EMI characteristics. Integrated the DC-link capacitor makes the inverter smaller, more reliable and robust. This compact construction technique is extremely rugged making it a versatile design for applications in mobile platforms. It can be configured with the newest generation of 600 volts, or 1200 volts IGBTs. The heat sink can be liquid cooled for high power applications, but in our system forced air by fans in the rack is sufficient. The SKAI incorporates the IGBT gate drivers with built-in current protection and the internal circuitry allows several outputs for interfacing with the

computer control (APPENDIX C contains information of inverter module pin out). Figure 4.13 shows the external power terminals for connections.

4.4.1 Module Components

This section describes module components such as the IGBTs, heatsink, the driver board, interlocking time specifications and the driver signals control logic.

4.4.1.1 IGBTs

The IGBTs are mounted on 3 DBCs (Deadbeat controller) each in a half bridge configuration. The DBCs are populated in this module with 600 volt IGBTs. The DBC material is ALN (Aluminum Nitride) which provides better thermal conduction for a higher current capability. The DC Link bus bars have a film capacitor incorporated in the module, which eliminates the need for high frequency device snubber capacitors.

Table 4.3 Module parameters.

Module Ratings	600	Units
Silicon Voltage	600	V
IGBT Breakdown Voltage	600	V
Maximum DC Link Voltage	450	V
Maximum Continues AC Output Current	400	$Arms$
Peak Current Limit	1000	$Apeak$
DC-Link Trip Voltage	458	V
DC-Link Capacitance	1	mF

4.4.1.2 Heatsink

Standard air-cooled HV SKAI modules use an Alcan HKH R400 heatsink. When used with three (3x) 4“ muffin fans (NMB 4715FS-12T-B50/ 115 VAC) and the appropriate plenum for a total airflow of 110 CFM, the heatsink performance was measured to be 0.032 K/W. Note the direction of the air flow for this type of a heat sink.

The default dead-time between TOP and BOT turn on is set for 2 μs. The driver board can be configured (at the factory), for 1, 2, 3, or 4 us interlock time or zero cross conduction protection.

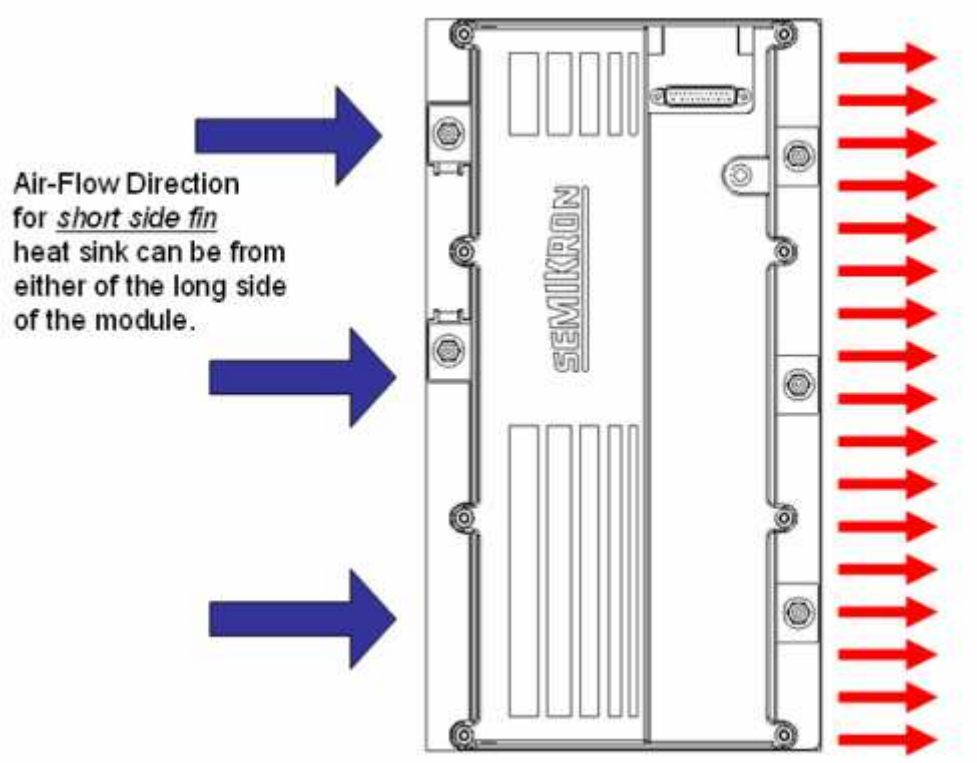

Figure 4.14 Short side fin air-flow direction.

The interlock time is not simply added to the TOP and BOT signals. If the TOP and BOT signals have greater than the set minimum interlock time then the TOP and BOT signal propagate through with no timing change. The interlock protection only guarantees a minimum interlock time.

4.4.1.3 Drive Signals

BOT HB 1, TOP HB 1, BOT HB 2, TOP HB 2, BOT HB 3, and TOP HB 3 are input signals that generate the switch commands for the 6 switches, and are provided by the dSPACE, see the Table 4.2. These are positive 5 or 15 V CMOS logic, and in this system it is set to 5 V. When the binary output is "High" the correspondent switch is on and when it is "Low" the correspondent switch is off. When driven from 5 volt logic the input impedance is 60k. When driven from 15 volt logic the input impedance when driven to logic high is 7k, when driven to a logic low the input impedance is 60k.

4.4.2 DC link Analog Output

The terminal # 19 of the interface connector provides the DC link OUT measurement, i.e. an analog signal proportional to the DC link voltage. The maximum voltage(9 V) indicates full scale and the scaling factor can be computed based on Table 4.4.

Table 4.4 DC link out parameters.

Silicon Voltage	600
Scale V_{link}/V_{out}	50
DC Link Max Voltage(@9V)	450
DC Link fault Voltage (@9.18V)	459

4.4.3 Error Signals

Terminals #3, #14, and #17 of the interface connector are the ERROR OUT pins. All those 3 pins are open-collector and tied together so there is only 1 signal pulled "High" by an external pull-up resistor. When the signal is "Low" there is no error. This signal reports an error for a V_{fault} on any switch, over-current on any phase, over-voltage of the DC link, under-voltage of the +15 V supply, and over-temperature of the heat sink. When an error is detected the switching must be inhibited i.e. all switches are turned off. In order to reset the control board and restart, all fault conditions must be removed and all upper and lower IGBT input signals must be low for at least 9 s.

4.4.4 Driver Board Power Supply

The SKAI driver board requires a supply of DC input voltage from 8 to 30VDC and 16W. This is supplied to the PWR and GND pins. The integrated DC/DC converter supplies all necessary voltages for the driver and controller, in this project the supply voltage is 12 VDC volts, fed by a power supply, indicated in Figure 4.15. The module has a high voltage insulation (3,000 VAC) between the interface connector pins and the DC-Link terminals.

Figure 4.15 DC power supply.

4.5 LCL filter Inductors Software and Magnetic Design

This section describes how the LCL filter was magnetically designed and constructed using a software called Inductor Design [57].

4.5.1 LCL filter Inductors Software Design

The Inductor Design software assists practicing engineers in selecting the optimum core for inductor applications. Such software has been specifically made for switch-mode power supply (SMPS) output filters (DC Inductors), but the procedure has been adapted for designing the AC inductors for this inverter. This software uses a design algorithm intended to specify the smallest design package size for the given input parameters: (such as current, inductance value, frequency and so on)

- Online Help to educate users with respect to important core material characteristics, as well as a comparison of powder core materials, including; MPP, High Flux, Kool Mμ®, and XFLUX®;
- A comprehensive reference list of further information to help designers find answers to even more involved design issues;
- A complete overview and definitions of input and output parameters;
- The software has a database for several magnetic geometries such as E cores, U cores and toroidal cores with the consideration of stacking of cores for increased magnetic volume;
- Hardware recommendations for core selections are also included;
- And an option to save the inductor design for reference and comparative analysis.

  The software user interface is depicted in the next two pictures: Figure 4.16 and Figure 4.17.

Two types of cores (Table 4.5) from Magnetics (www.mag-inc.com) were used for the inductors. The design software is available online (http://www2.mag-inc.com/calculators/inductor-design-calculator-test). It has been used to define the core types, calculate the required number of stacked cores for each inductor, to specify the wire gauge. The inductors were constructed by hand.

Table 4.5 Inductor parameters.

Parameter	L_1	L_2
Inductance(mH)	2.33mH	0.045mH
Core Type	77102-A7	77258-A7
Number in Stack	5	1
Wire	AWG # 12	AWG # 12
Number of Turns	116	43

Table 4.5 sums up all calculated parameters required for wire length calculation, which can be found in Appendix B.

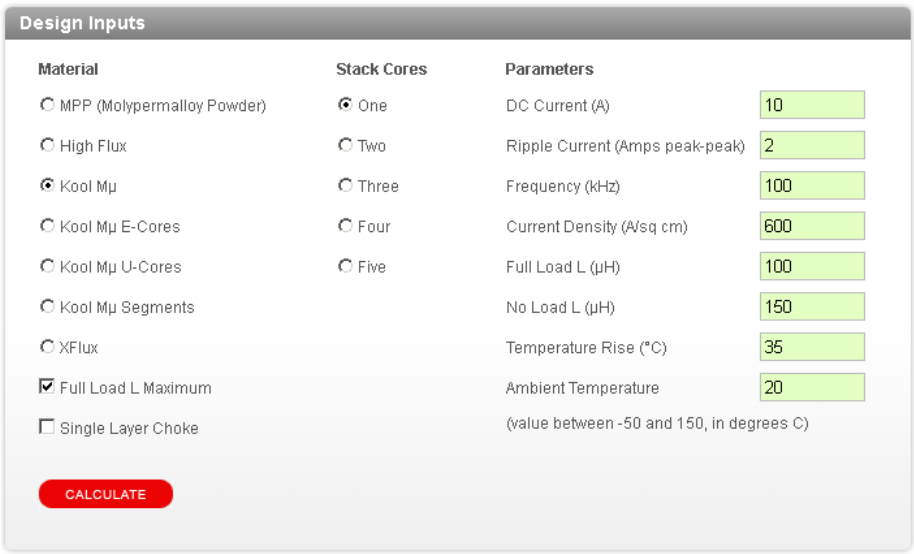

Figure 4.16 Screen showing the design of the inductors.

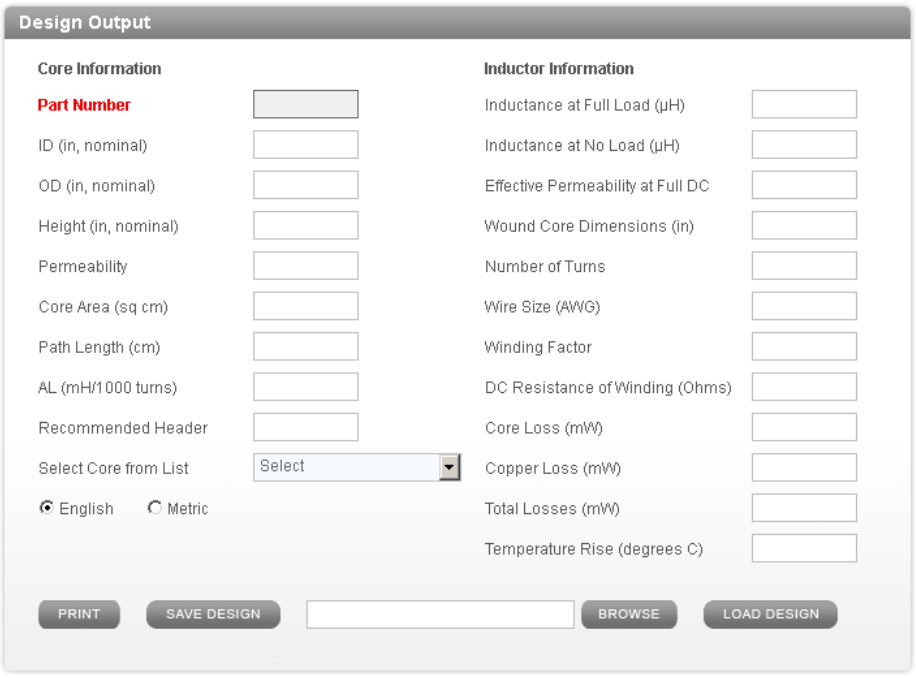

Figure 4.17 Design outputs for inductor.

Figure 4.18 shows the delta circuit of filter capacitors with sandstone damping resistors in series. Implemented LCL filter is presented on Figure 4.19.

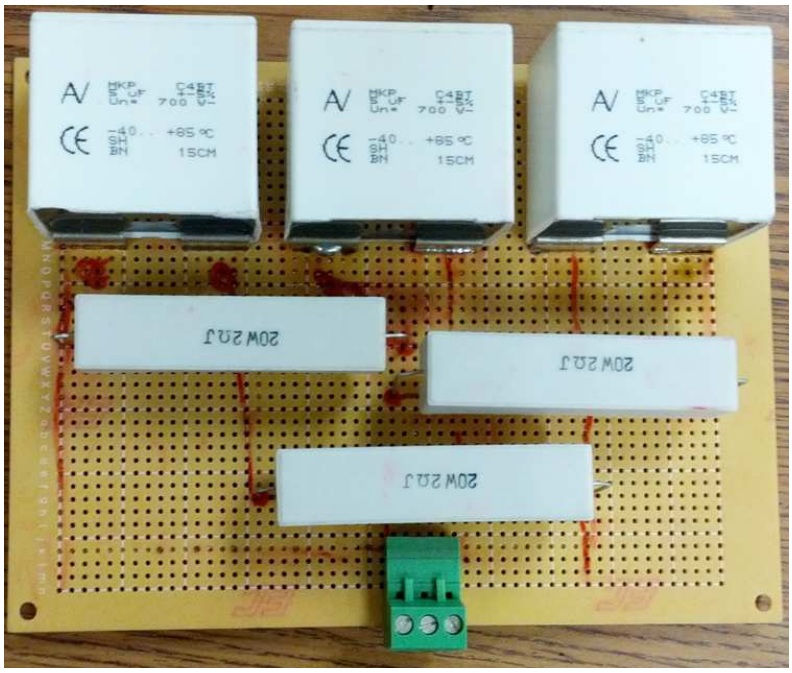

Figure 4.18 C_f, R_f delta circuit.

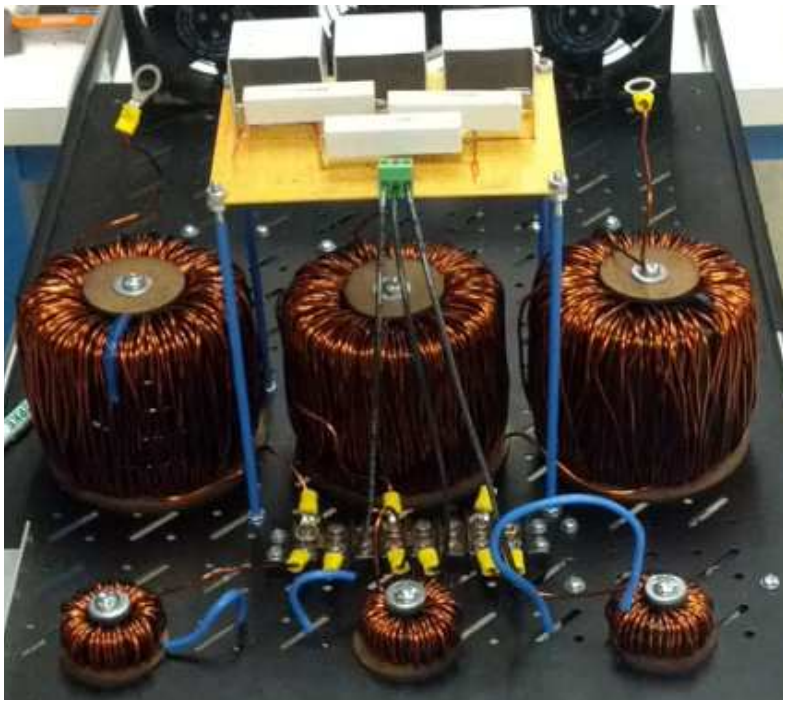

Figure 4.19 Implemented LCL filter.

4.6 Control Desk User Interface

A simple graphical user interface can be implemented in Control Desk for this inverter control, as shown in Figure 4.20. It displays relevant data and various options to control the inverter. The displayed values on the screen are either three-phase quantities in reference-frame or dc quantities. Data such as the reference voltage, active and reactive power for the inverter can be observed and the controller can be stopped for debugging if the values seem to be out of range. The values are refreshed every $10ms$ when running without storing data and are refreshed every 1 sec when storing data. Reference values and PI gains can be changed on the fly and it is possible to observe the response of the inverter to new input values.

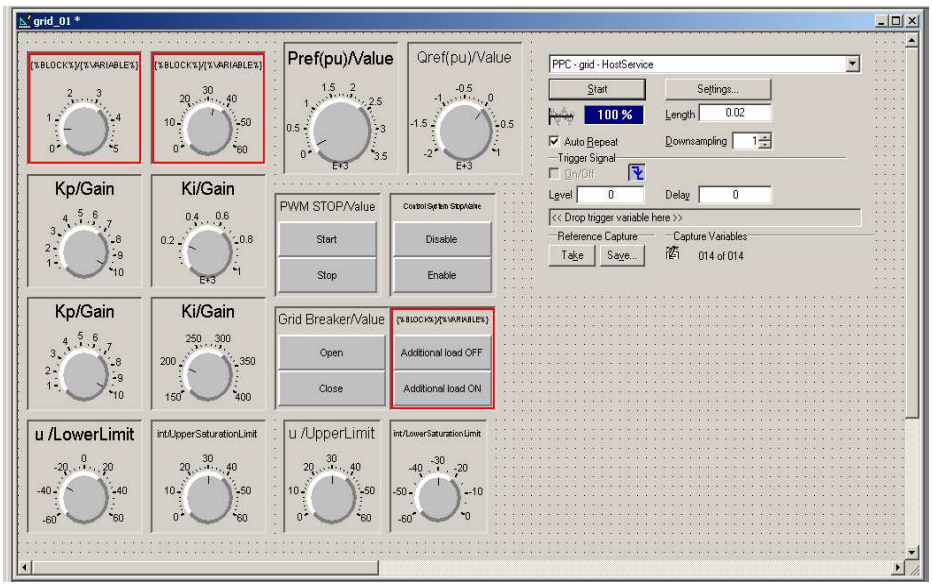

Figure 4.20 Control Desk user interface.

4.7 Conclusion

The prototype construction and testing has been performed stage by stage in the following sequence, in order to prepare the system to be able to run the experiments:

- Building of the interface circuits and testing;
- Building of the main components of the inverter system, cabinet and testing;
- Software development, testing and interaction with hardaware;
- Procurement of the cabinet, components, materials and tools;
- Wiring and marking;

This work on the prototype construction, involved practical experience and required manufacturing and engineering skills such as mounting, assembling, wiring, programming and testing.

Testing of the prototype was done in a systematic manner. Each section and component was tested individually before putting them together. Debugging of certain problems was time consuming but was adopted in a modular fashion to achieve goals.

Next chapter will present experimental results which is the logical end of all work and analysis presented in first four chapter.

CHAPTER 5
EXPERIMENTAL RESULTS

5.1 Objective

This chapter shows different experiments that have been done in order to support the a simulation results presented earlier and test overall system. It consists of four sections: the first and second ones contain case studies that support the control design and the LCL filter performance for the standalone mode and grid connected mode operation. The third part contains experiment of ride-through operation, and the system response when the inverter transits to standalone from grid connected mode. The last section contains further results evaluation and discussions.

5.2 Stand Alone Mode Operation

The stand-alone mode test were done with maximum available resistive load in the laboratory, which is around 1.2 kW. Unfortunately inductive and capacitive load was not available in the laboratory. In order to test inverter operation with nonlinear load three phase diode rectifier with approximately 300 W DC load was connected.

Figure 5.1 shows the data captured from the Fluke 43B Power Quality Analyzer. It can be seen that the inverter operating under nominal voltage conditions with nominal frequency 60Hz and providing 1.2 kW with PF=1 (power quality analyzer measures single phase power). THD of current is 0.3%, so the inverter providing clean sinusoidal voltage.

All other data, which shows the controller performance and three phase values are captured with Control Desk dSPACE software.

It can be seen from Figure 5.5 and Figure 5.6, that V_d component which is extracted from the three phase grid voltage is followed very good and error fluctuates around zero, however V_q component has constant error and PI controller of voltage control system can't reach zero error due to unbalanced and distorted grid voltage. For the purpose of successful extraction of V_d and V_q and minimize grid disturbance influence positive sequence detector was implemented as discussed in Chapter 3.

5.2.1 Voltage Step Response

During this experiment reference phase voltage was changed with step command from 100 V peak value to 170 V peak and back. It can be seen that controller has good performance and follows the reference command.

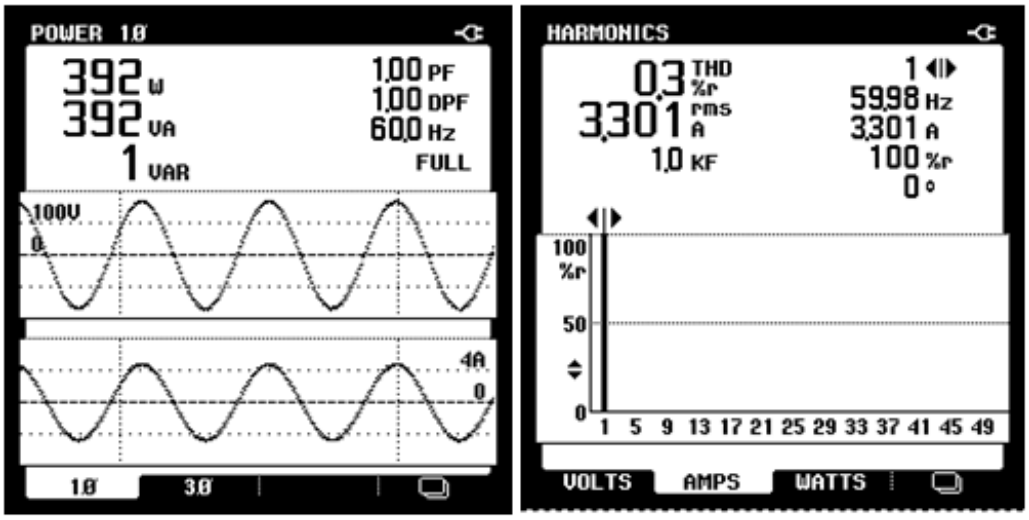

Figure 5.1 Power quality analyzer data: (a) phase A voltage, current waveforms and single phase power; (b) THD of load current.

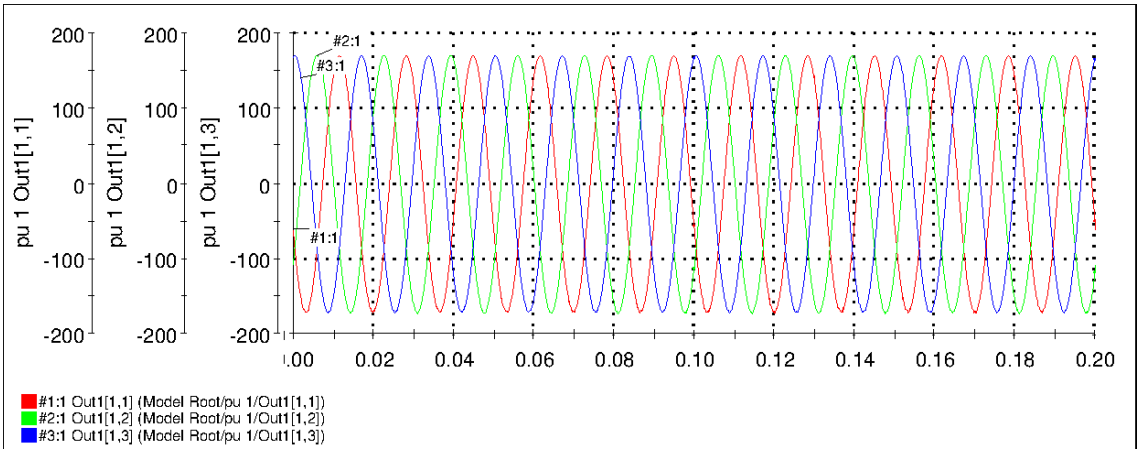

Figure 5.2 Phase voltages measured at load terminals.

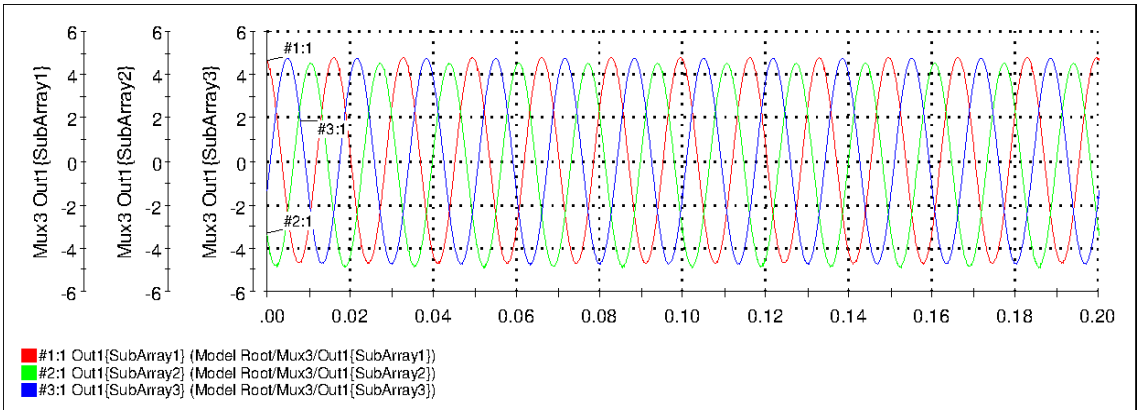

Figure 5.3 Line currents measured at load terminals.

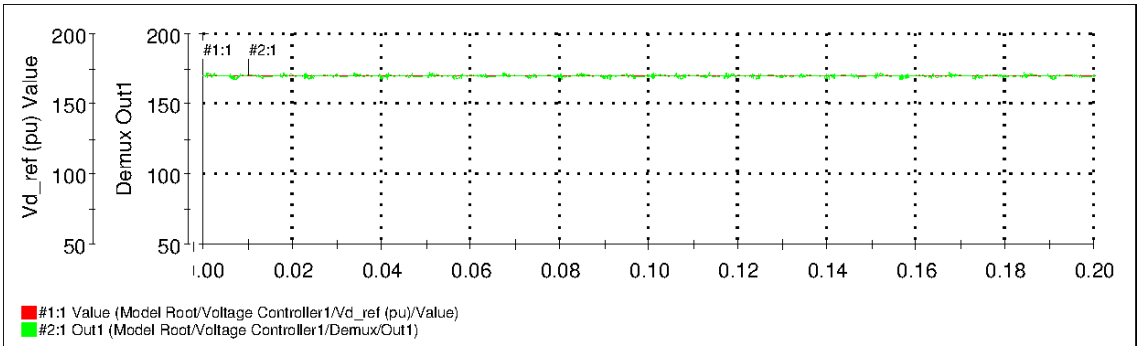

Figure 5.4 V_d and V_{dref} (V).

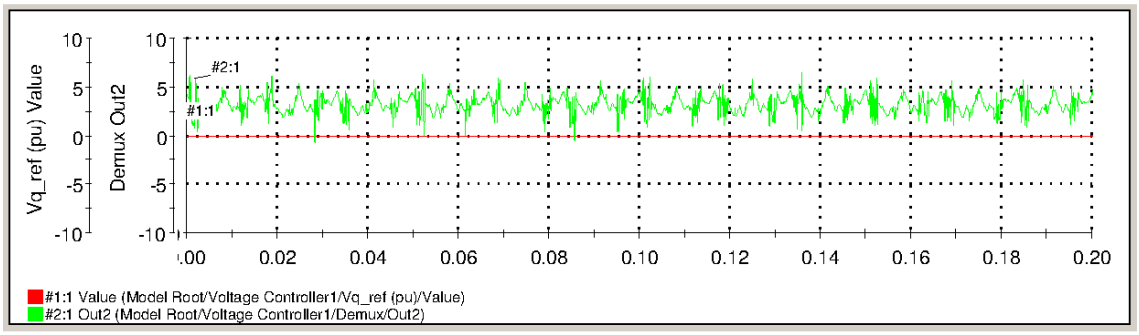

Figure 5.5 V_q and V_{qref}(V).

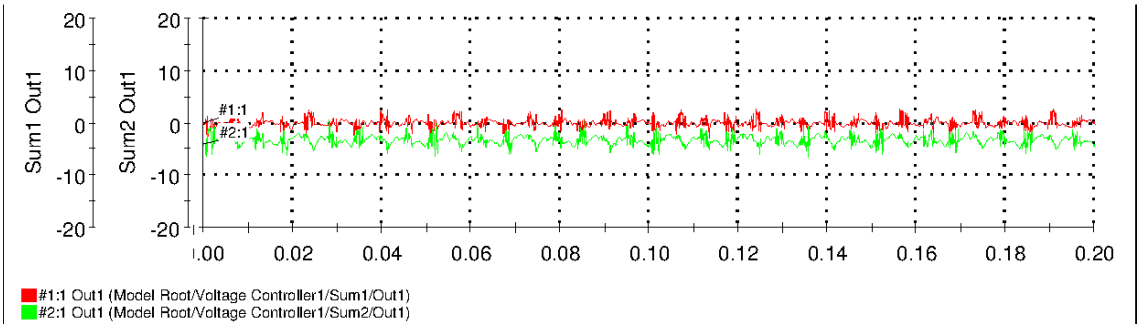

Figure 5.6 V_d and V_q error.

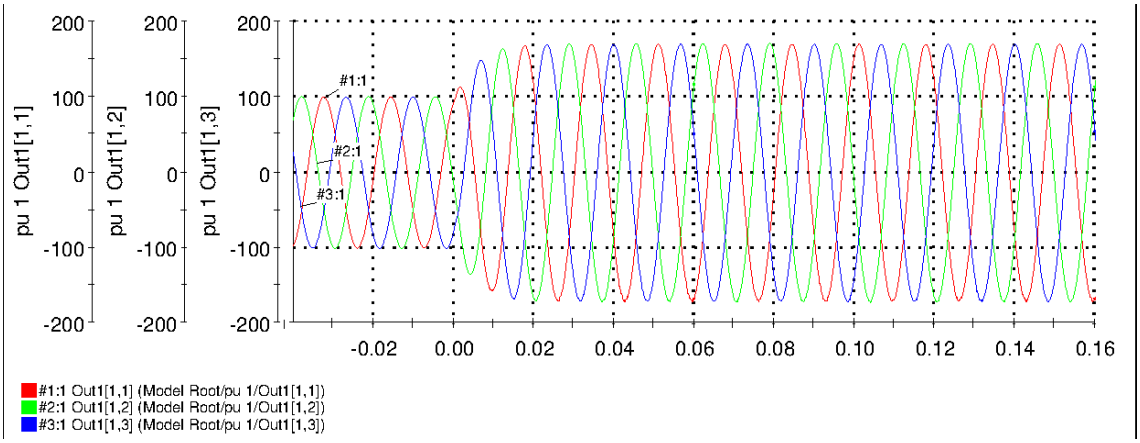

Figure 5.7 Phase voltages measured at load terminals.

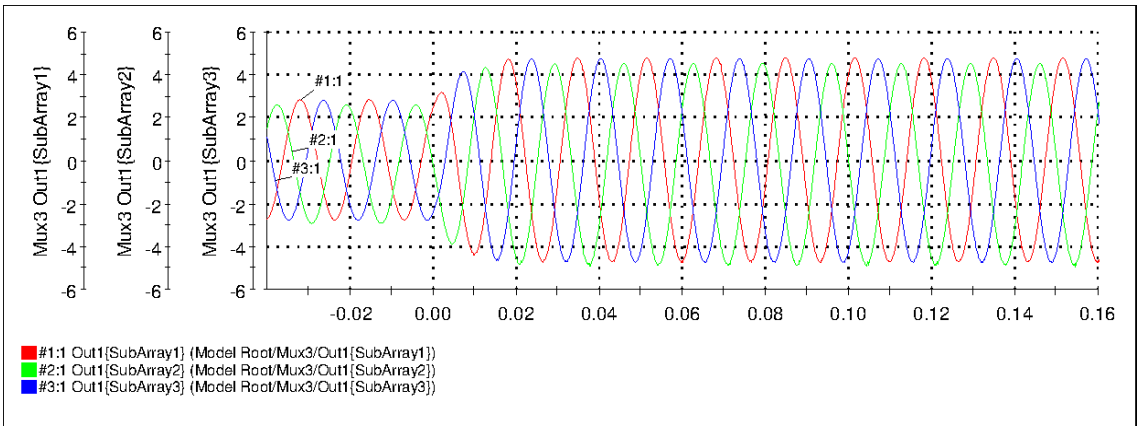

Figure 5.8 Line currents measured at load terminals.

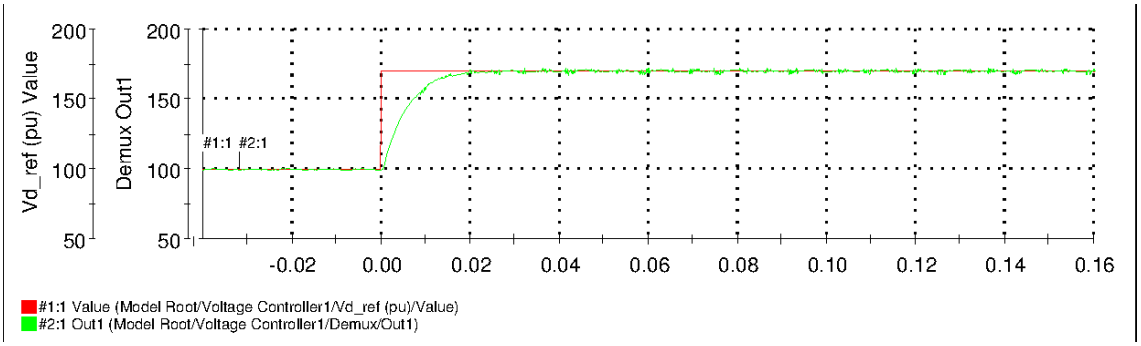

Figure 5.9 V_d and V_{dref}.

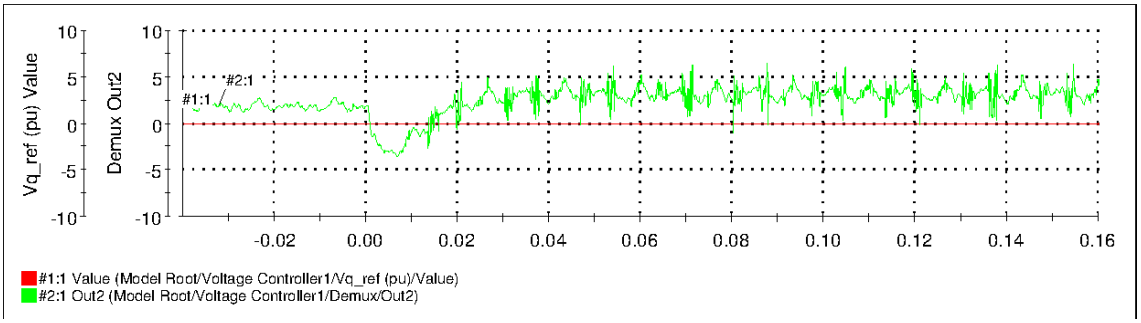

Figure 5.10 V_q and V_{qref}.

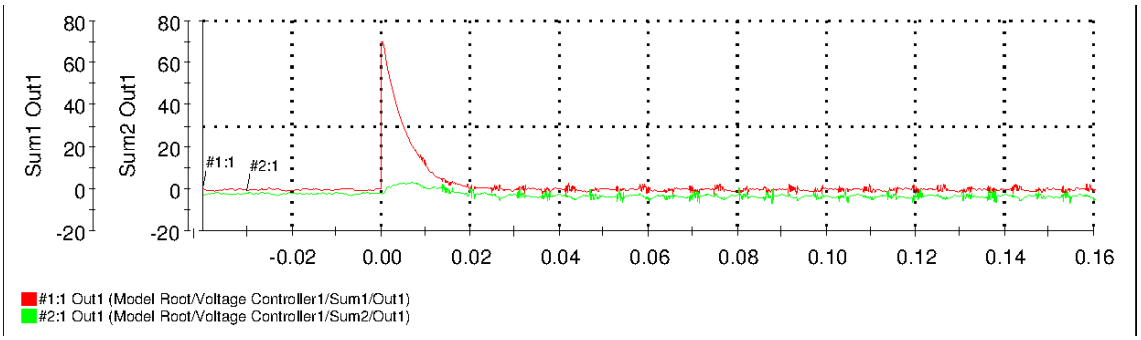

Figure 5.11 V_d and V_q error.

Figure 5.12 - Figure 5.16 show the inverter operation when the reference phase voltage was changed with step command from 170 V peak value to 100 V.

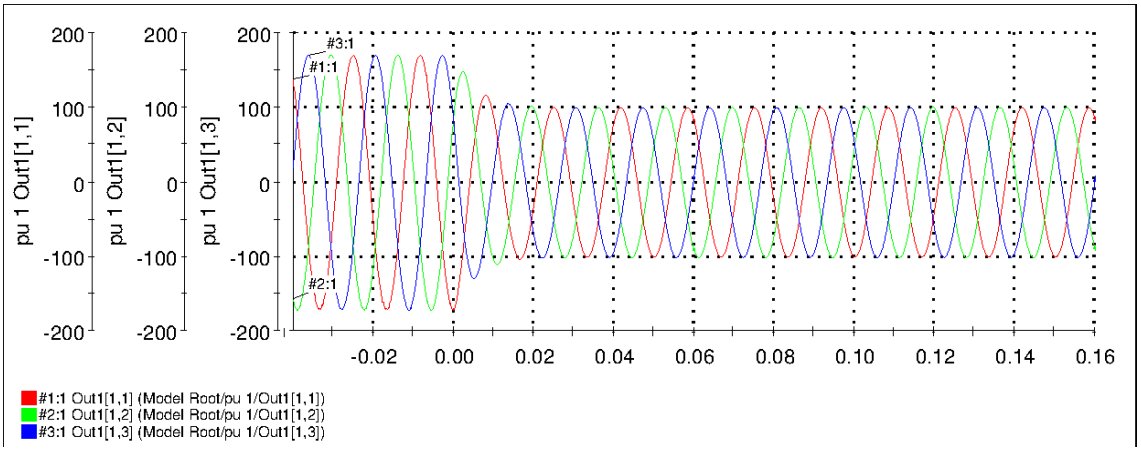

Figure 5.12 Phase voltages measured at load terminals.

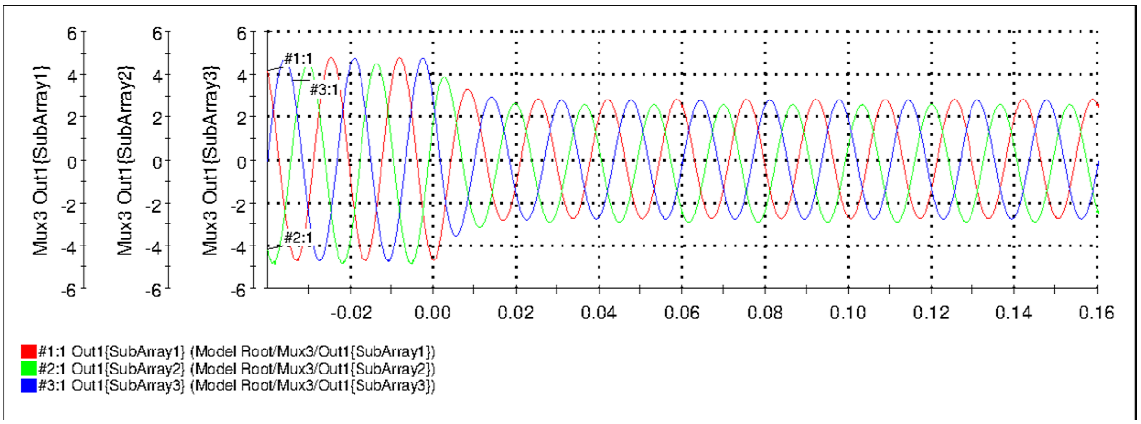

Figure 5.13 Line currents measured at load terminals.

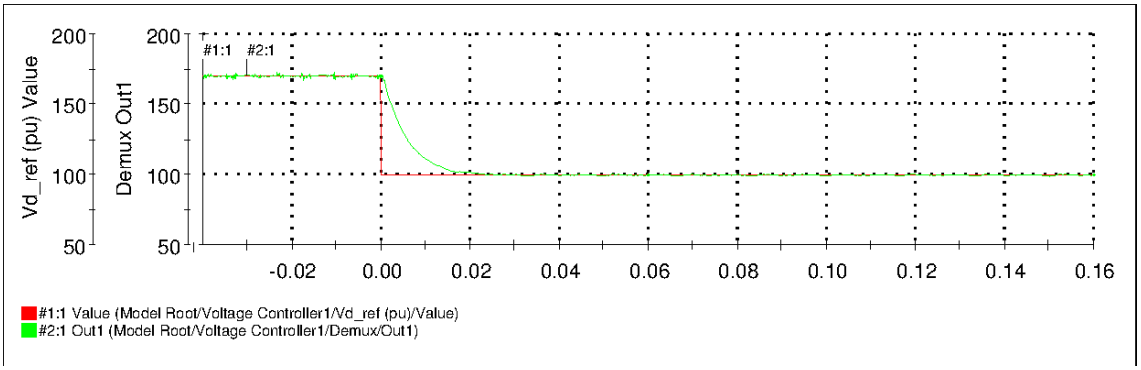

Figure 5.14 V_d and V_{dref}.

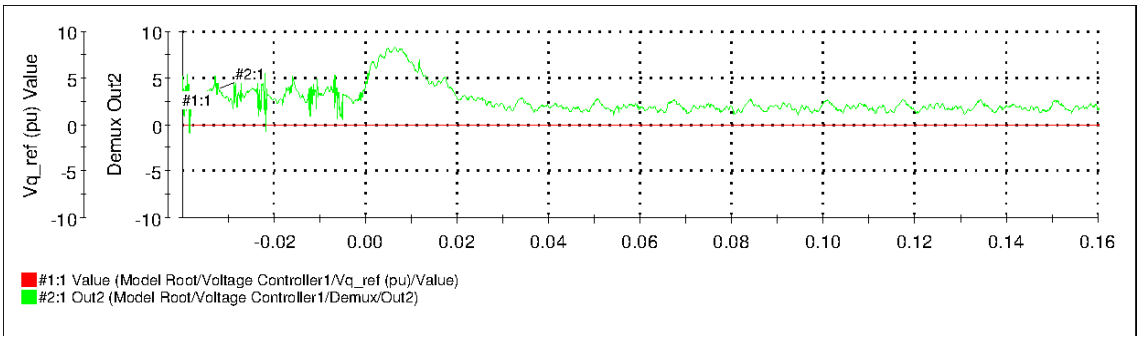

Figure 5.15 V_q and V_{qref}.

5.2.2 Load Step Change Response

During this experiment inverter at the beginning operating with 500 W load, then there is a command and additional 700 W load is connected, after some time this load is disconnected.

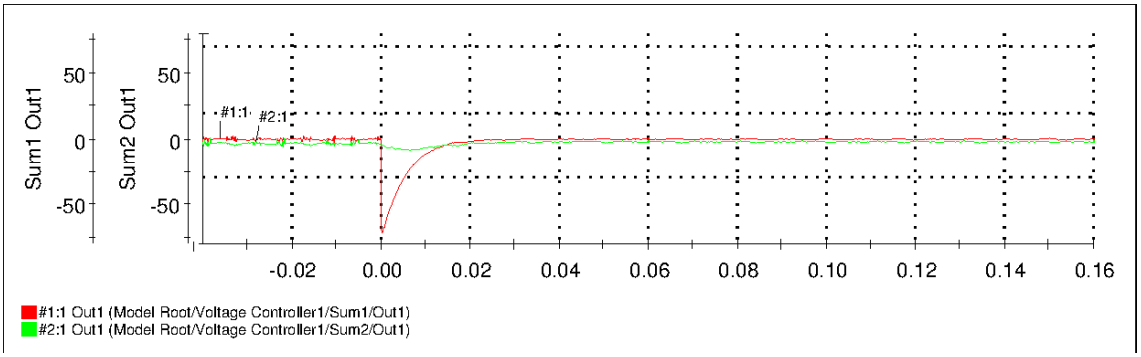

Figure 5.16 V_d and V_q error.

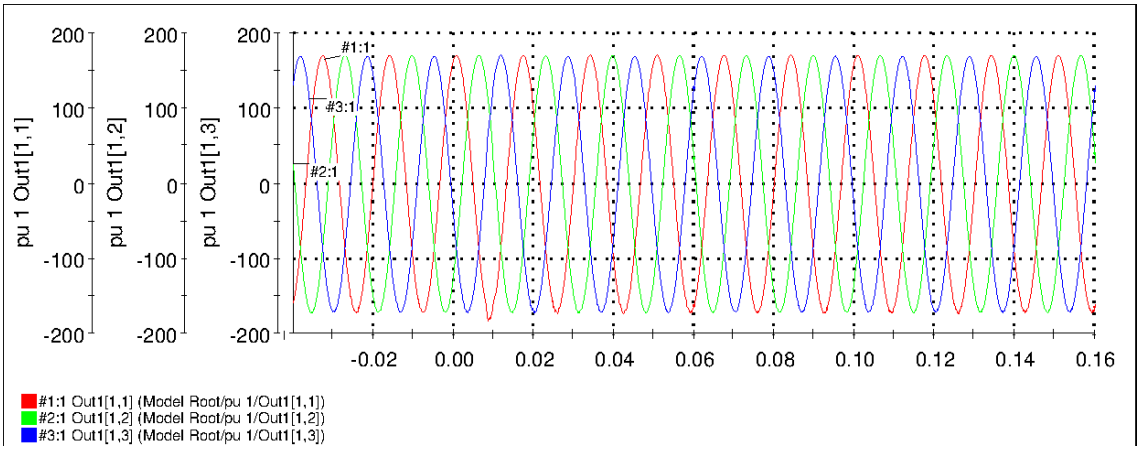

Figure 5.17 Phase voltages measured at load terminals.

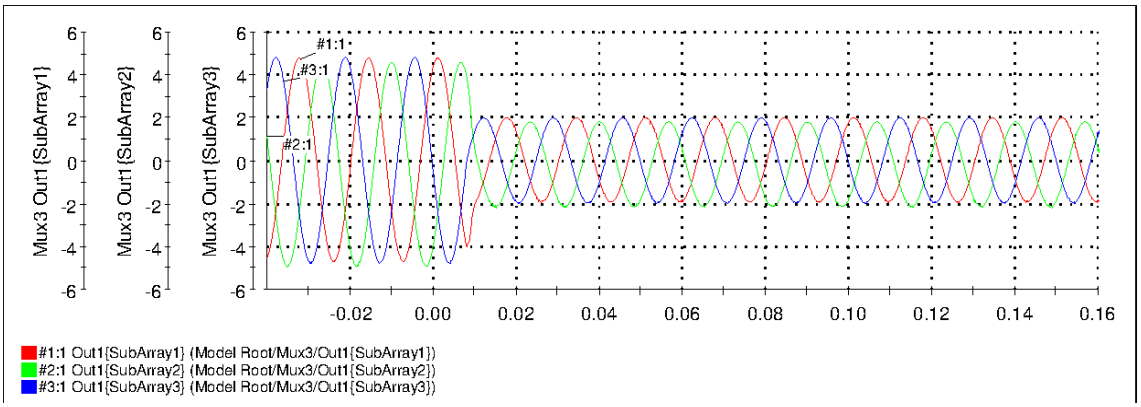

Figure 5.18 Line currents measured at load terminals.

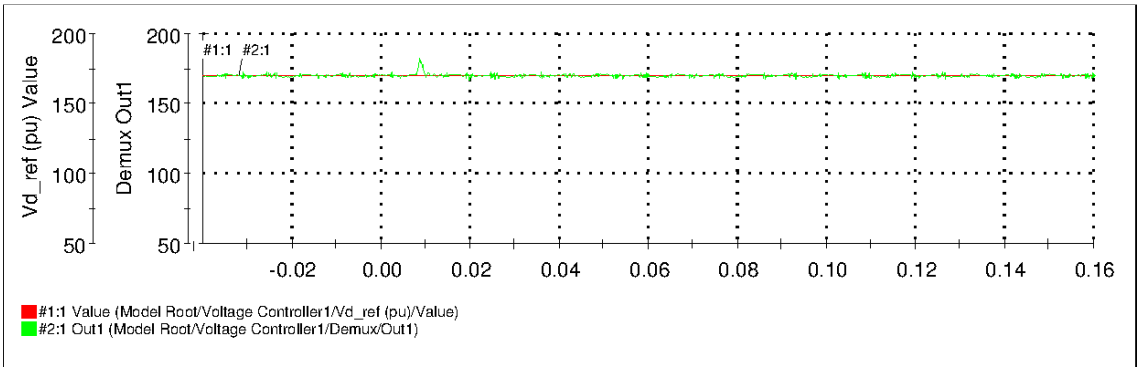

Figure 5.19 V_d and V_{dref}.

Figure 5.20 and Figure 5.21 show that with positive sequence detector PI controller of voltage control system works much better and able to regulate V_q component around zero.

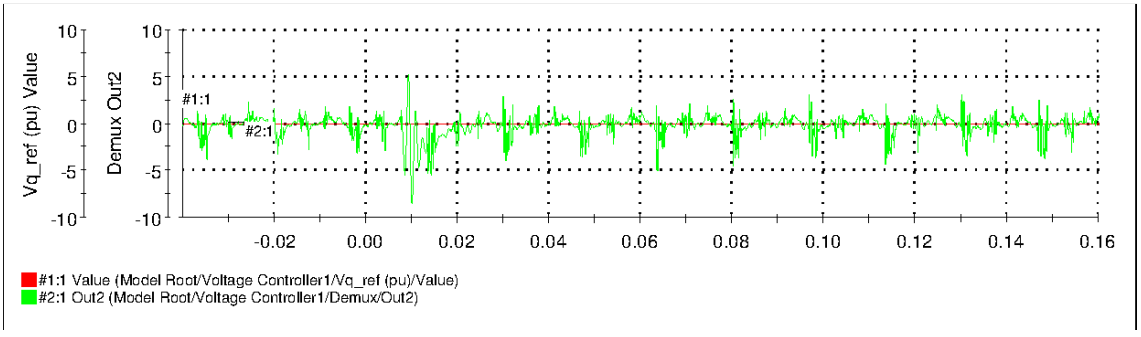

Figure 5.20 V_q and V_{qref}.

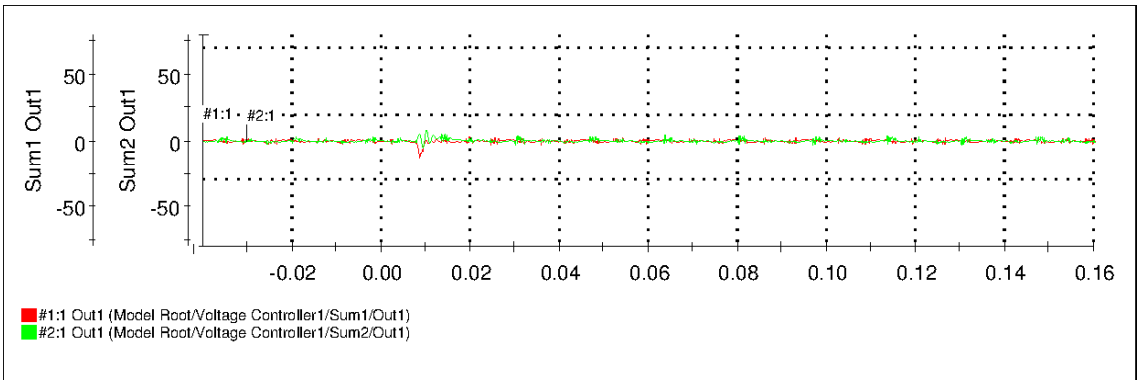

Figure 5.21 V_d and V_q error.

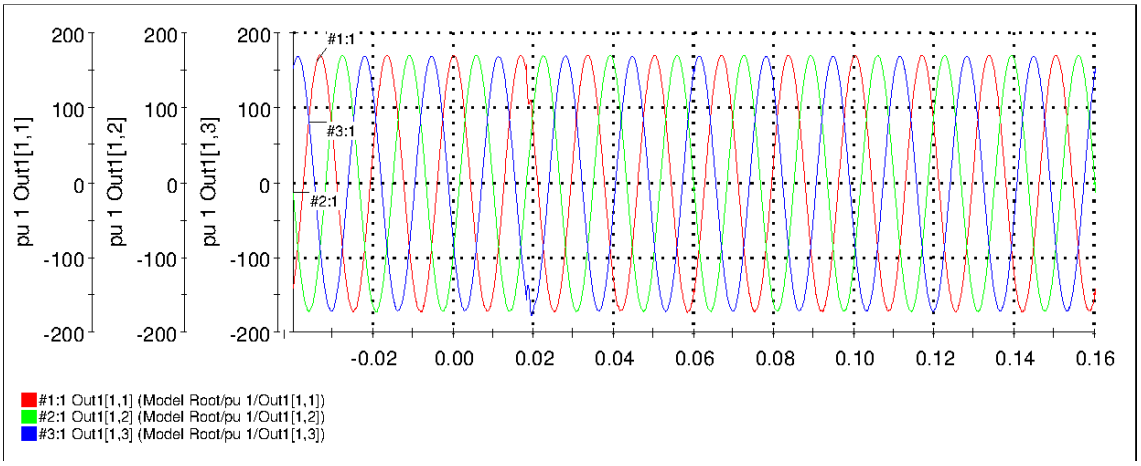

Figure 5.22 Phase voltages measured at load terminals.

Also it can be seen from Figure 5.22 that generated voltages in stand alone mode are completely balanced because of reference V_d and V_q used from positive sequence detector.

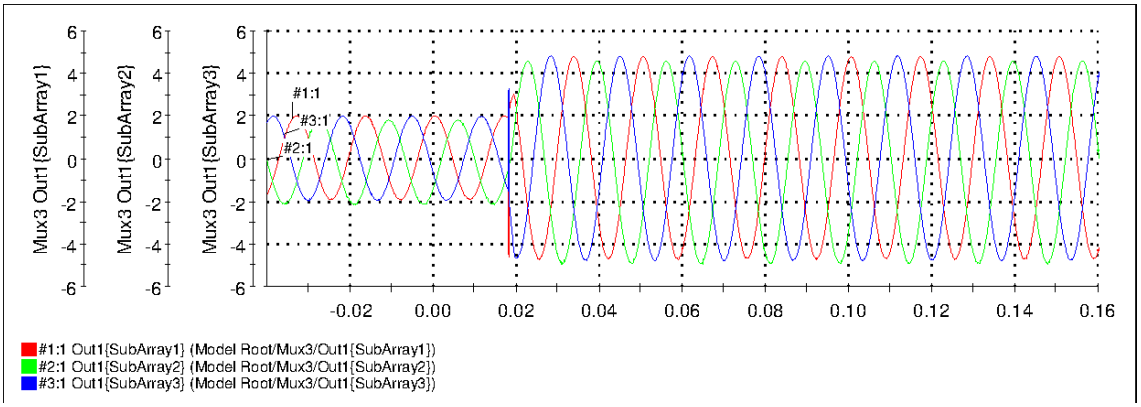

Figure 5.23 Line currents measured at load terminals.

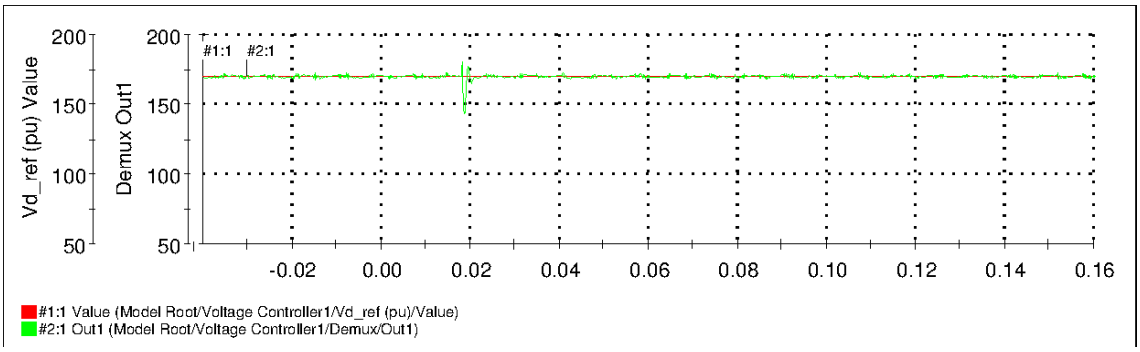

Figure 5.24 V_d and V_{dref}.

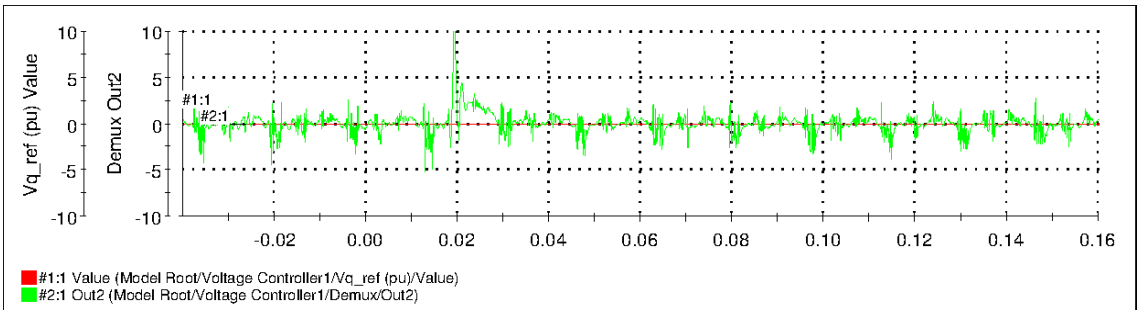

Figure 5.25 V_q and V_{qref}.

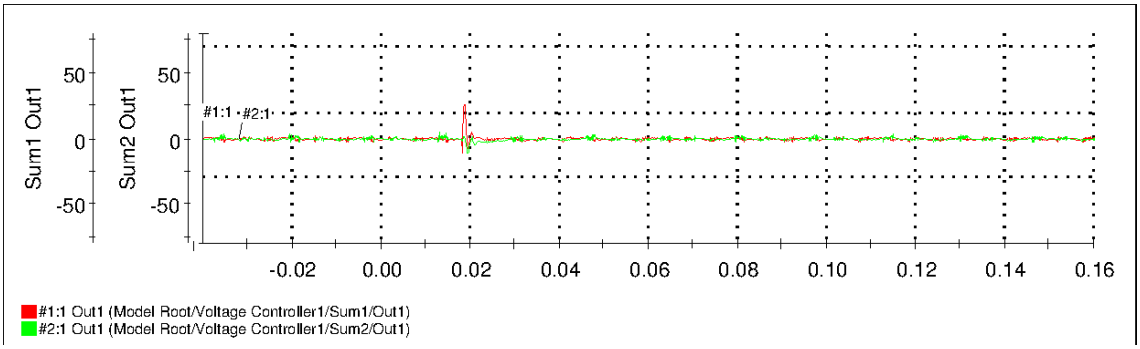

Figure 5.26 V_d and V_q error.

5.2.3 Stand Alone Mode Operation with Nonlinear Load

This test was done with maximum available resistive load in the laboratory, which is around 1.2 kW and around 300 W of load which was connected through three phase diode rectifier.

It can be seen from this experiment that inverter output voltage doesn't have pure sinusoidal form. Figure 5.27 shows that the voltage distortion is caused by highly distorted load current, which has large 5th and 7th harmonic content.

5.3 Grid-Connected Mode

For all grid-connected mode experimental results inverter was connected straight to three phase receptacle available in the Power Electronics Laboratory of the Department of Electrical Engineering and Computer Science on the third floor.

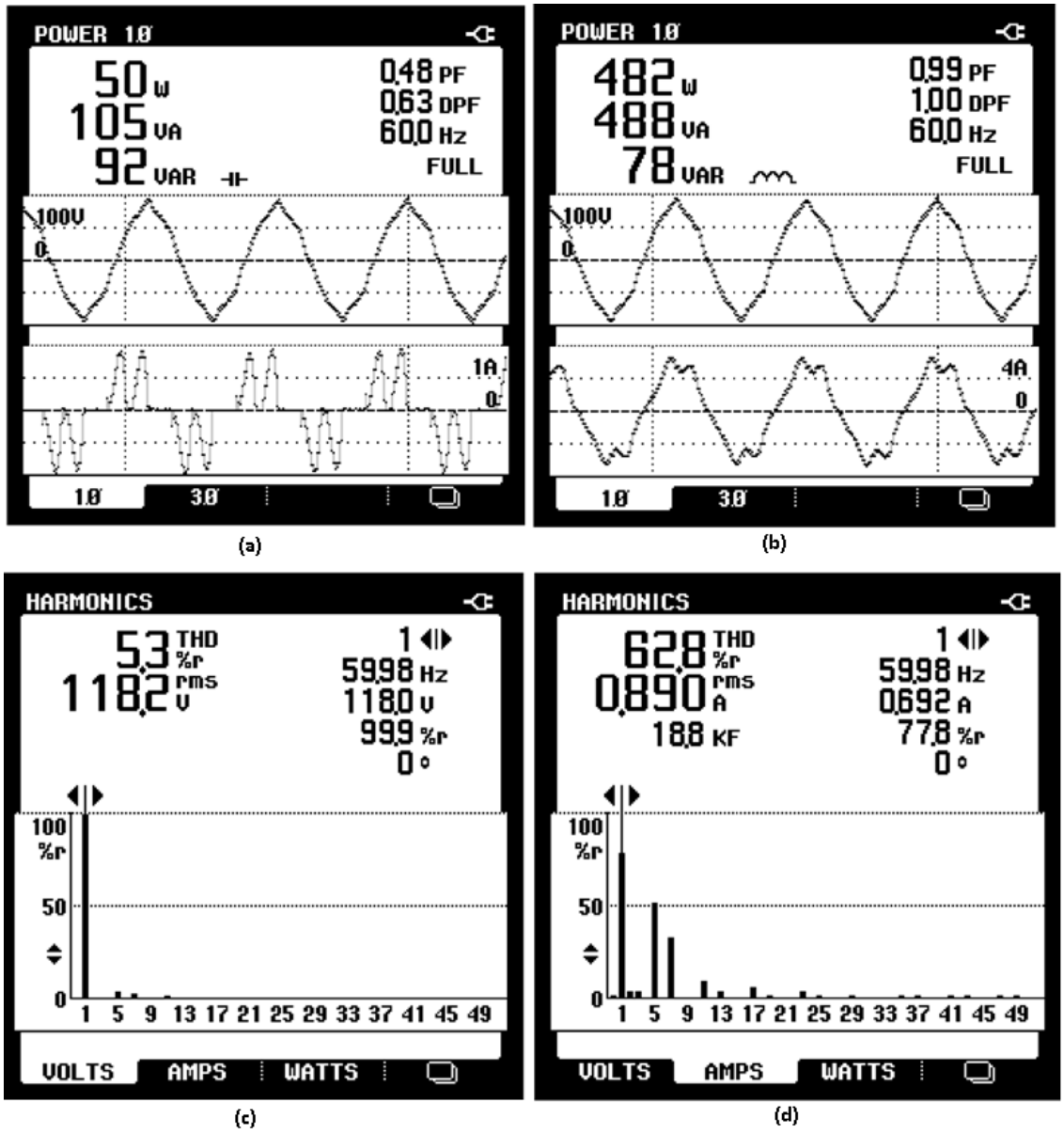

Figure 5.27 Power Quality Analyzer data: (a) phase A voltage and current and single phase power for nonlinear load; (b) phase A voltage and current and single phase power for total load; (c) THD for voltage output; (d) THD for nonlinear load current.

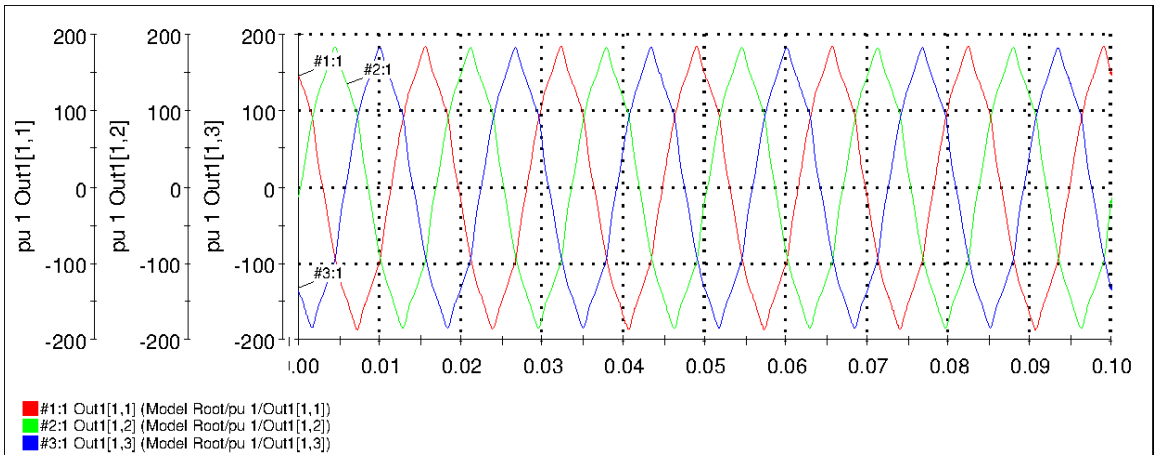

Figure 5.28 Phase voltages measured at load terminals.

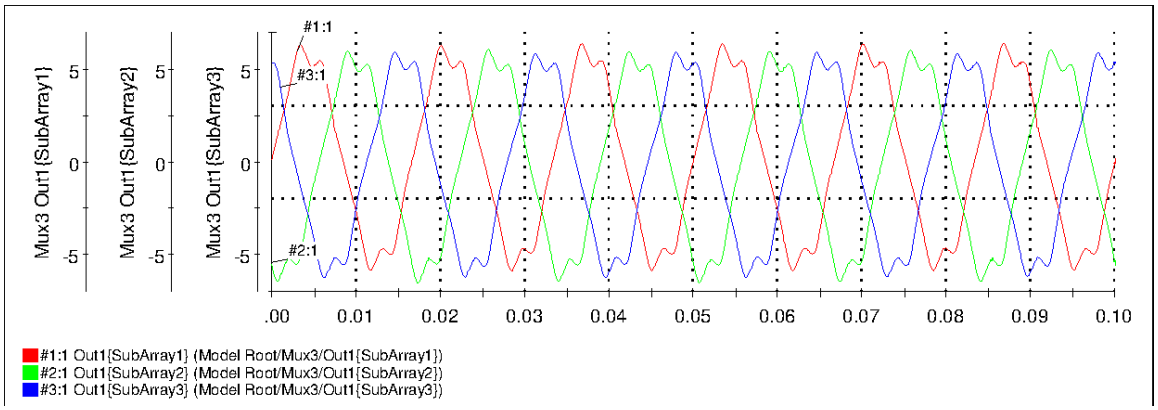

Figure 5.29 Line currents measured at load terminals.

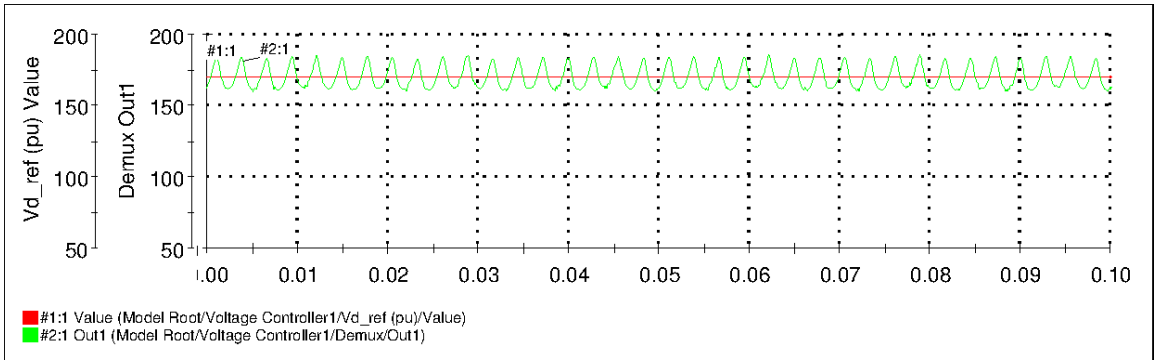

Figure 5.30 V_d and V_{dref}.

Grid conditions and power quality of grid voltage was analyzed before connecting inverter to the grid with available tools and meters in the laboratory. It's clearly seen from Figure 5.33 that grid voltage

before connecting the inverter has high distortion with 5th and 7th harmonics, this was observed during the long and extensive experimental work.

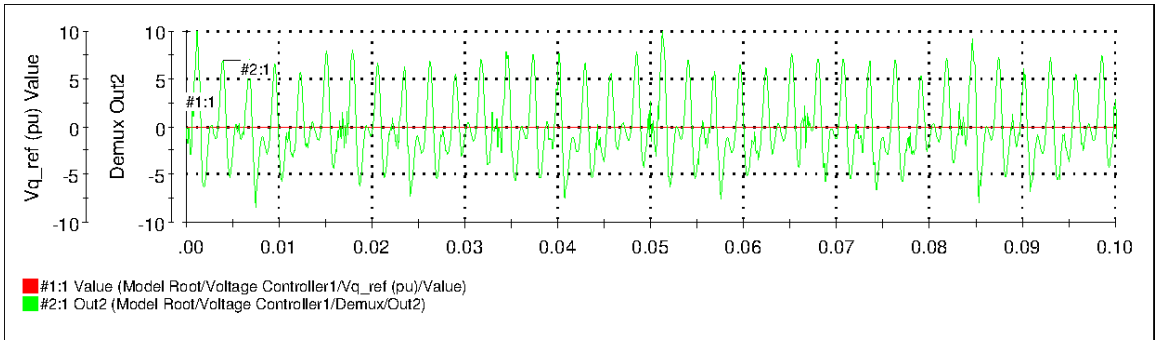

Figure 5.31 V_q and V_{qref}.

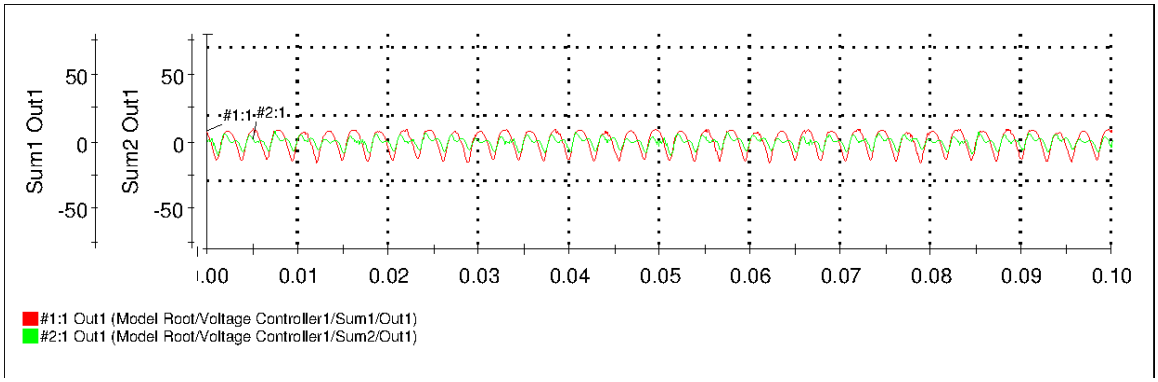

Figure 5.32 V_d and V_q error.

Also the three phase voltage was affected by the operation of HVAC system in the building. When LCL filter is under grid voltage and inverter is not operating THD of grid voltage is lower. This can be explained by Figure 5.34 where it can be seen that LCL filter circuit is consuming highly distorted current with fundamental around 0.7 A RMS, so the LCL filter works as a grid filter.

5.3.1 Active Power Injection to the Grid

In this section results of active power injection to the grid are presented. During the first experiment 3000 W was injected to the grid Figure 5.35 through Figure 5.41 present the data of supplying 3000 W to the grid.

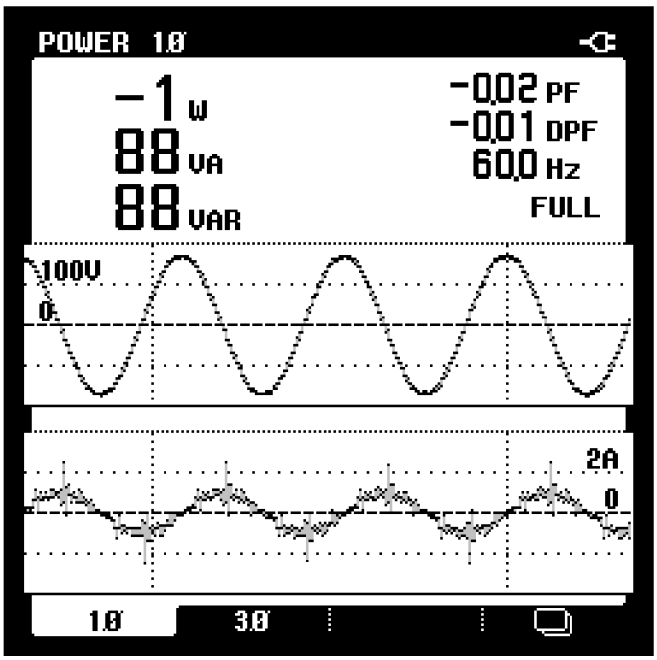

Figure 5.33 Power quality analyzer data: Power consumed by LCL filter.

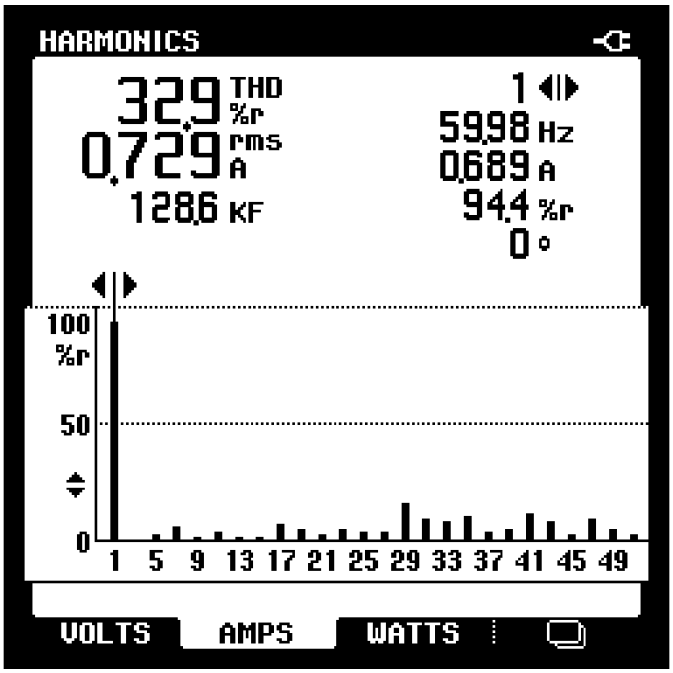

Figure 5.34 THD of current consumed by LCL filter circuit.

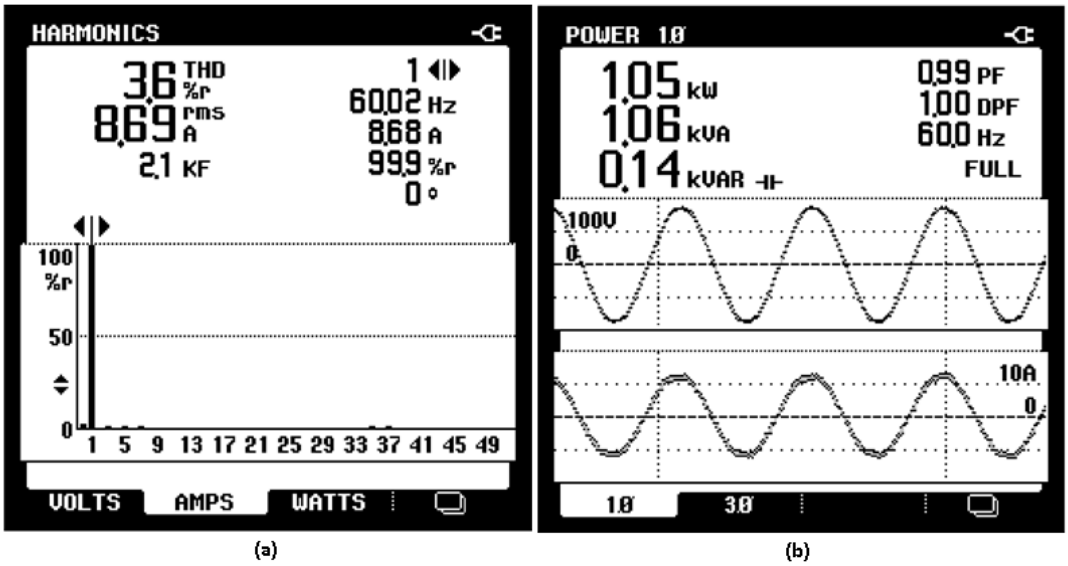

Figure 5.35 Power quality analyzer data: (a)THD of current injected to the grid (b) phase A voltage, current waveforms and single phase power.

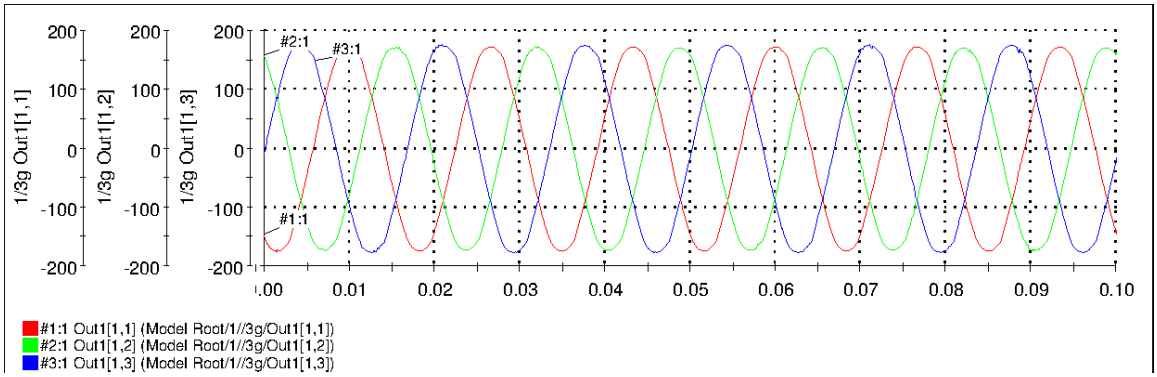

Figure 5.36 Phase voltages measured at load terminals.

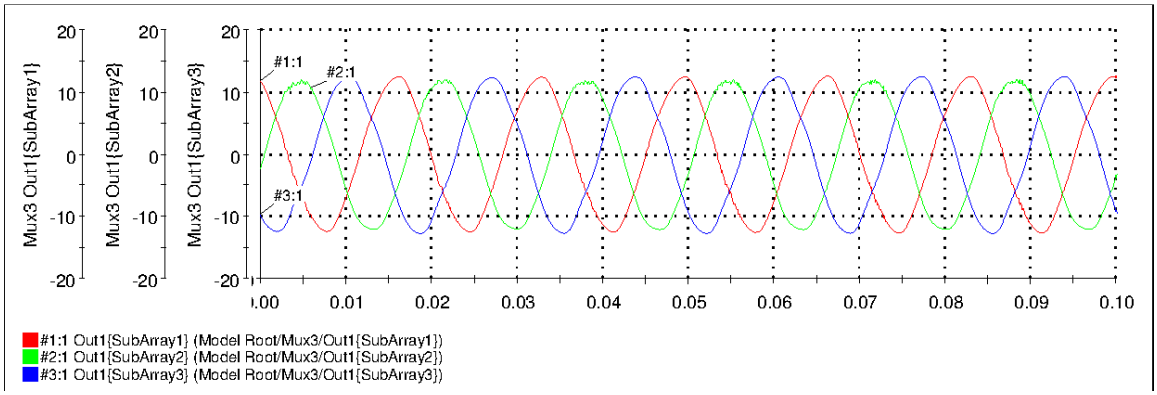

Figure 5.37 Line currents injected to the grid.

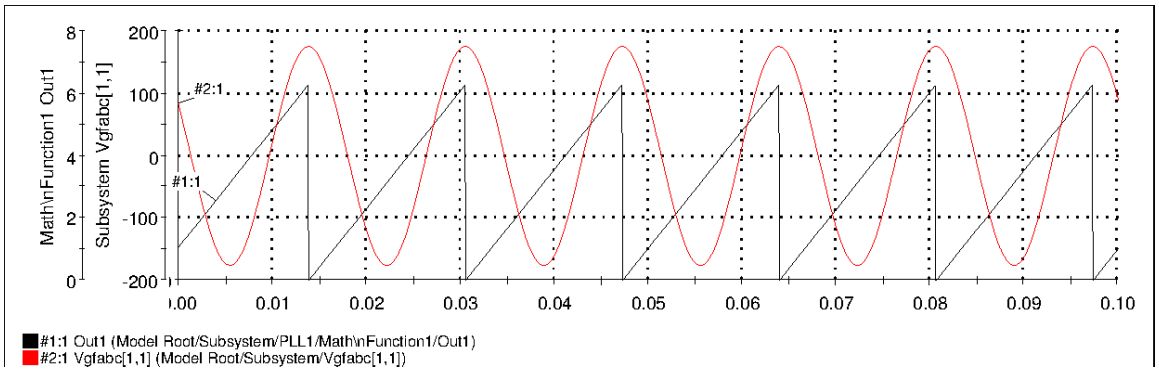

Figure 5.38 PLL operation: v_A(V) and θ.

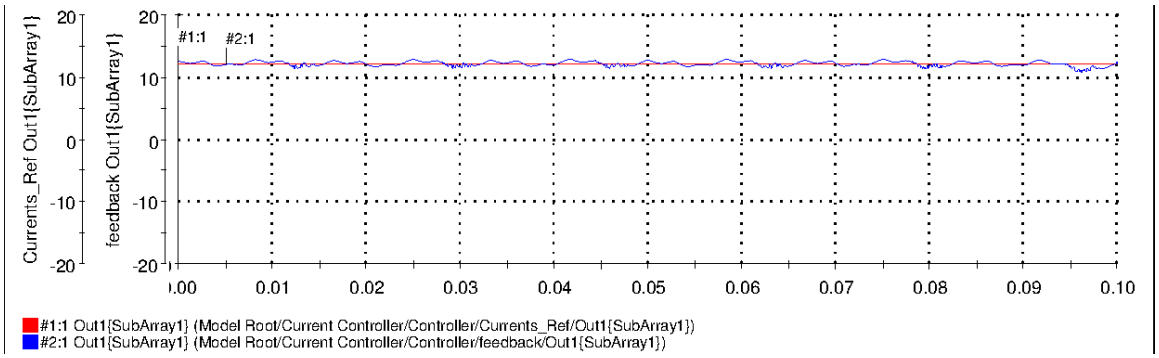

Figure 5.39 I_d and I_{dref}.

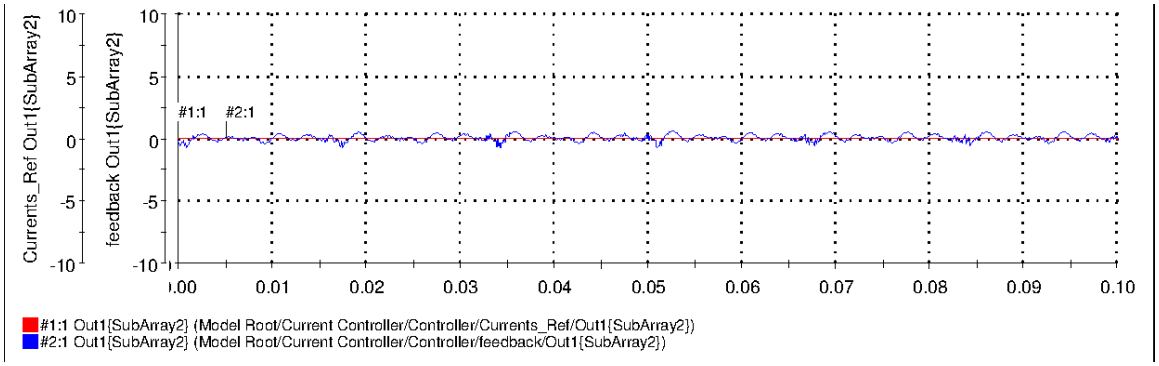

Figure 5.40 I_q and I_{qref}.

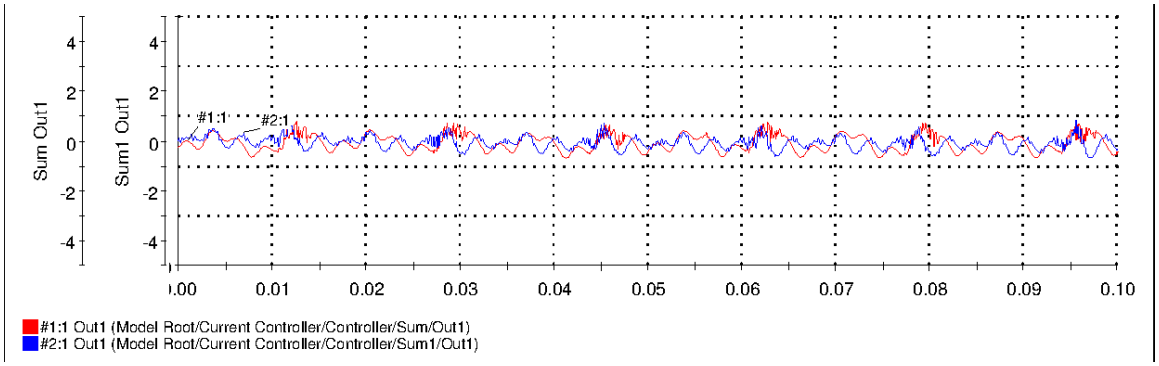

Figure 5.41 I_d and I_q error.

Figure 5.42 through Figure 5.46 shows the control system performance when the inverter injecting 2000 W to the grid.

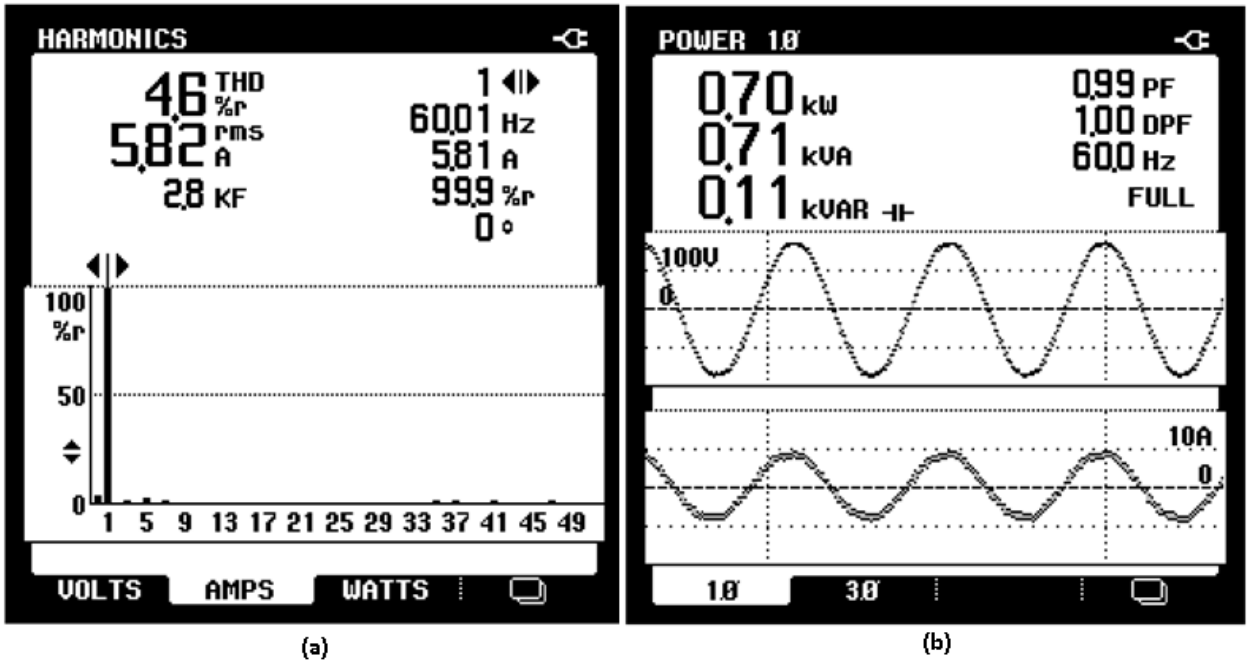

Figure 5.42 Power quality analyzer data: (a)THD of current injected to the grid (b) phase A voltage, current waveforms and single phase power.

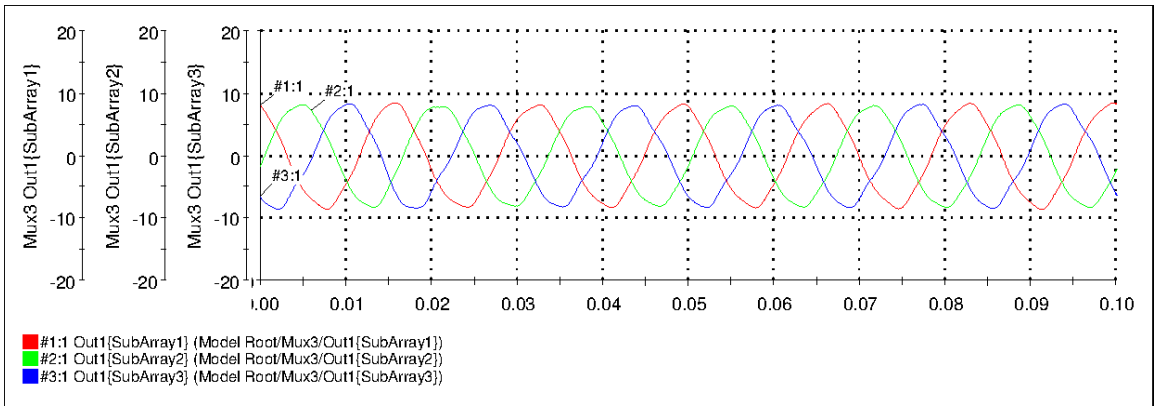

Figure 5.43 Line currents injected to the grid.

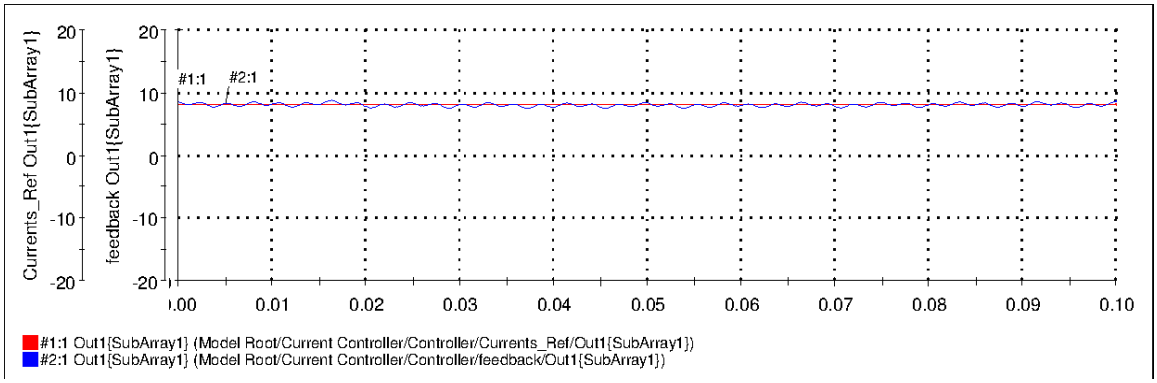

Figure 5.44 I_d and I_{dref}.

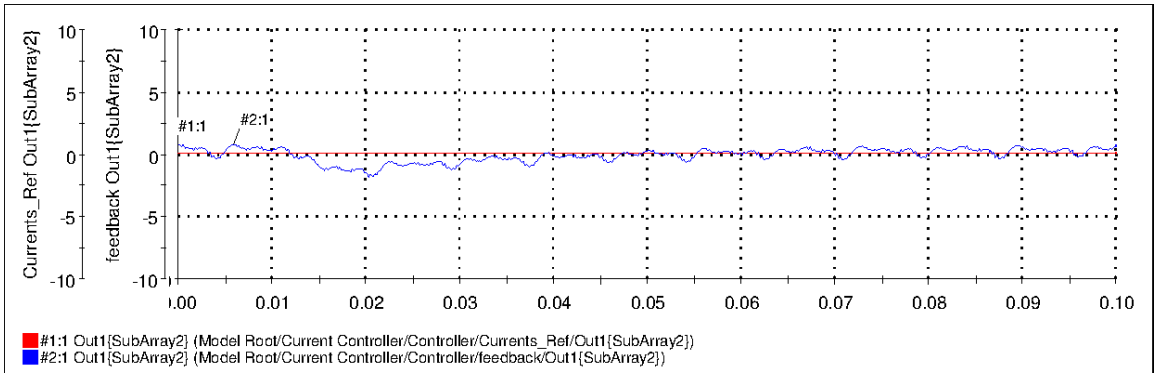

Figure 5.45 I_q and I_{qref}.

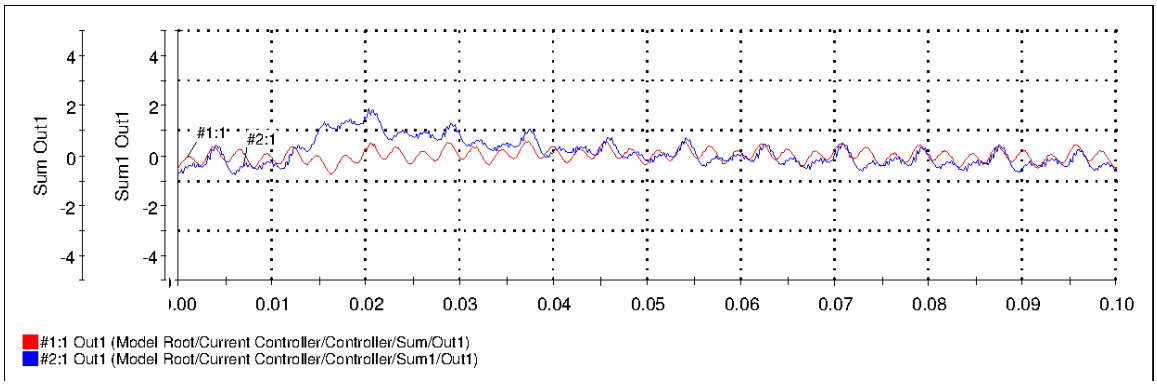

Figure 5.46 I_d and I_q error.

5.3.2 Mixed Power Injection to the Grid

In this section experimental results are presented when inverter injecting mixed power with lagging and leading power.

Figure 5.47 through Figure 5.51 shows the system performance when inverter injecting 3000 W and 1200 Var to the grid.

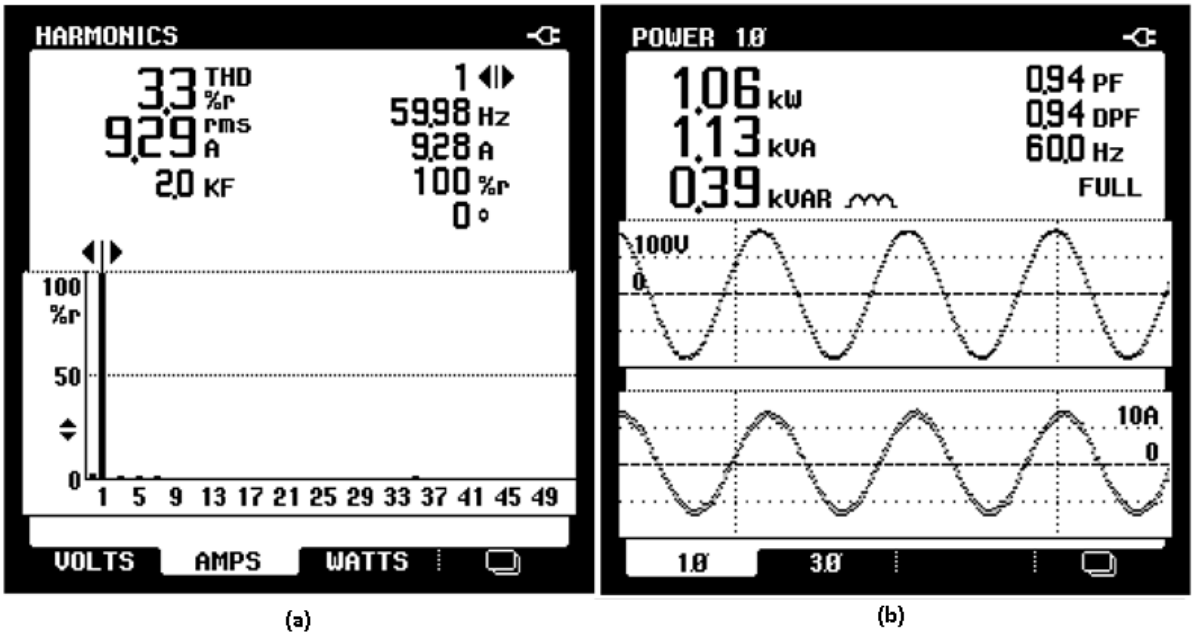

Figure 5.47 Power quality analyzer data: (a)THD of current injected to the grid (b) phase A voltage, current waveforms and single phase power.

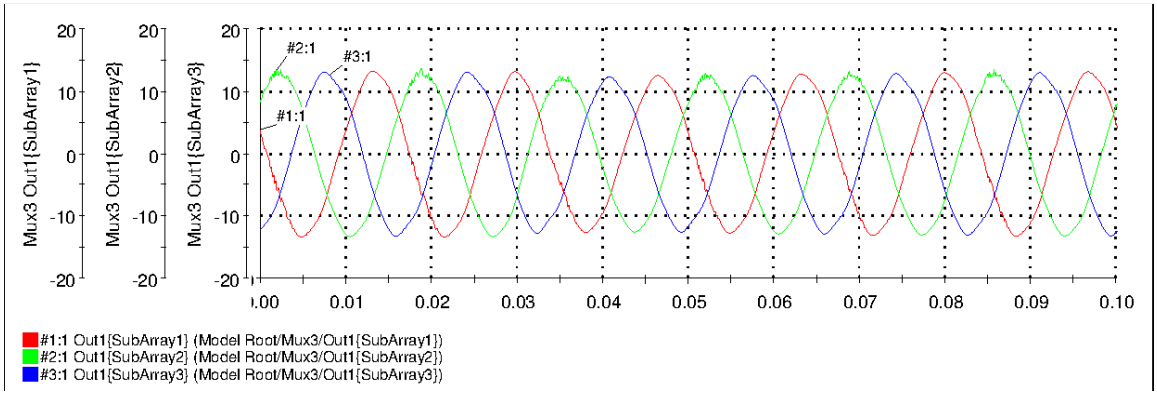

Figure 5.48 Line currents injected to the grid

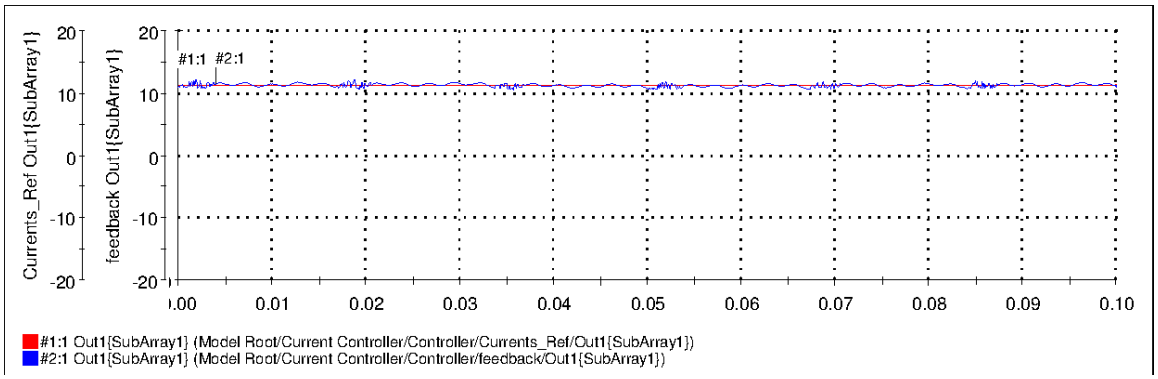

Figure 5.49 I_d and I_{dref}.

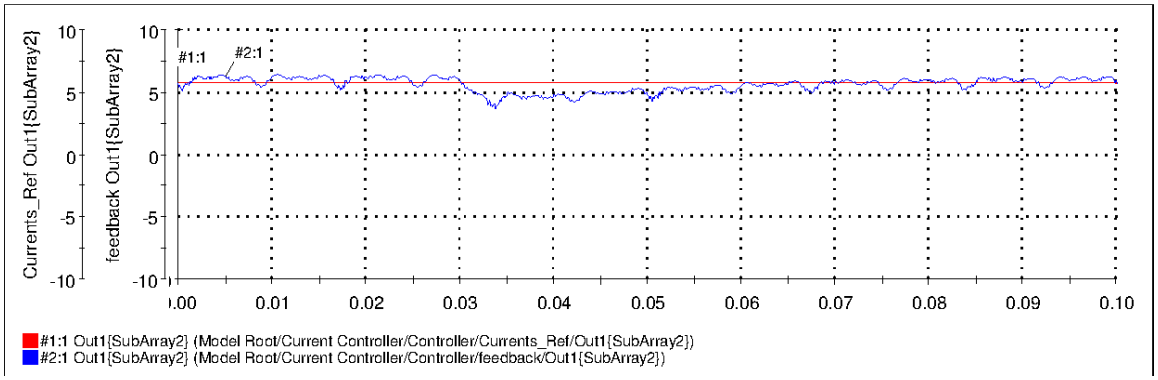

Figure 5.50 I_q and I_{qref}.

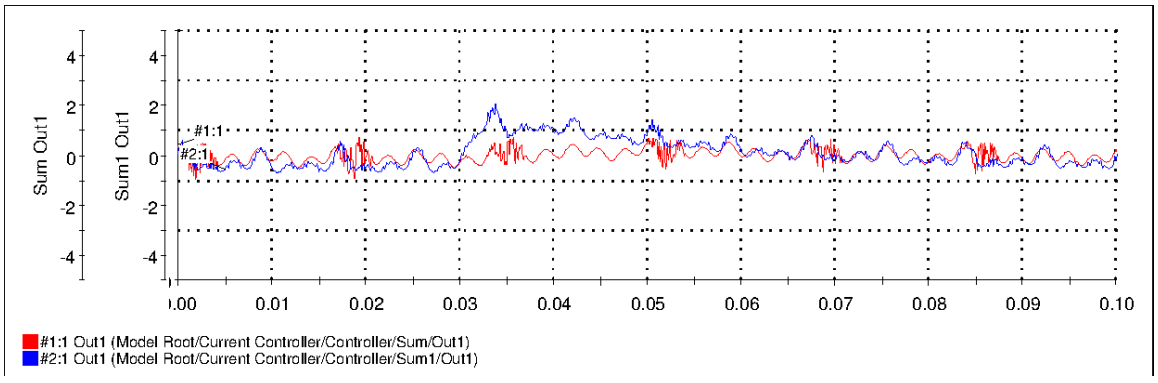

Figure 5.51 I_d and I_q error.

Figure 5.47 through Figure 5.51 shows the system performance when inverter injecting 3000 W and consumes 1200 Var form the grid.

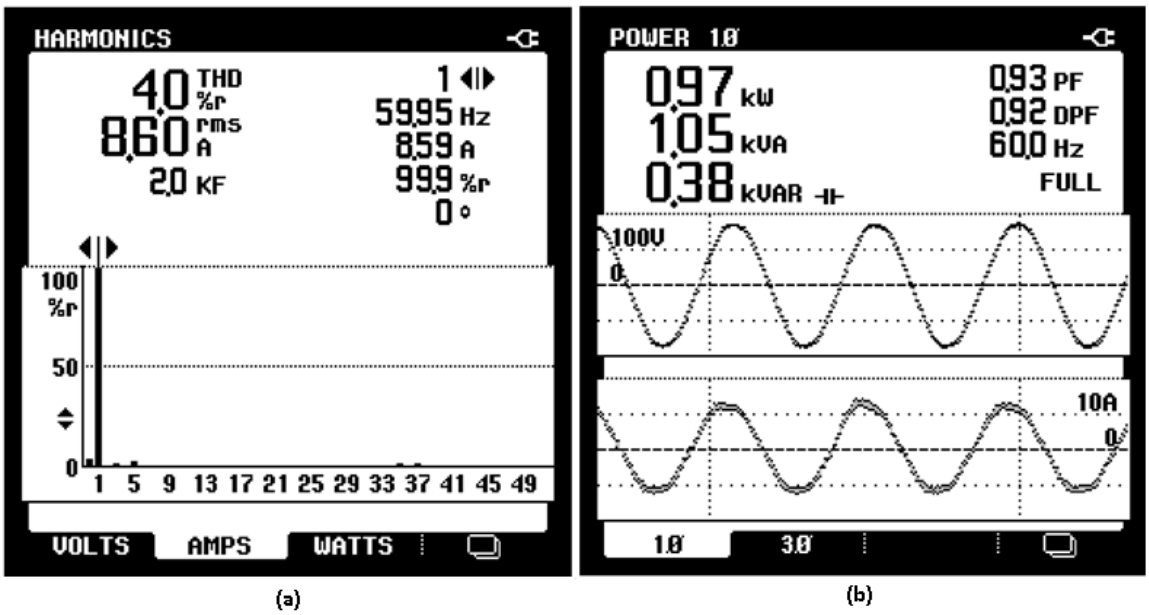

Figure 5.52 Power quality analyzer data: (a)THD of current injected to the grid (b) phase A voltage, current waveforms and single phase power.

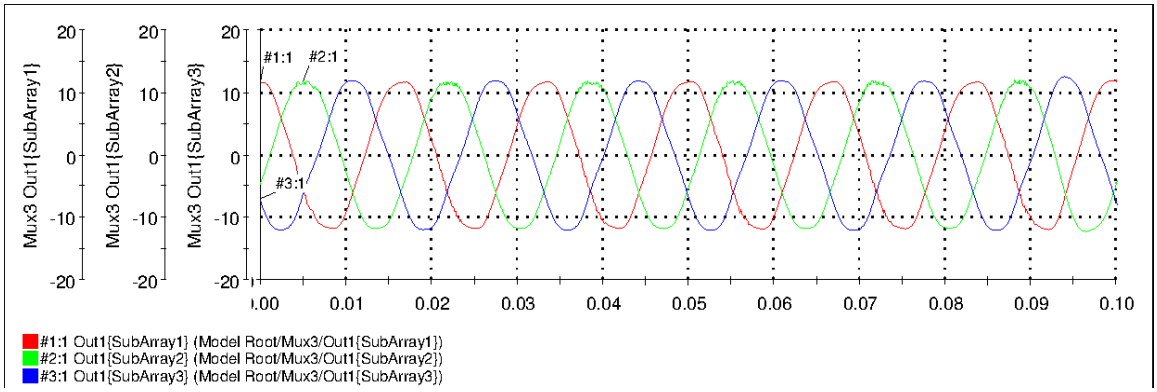

Figure 5.53 Line currents injected to the grid.

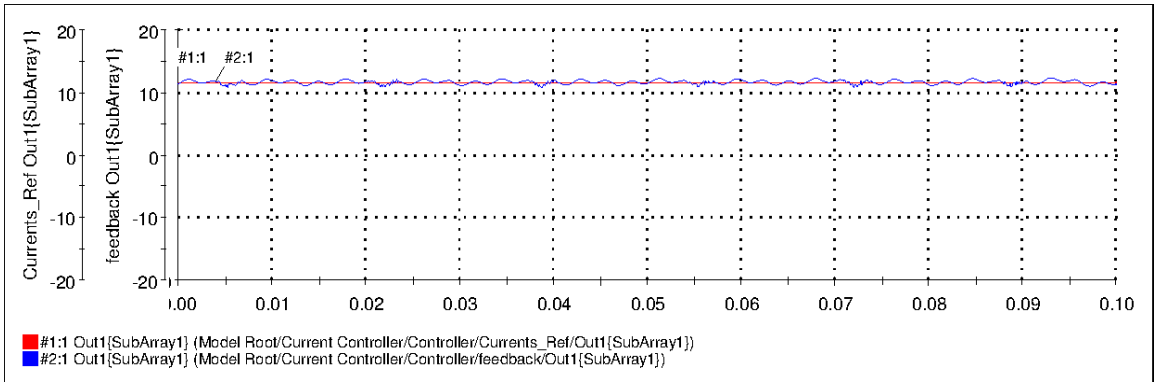

Figure 5.54 I_d and I_{dref}.

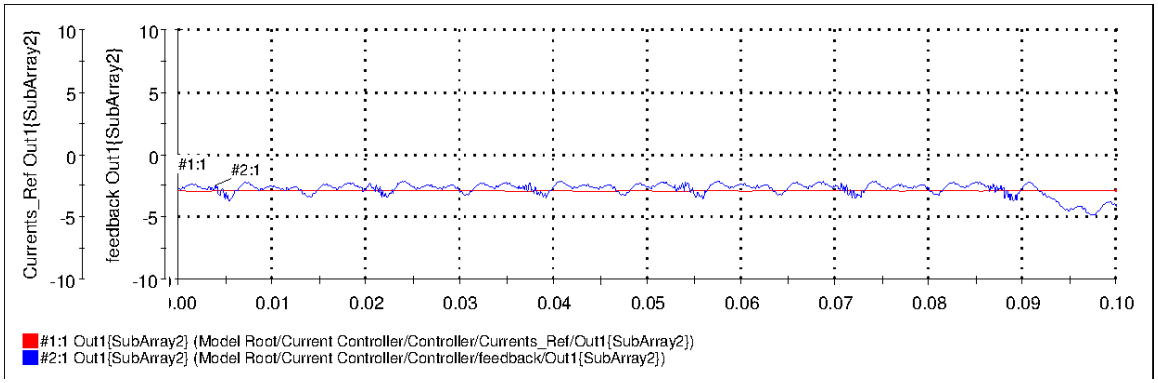

Figure 5.55 I_q and I_{qref}.

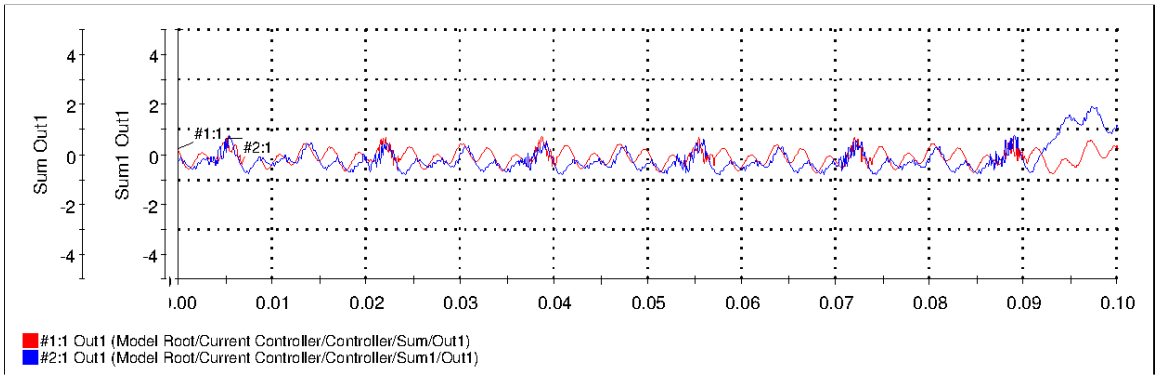

Figure 5.56 I_d and I_q error.

Figure 5.57 through Figure 5.61 show the system performance when inverter injecting 2000 W and 1200 Var to the grid.

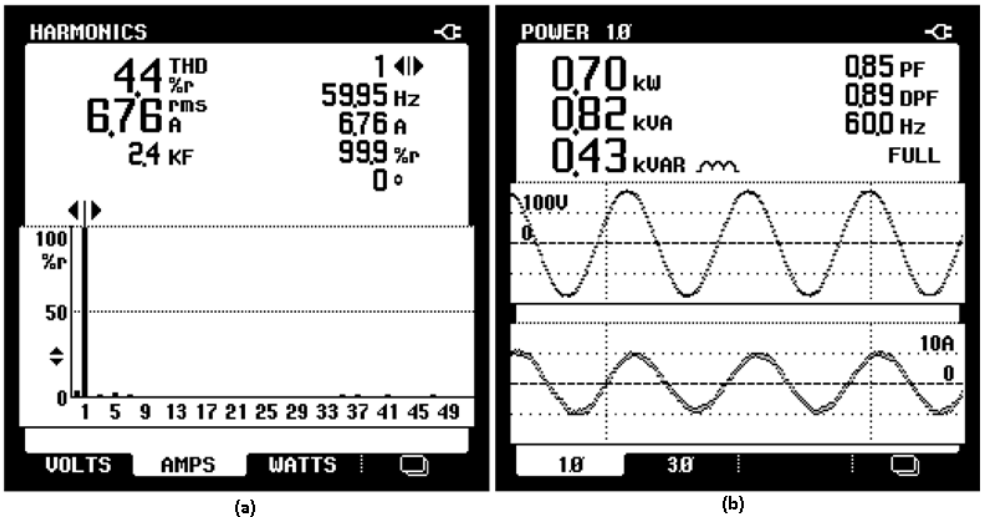

Figure 5.57 Power quality analyzer data: (a)THD of current injected to the grid (b) phase A voltage, current waveforms and single phase power;

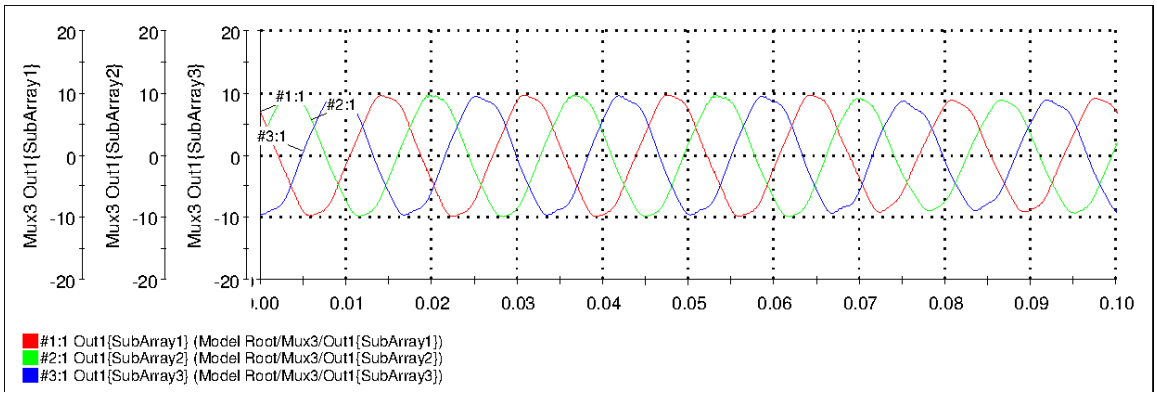

Figure 5.58 Line currents injected to the grid.

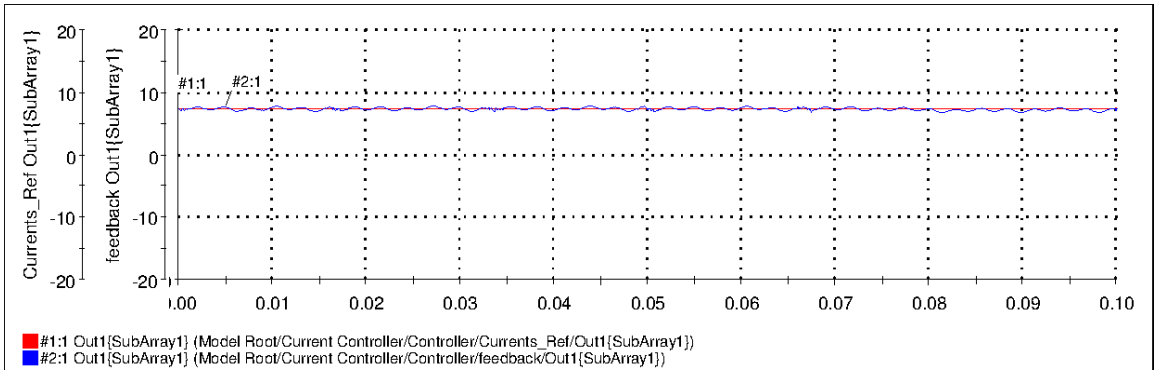

Figure 5.59 I_d and I_{dref}.

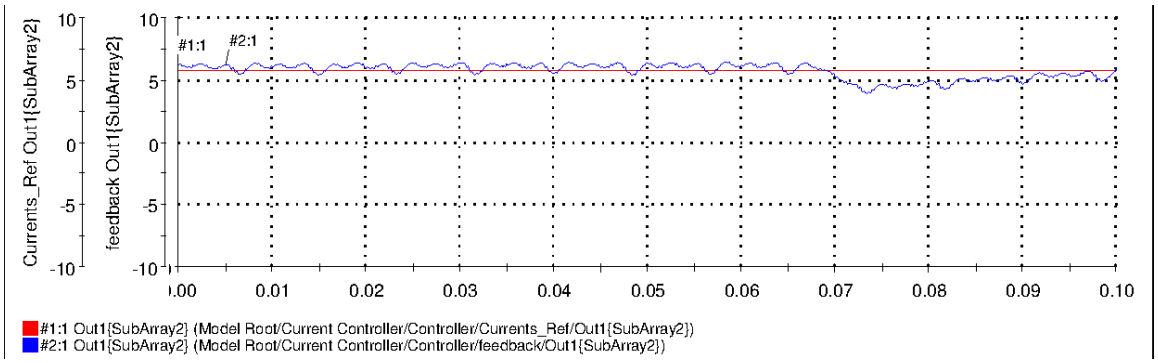

Figure 5.60 I_q and I_{qref}.

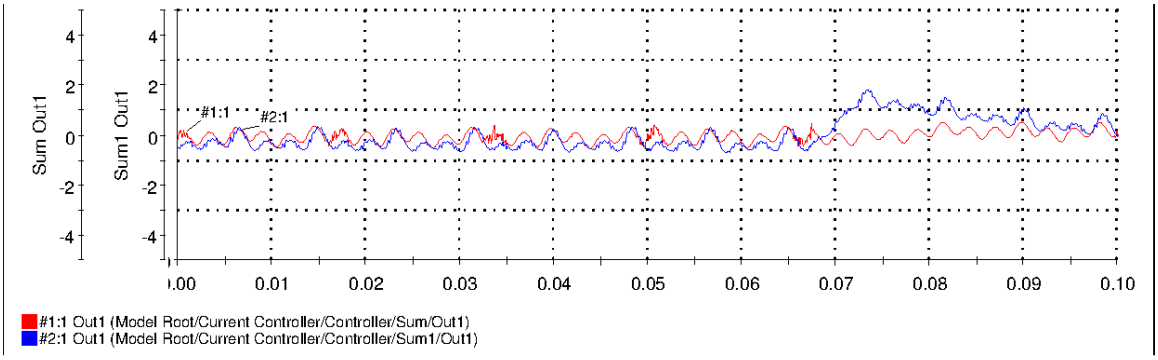

Figure 5.61 I_d and I_q error.

5.3.3 Pure Reactive Power Injection to the Grid

Figure 5.62 represents the Power Quality Analyzer when there is the command to provide pure reactive power in amount 2000 Var to the grid. In this condition inverter operates with almost zero power factor, can be seen on Figure 5.62 (b).

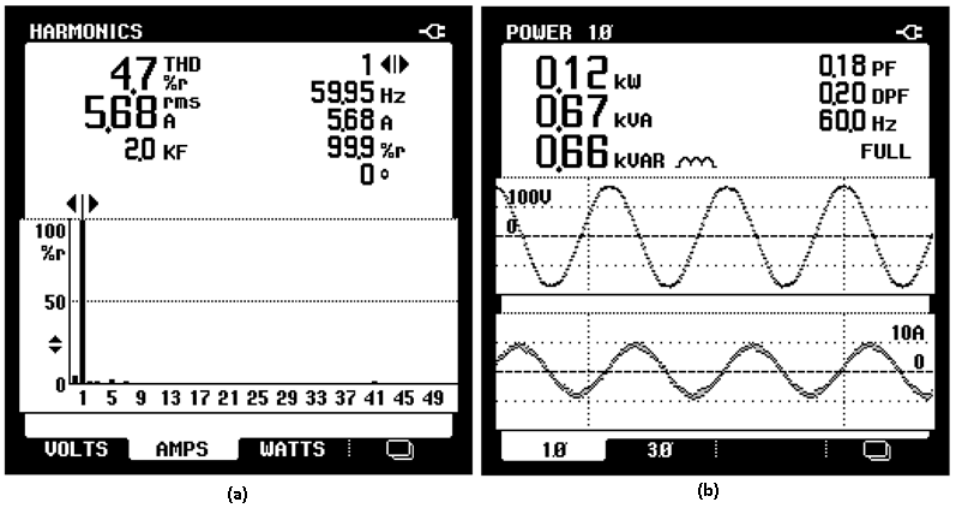

Figure 5.62 Power quality analyzer data: (a)THD of current injected to the grid (b) phase A voltage, current waveforms and single phase power.

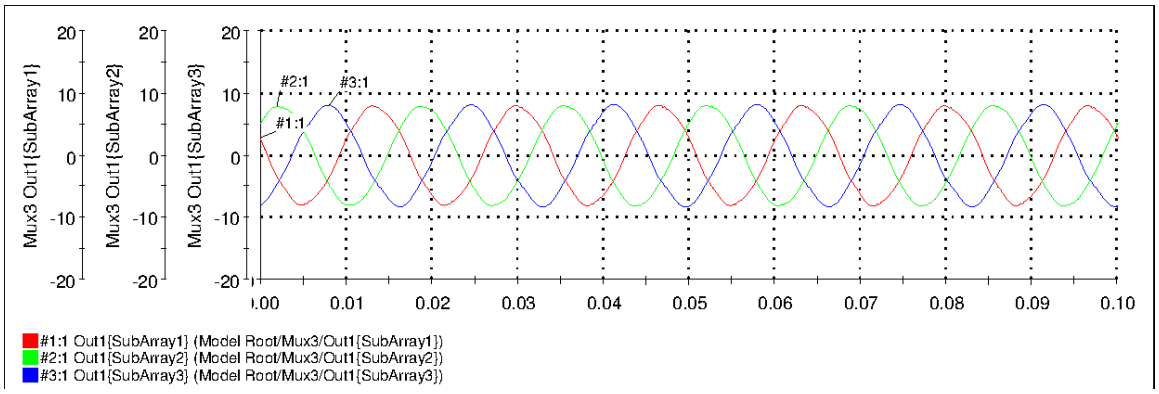

Figure 5.63 Line currents injected to the grid.

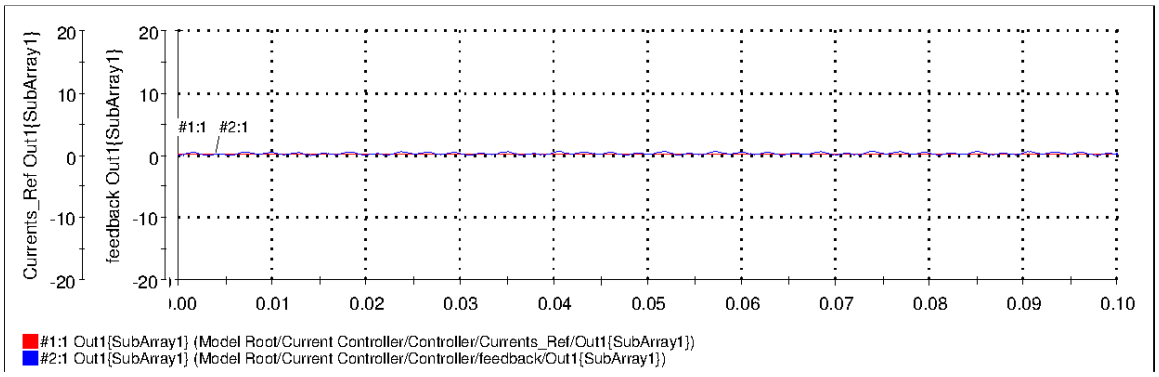

Figure 5.64 I_d and I_{dref}.

It can be seen from Figure 5.64 I_d and I_{dref}Figure 5.64 that current I_d responsible for active power, successfully follows 0 reference.

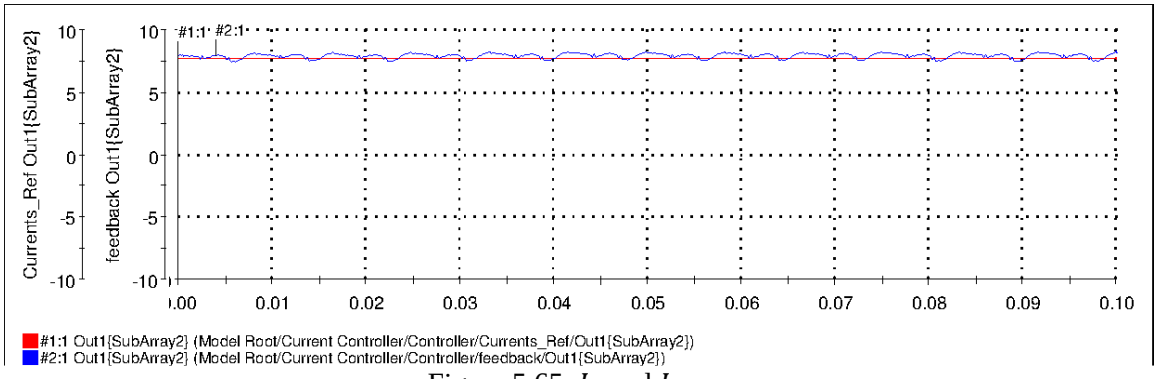

Figure 5.65 I_q and I_{qref}.

Current I_q, responsible for reactive shown on Figure 5.65. It can be seen from Figure 5.64 I_d and I_{dref}Figure 5.64 that current I_d responsible for active power, successfully follows 0 reference.

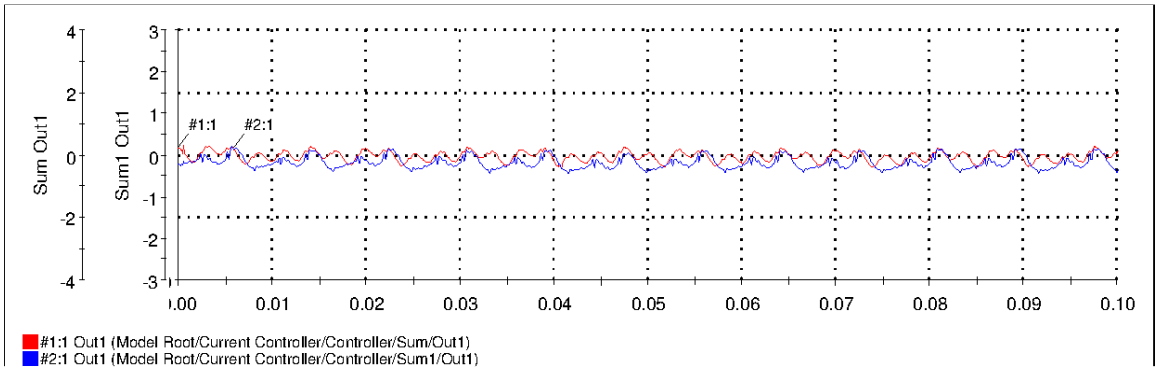

Figure 5.66 I_d and I_q error.

5.3.4 Reactive Power Consumption from the Grid

Figure 5.67 represents the Power Quality Analyzer when there is the command to consume pure reactive power (zero active power) in amount of 2000 Var from the grid. In this regime inverter operates with almost zero power factor, can be seen on Figure 5.67(b).

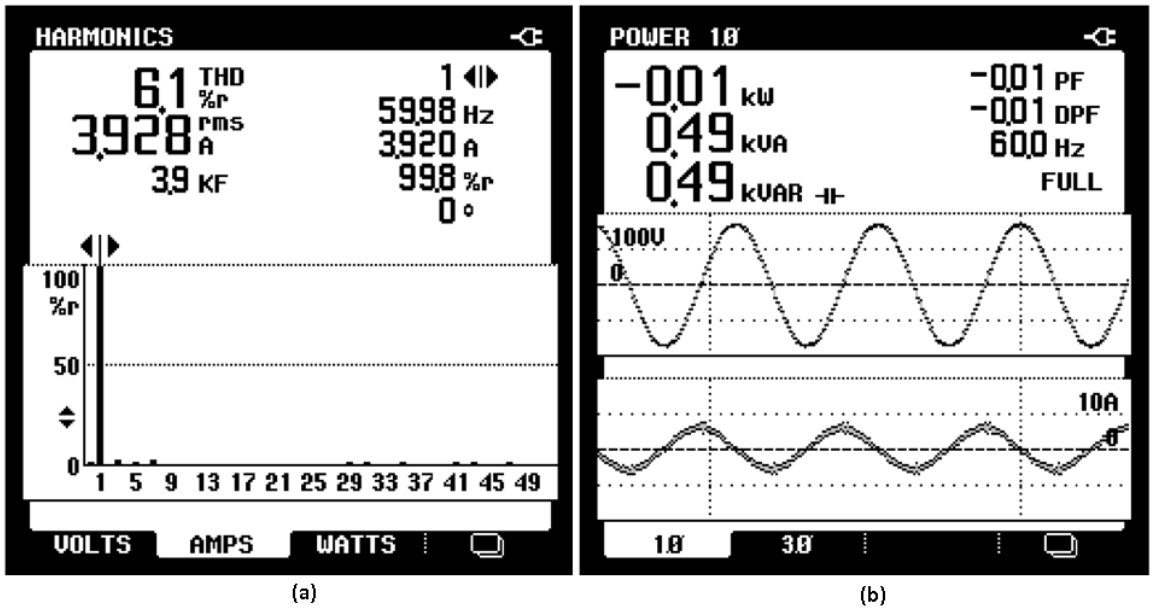

Figure 5.67 Power quality analyzer data: (a)THD of current injected to the grid (b) phase A voltage, current waveforms and single phase power.

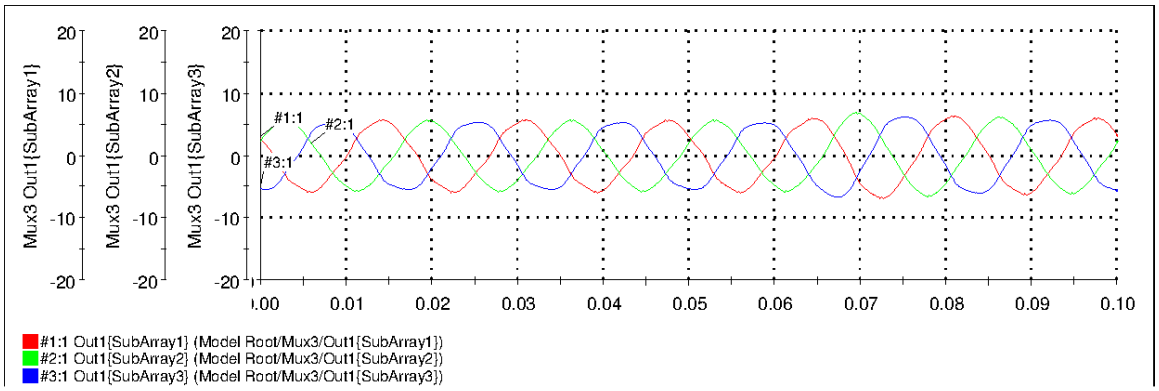

Figure 5.68 Line currents injected to the grid.

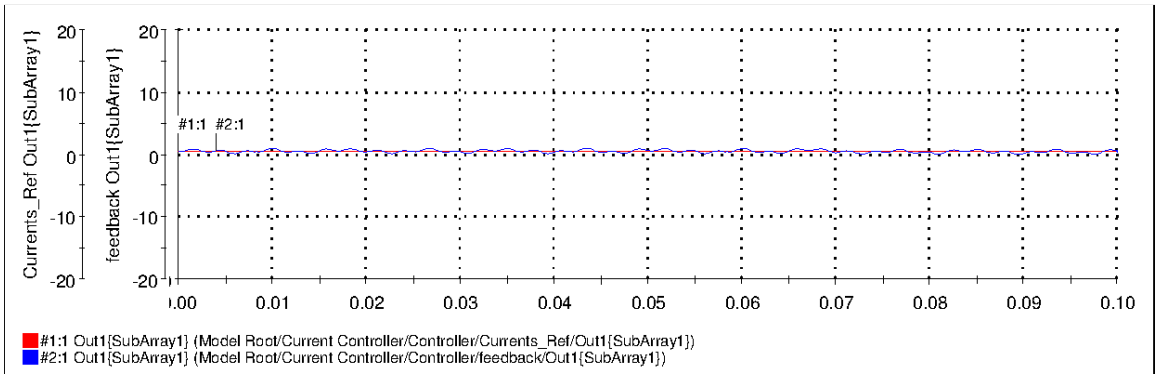

Figure 5.69 I_d and I_{dref}.

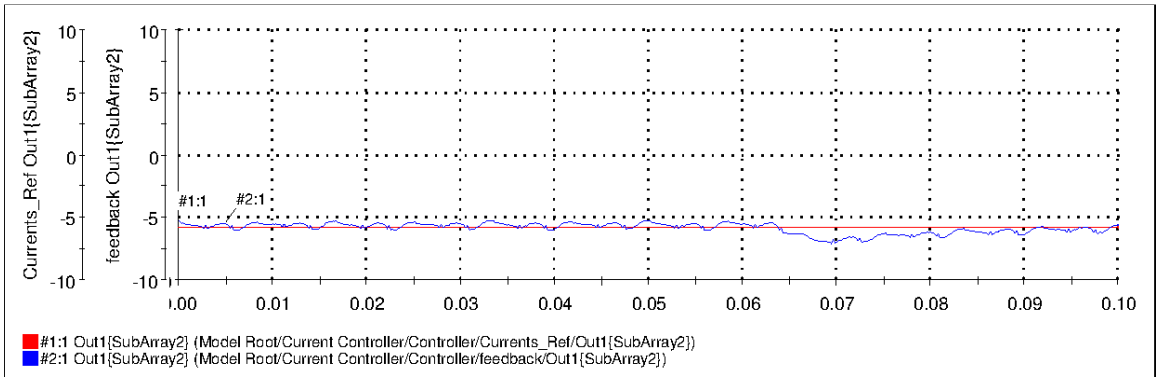

Figure 5.70 I_q and I_{qref}.

5.3.5 Reference Power Step Change Response

Two test were performed to show how the inverter operates during the step change in reference command. As it can be seen from Figure 5.72 - Figure 5.76 step change from 3000 W to 1500 W occurs at time 0 s.

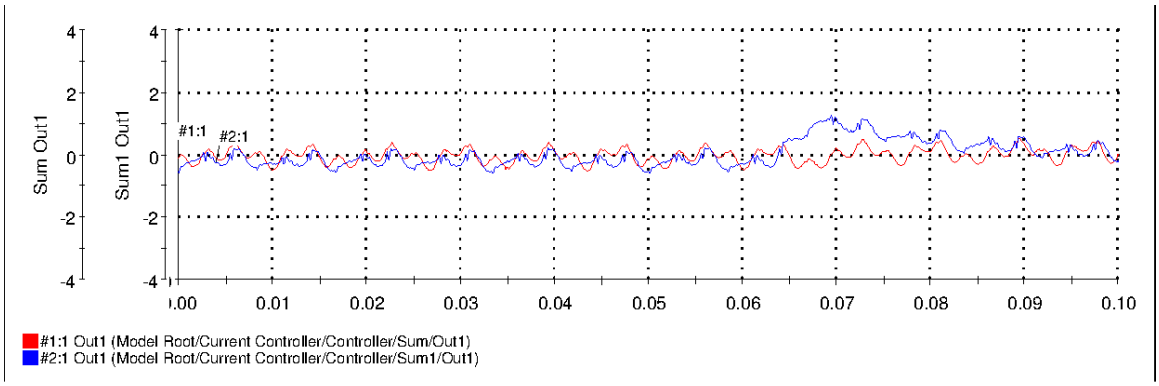

Figure 5.71 I_d and I_q error.

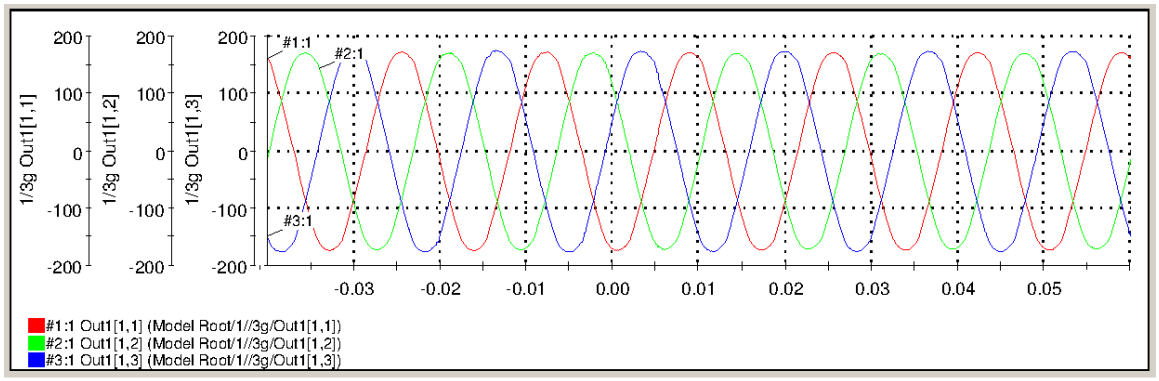

Figure 5.72 Phase voltages measured at load terminals.

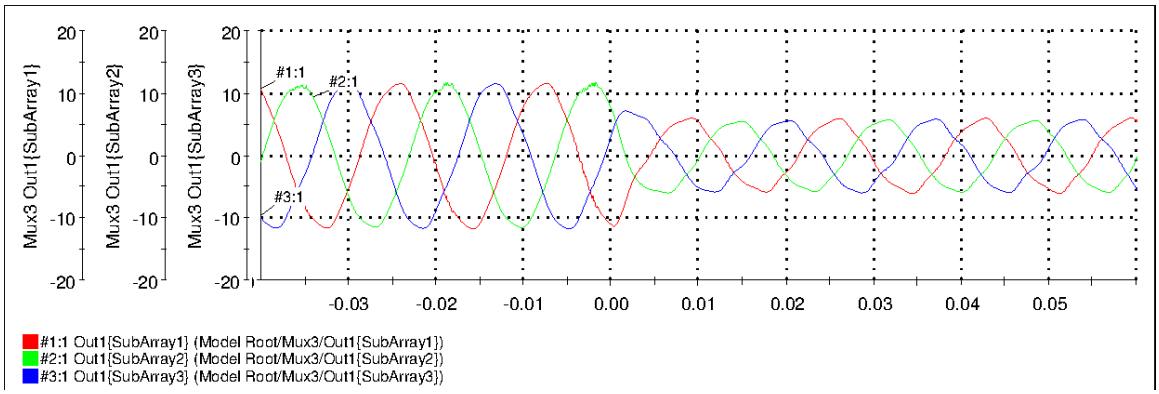

Figure 5.73 Line currents injected to the grid.

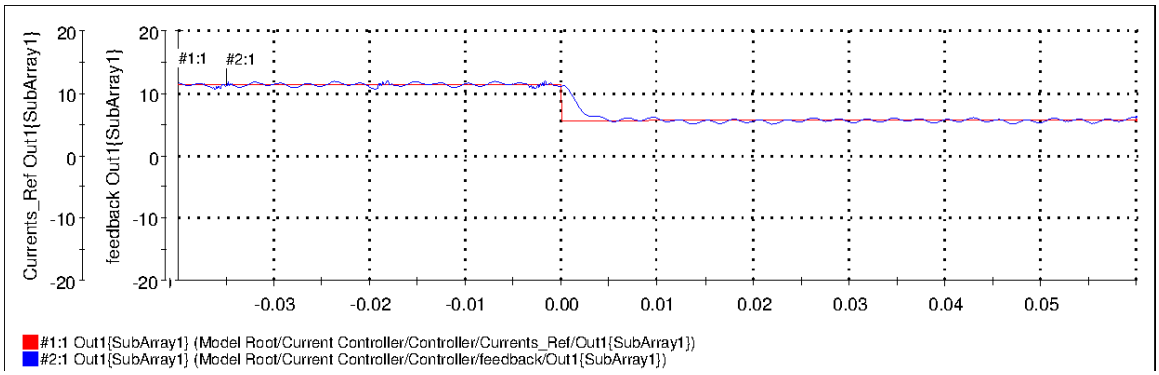

Figure 5.74 I_d and I_{dref}.

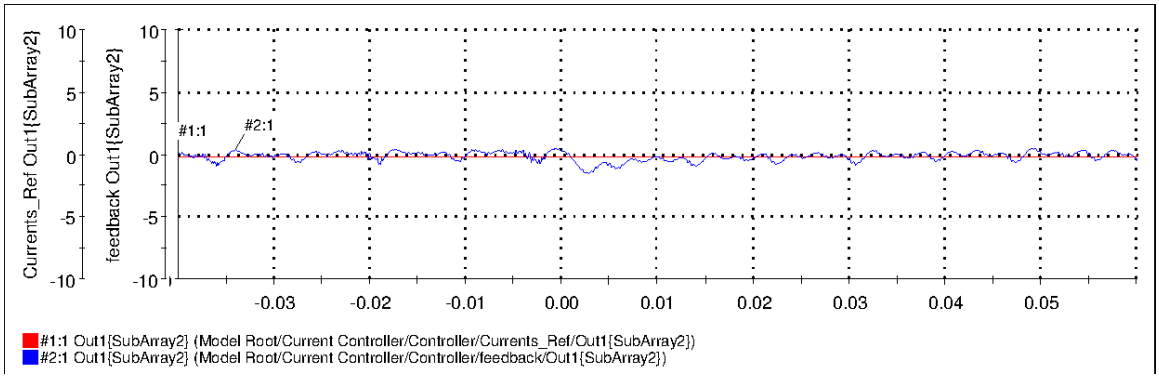

Figure 5.75 I_q and I_{qref}.

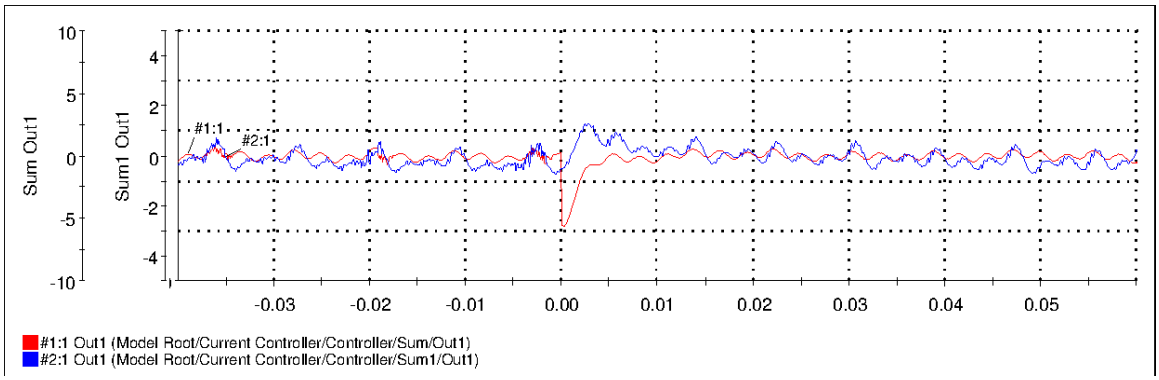

Figure 5.76 I_d and I_q error.

Figure 5.77 - Figure 5.81 show system operation when there is step change from 1500 W to 3000 W, which occurs at time 0 s.

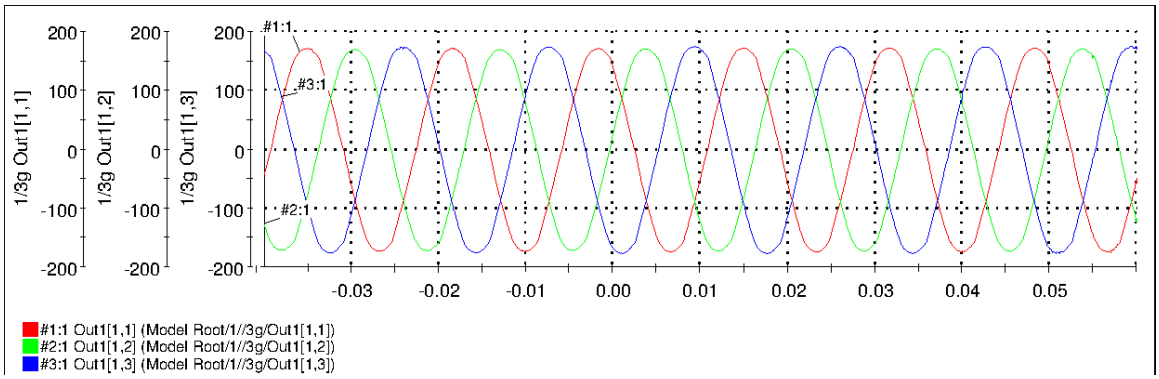

Figure 5.77 Phase voltages measured at load terminals.

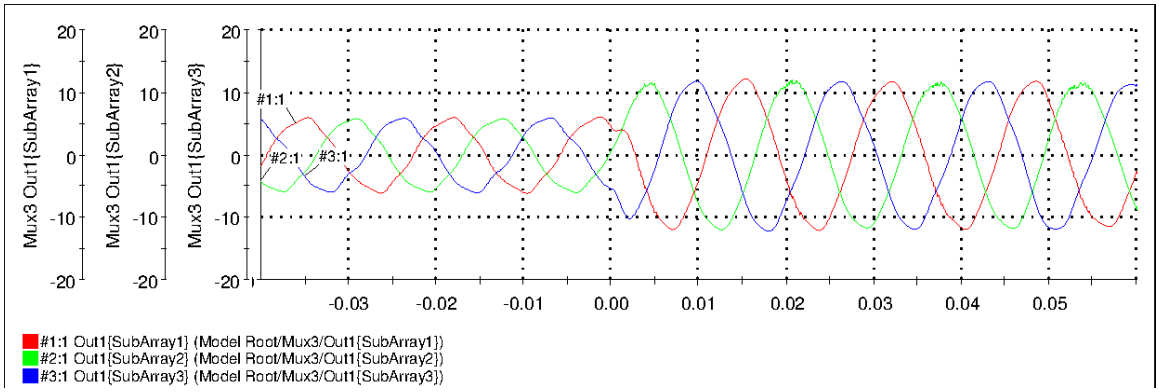

Figure 5.78 Line currents injected to the grid.

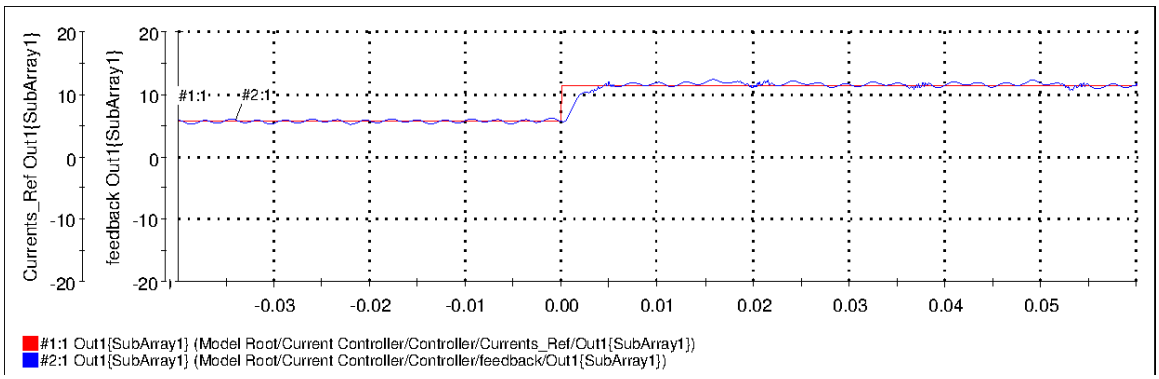

Figure 5.79 I_d and I_{dref}.

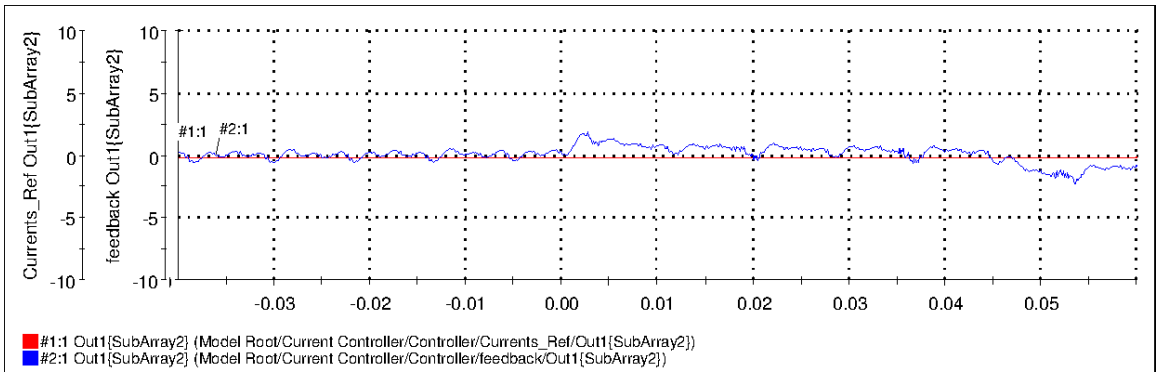

Figure 5.80 I_q and I_{qref}.

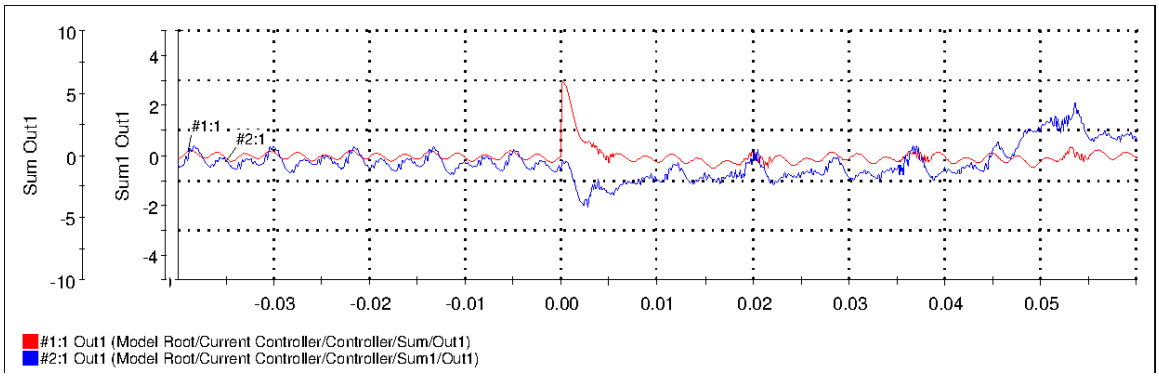

Figure 5.81 I_d and I_q error.

5.3.6 Bidirectional Power Flow the Grid to the DC-link

During this experiment inverter provides 1.5 kW to the grid after some time there is a command and inverter consumes around 1 kW power from the grid and provides it to the load connected at DC link. Steady state operation can be observed on Figure 5.82.

Step change in power command can be observed at time 0.0s (Figure 5.83 through Figure 5.86). After time 0.0s. inverter output current switches its polarity and flows the grid to DC link (negative PF at Figure 5.82)

5.4 Evaluation of Results

This chapter presents two different modes of designed prototype operation, when it works in stand-alone mode and providing nominal voltage and nominal frequency to the load and grid connected

mode, when it operates synchronously with grid and provides or consumes active and reactive power to the grid.

Voltage controller for stand-alone mode operates normally when the load is linear and balanced, however during operation with nonlinear load (three phase diode rectifier with DC load) inverter provided distorted voltage output with high content of 5^{th} and 7^{th} harmonic.

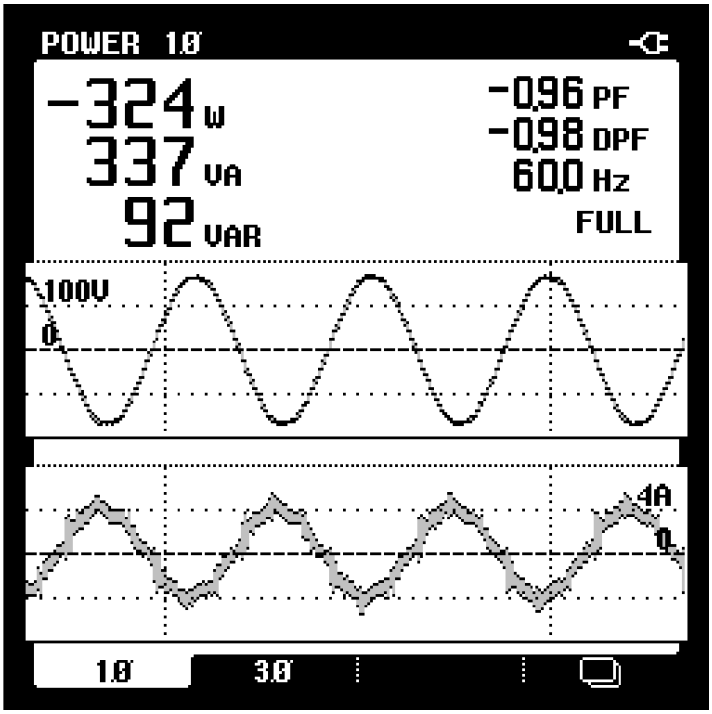

Figure 5.82 Power quality analyzer data: steady state operation.

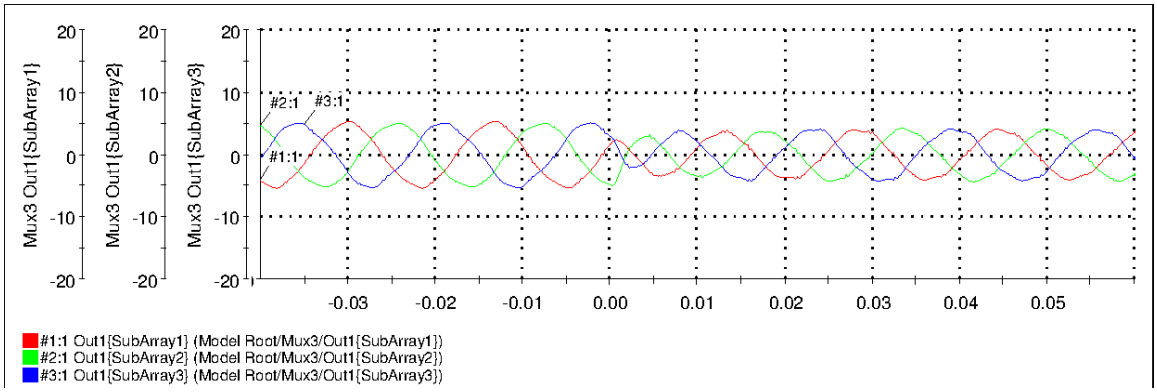

Figure 5.83 Line currents injected to the grid.

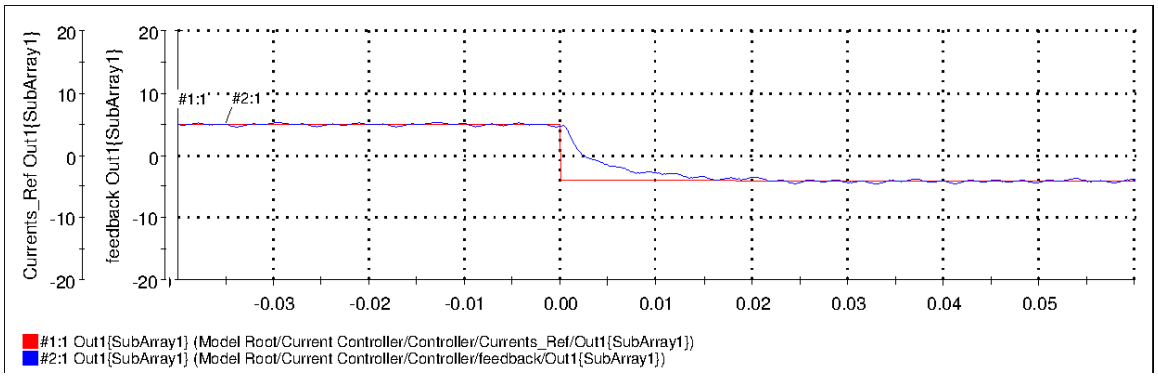

Figure 5.84 I_d and I_{dref}.

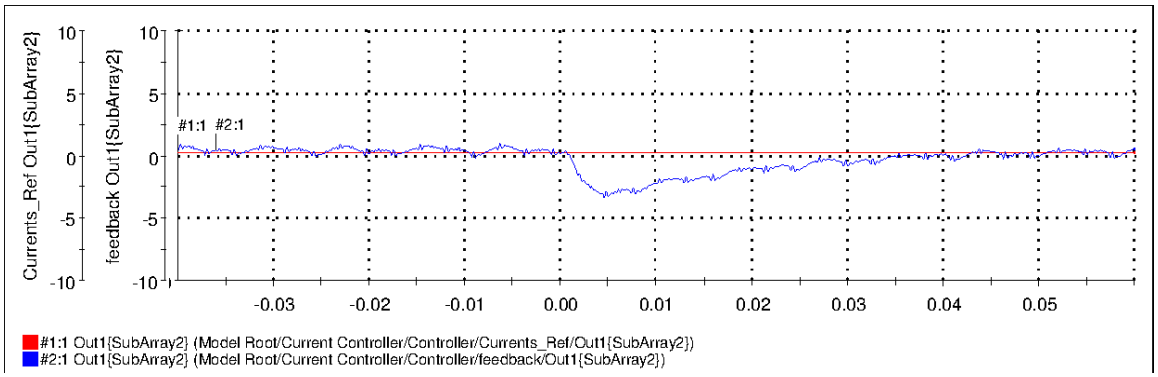

Figure 5.85 I_q and I_{qref}.

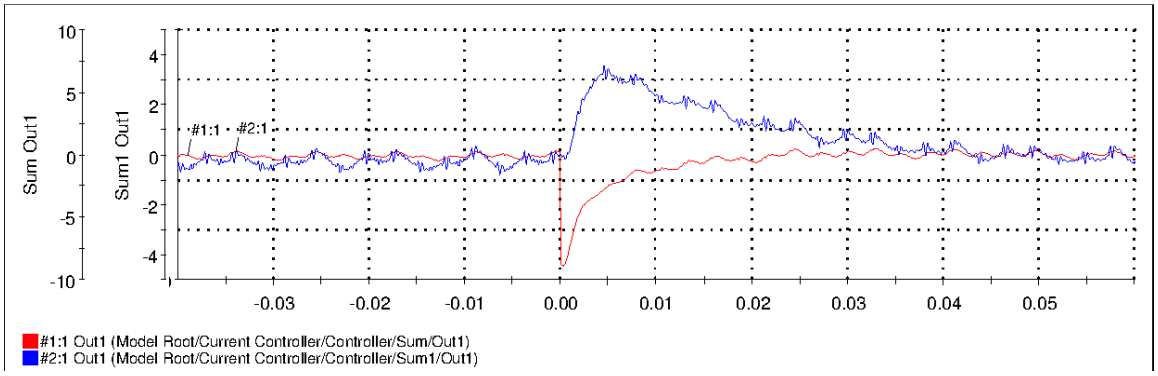

Figure 5.86 I_d and I_q error.

To improve the stand alone control system there is need in additional inner current control loop. Control system with this additional control loop will be able to provide pure sinusoidal voltage.

The inverter successfully operates in grid-connected mode. However, there are some problems related to the intrinsic distorted and imbalanced three-phase voltage available in the building where the

laboratory is located (Brown Building). The inverter can only provide sinusoidal current (with THD less than 5%) when the reference power is higher than 2000W. With the increase of injected power, THD of current getting better. Same is valid for pure reactive power injection, inverter provides reactive current with THD less than 5% only after 2000 Var reference. Maximum injected power to the grid was 3000 W and 1200 Var (line current is around 9.3A RMS), which is the limit of DC link voltage of inverter and DC Power Supply voltage/current limit. During the simple analysis of grid conditions, current consumed by LCL filter from the grid were investigated, which affects the THD measurements done by Power Quality Analyzer. Since the current probe measures resultant current on inverter output, then the analyzed current is sum of LCL filter consumed current and current generated by inverter.

As it was mentioned before, unbalanced and distorted grid has big impact on inverter performance. For this purpose positive sequence detector was developed and implemented, however even this effort is not enough and better decoupling of inverter with the grid is required, which can be achieved with more sophisticated control system and a more powerful hardware-in-the-loop (HIL) prototyping system.

Regarding islanding detection, decision was made not to perform this experiment, since switching from one state to another might cause high inrush currents and inverter works synchronously with the building three phase grid, but for this test will be safer to have independent three phase system. Also another problem with islanding detection was discovered during the experimental work, which also limited ability to test IEEE 1547. The frequency output of PLL system was giving fluctuations which are already outside the boundaries defined by IEEE 1547.

Next chapter will discuss on all the work done for the system implementation and will propose some ideas and suggestions for future work in order to improve the current system.

CHAPTER 6
CONCLUSION AND FUTURE WORK

6.1 Conclusion

This thesis presents complete design and implementation of an experimental prototype of three phase grid connected inverter. The objectives for this Ms thesis have been successfully realized through analysis, simulation and experimental investigations. As a part of this research activity a 5 kW prototype of three-phase grid connected inverter has been built and tested with all necessary interface circuits. Also, a three-phase grid connected inverter simulation model has been analyzed in Matlab/Simulink which was used to design the prototype and to develop proposed control solutions. The completion of three-phase grid connected inverter and effectiveness of the proposed techniques has been proved through numerous simulation and experimental results, even though there are some limitations in hardware setup. During the experimental work some disadvantages of proposed control system were discovered, possible suggestions for improvements will be given in next section.

6.2 Future work

Future extension of the project will need better and sophisticated real-time hardware from dSPACE or Opal RT producers. The dSPACE 1104, used for this experimental work, has only 8 analog input and output channels and will be definitely not enough for that, also power of processor is very limited. Each designed control system (for stand alone mode and grid connected mode) needs at least 60 μs to run successfully, however with additional control system of DC link voltage and MPPT it will be impossible to run the model at required speed.

Future work of the present project includes:

- High efficiency interleaved boost DC/DC converter and it's control system design;
- Maximum power point tracking algorithm implementation for solar panels;
- IEEE 1547 islanding detection experiment;
- Model discretization will provide smaller run time for the proposed model;
- Design and implementation of other control strategies for the grid side converter in order to do a comparison between methods of control;
- Advanced relay protection of inverter, which will be done in hardware and independently from computer with control system;
- Evaluation of virtual resonance damping technique in LCL filter for real implementation;

- Grid connected control system optimization with weak grid operation(independent operation of inverter from grid conditions);
- Incorporating a storage system in order to provide power for critical load under black out and no sun condition;
- Implementing an energy-management system to minimized the operation cost and enhance the system stability;
- Grid fault ride through;
- Real time communication implementation between control system and utility grid;
- An advanced voltage control system with nested current loop for stand-alone operation.

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APPENDIX A

MATHEMATICAL TRANSFORMATION

Stationary Reference Frame αβ [58]

Transformations from a three-phase (Equation A-1) system to different two-phase systems can be used in order to avoid controlling coupled ac currents and voltages. These are based on the fact that in a balanced three-phase system there are only two independent current/voltages, thus the third current/voltage can be expressed by the other two. These systems are often referred to as reference frames, where the frame is the axis system of the transformed system.

When a three-phase system is transformed into a two-phase system, this is often called a abc to αβ (or αβ0 when the zero vector is used) transform, or a transform into the stationary reference frame. Both the three phase and the two phase system is said to be stationary, because the axes is locked in one position, but the term stationary reference frame usually refers to a two phase stationary reference frame.

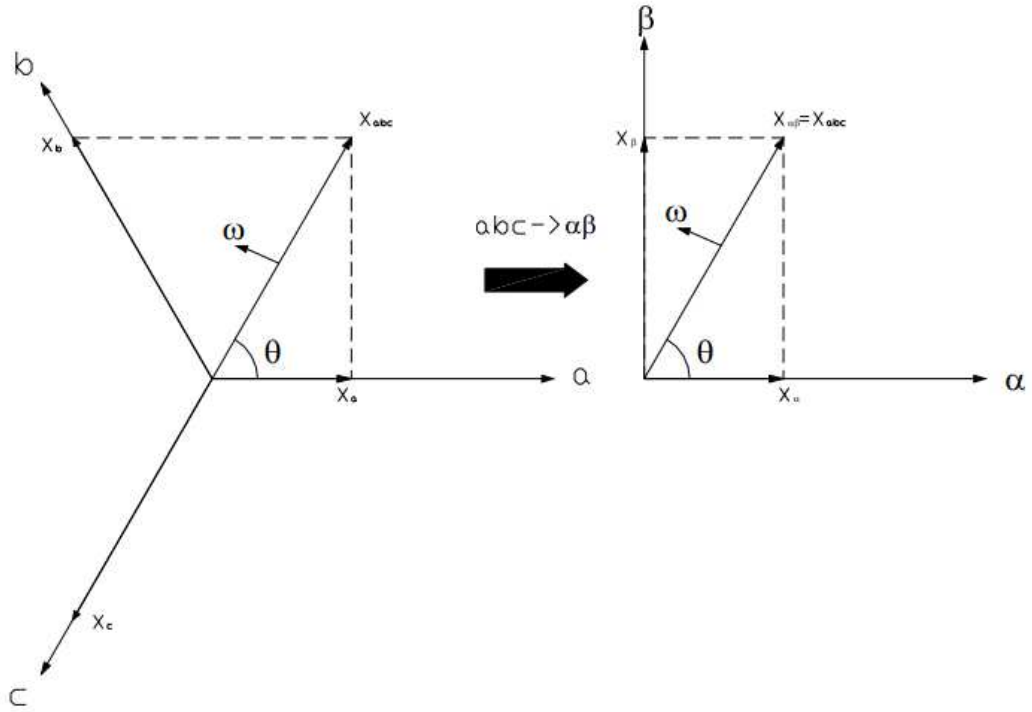

Figure A-1 $abc\ to\ \alpha\beta$ transformation.

The transformation is made by applying the Clarke transformation in Equation A-2, where the three phase quantities must be phase values, i.e. not line values. By inverting the coefficient matrix, the three-phase quantities can be found as a function of the two phase quantities.

$$X_a = X_{abc} sin\,(\theta)$$
$$X_b = X_{abc} sin\,(\theta - \frac{2\pi}{3}) \quad \text{(A-1)}$$
$$X_c = X_{abc} sin\,(\theta + \frac{2\pi}{3})$$

$$\begin{bmatrix} X_\alpha \\ X_\beta \\ X_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \quad \text{(A-2)}$$

Carrying out the matrix multiplication in Equation A-2 yields to Equation A-3

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} V_{abc} sin\,(\theta) \\ -V_{abc} cos\,(\theta) \end{bmatrix} \quad \text{(A-3)}$$

The transformation can be thought of as a change of coordinate system, from a three axis(phase) system to a two axis (phase) system as shown in Figure A-1. It can be seen from the abc system that the only two phases is needed to express the vector X_{abc}, and thus it can be expressed in the αβ system as the vector $X_{\alpha\beta}$ without any loss of information. If X is the grid voltage, then ω represents the grid frequency, and θ is the instantaneous phase angle .

Synchronous Rotating Frame dq [18]

In this system the axis is no longer locked, and rotates following an arbitrary vector, hence the term "synchronous reference frame". It is sometimes also termed the dq system (or dq0 if zero-vector is used). This transformation is widely used in motor drives, where the axis system follows for instance the rotor position or rotor flux. In grid connected inverter it is most common to lock the axis system voltage or current (usually the grid voltage). In the Figure A-2 the d-axis is locked to the vector $X_{\alpha\beta}$, and therefore $X_d = X_{\alpha\beta}$ and $X_q = 0$. The axis system will the rotate with an angular speed ω, and have an instantaneous angle of θ (referred to the stationary system).

The transformation is made using the Park transformation shown in Equation A-4, where the stationary quantities can be found as a function of the synchronous quantities by inverting the coefficient matrix.

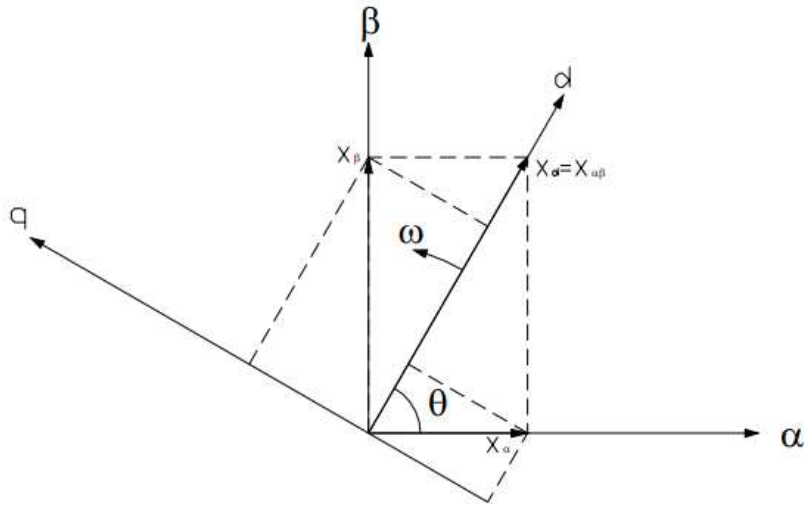

Figure A-2 $\alpha\beta$ *to* dq transformation.

$$\begin{bmatrix} X_d \\ X_q \\ X_0 \end{bmatrix} = \begin{bmatrix} cos\,(\theta) & sin\,(\theta) & 0 \\ -sin\,(\theta) & cos\,(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} X_\alpha \\ X_\beta \\ X_0 \end{bmatrix} \quad \text{(A-4)}$$

Where θ is instantaneous phase angle. If the dq-axis system is locked to the grid voltage, the axes will rotate with the frequency $2\pi f_g$, and the dq values will become DC-values.

These equations assume that both the voltage and the current is transformed into the dq system using the same reference frame. When the reference frame is oriented at the voltage vector, then the d-axis current will represent current in phase with the voltage, and thus it represents the active power in the circuit. The q-axis current will then represent current which is out of phase with the voltage, and thus it represents the reactive power in the circuit. It should be noted that other versions of the Park transformation exist, and in these the orientation of the dq-axis on the $X_{\alpha\beta}$ vector might differ. This can for instance lead to having the active power controlled by the q-axis.

APPENDIX B

LCL FILTER WIRE LENGTH CALCULATION

Inductor L_1 - inverter side

Core:77102-A7

Quantity per phase: 5 (in stack)

ID=57.2 mm (inside diameter)

OD=102.9 mm (outside diameter)

Ht=17.7 mm (height)

Winding Factor = 0.177 (round to 20%)

Number of Turns: 116

Wire: AWG 12

Data from catalog:

For Winding Factor =20%

$\frac{\text{Length}}{\text{Turn}}$ =96.8 mm

$L_{turn} = 96.8 + 2(5-1) * 17.7 = 238.4$ mm (turn length)

$L_{total} = 238.4 * 116 + 300(terminals) = 28$ m

Inductor L_2- grid side

Core:77258-A7

Quantity per phase: 1

ID=24.1 mm (inside diameter)

OD=40.77mm (outside diameter)

Ht=15.37 mm (height)

Winding Factor = 0.36 (say 40%)

Number of Turns: 43

Wire: AWG 12

Data from Catalog:

For winding factor =40%

$\frac{Length}{Turn}$=54 mm

$L_{total} = 43 * 54 + 300(terminals) = 2.622$ m

APPENDIX C

SEMIKRON INVERTER CONTROL BOARD PINOUT

Table C-1 Interface Connector Pin Assignment Driver D-sub 25 pin.

D-sub 25 pin	Signal	Remark
1	BOT HB 1 IN	positive 5V - 15V CMOS logic
14	ERROR OUT	fault monitoring. LOW = NO ERROR, open collector output, external pull up resistor required. Max 30V/15mA
2	TOP HB 1 IN	positive 5V - 15V CMOS logic
15	BOT HB 2 IN	positive 5V - 15V CMOS logic
3	ERROR OUT	fault monitoring. LOW = NO ERROR, open collector output, external pull up resistor required. Max 30V/15mA
16	TOP HB 2 IN	positive 5V - 15V CMOS logic
4	BOT HB 3 IN	positive 5V - 15V CMOS logic - sec Table 4
17	ERROR OUT	fault monitoring. LOW = NO ERROR, open collector output, external pull up resistor required. Max 30V/15mA
5	TOP HB 3 IN	positive 5V - 15V CMOS logic
18	Over temp OUT	over temperature monitoring. LOW = NO ERROR open collector output, external pull up resistor required. Max 30V/ 15mA
6	GND	may be used for analog signal reference
19	Voc analog OUT	analog voltage proportional to the DC link voltage, for scaling, max output current 5mA
7	PWR	24V IN (8V- 30V)
20	PWR	
8	+ 15 VDC OUT	15 V OUT +/- 4% at 60mA
21	+ 15 VDC OUT	
9	GND	GND for power supply and digital signals
22	GND	
10	Temp analog OUT	analog voltage proportional to the DBC temperature, max output current 5mA
23	REF 1	Reference for Phase 1 current. GND
11	1 analog OUT HB 1	analog voltage proportional to Phase 1 current. sec Table 6 for scaling, max output current 5mA
24	REF 2	Reference for Phase 2 current. GND
12	1 analog OLT HB 2	analog voltage proportional to Phase 2 current. see Table 6 for scaling, max output current 5mA
25	REF 3	Reference for Phase 3 current. GND
13	1 analog OUT HB 3	Analog voltage proportional to Phase 3 current, max output current 5mA

APPENDIX D

SPWM REALIZATION IN dSPACE

The sinusoidal PWM dSPACE block "DS1104SL_DSP_PWM1" shown on Figure C-1.

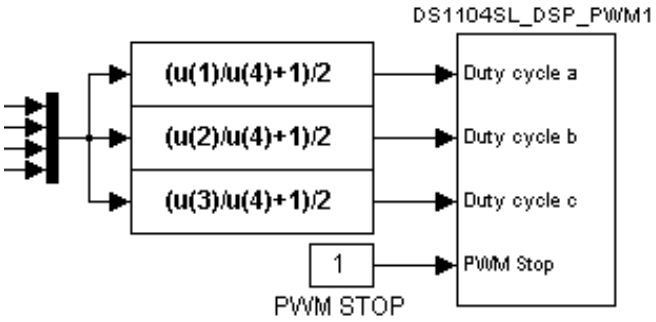

Figure D- 1 dSPACE SPWM block.

This is a sinusoidal symmetric PWM. PWM stop allows to enable (PWM stop=0) or disable (PWM stop=1) the PWM block. The signal needs double type.

The input range for "duty cycle abc" is [0;+1]. However dSPACE used a little bit different approach for sinusoidal PWM realization. This block requires input of duty cycle but not modulation wave form. Here only final formulas (Equation C-1) for three phase duty cycle calculation are presented. Derivation can be found in [59] and [60].

$$\begin{aligned} \text{Duty cycle a} &= \left(\frac{2\mathrm{v_A}}{\mathrm{V_{DC}}}+1\right)\frac{1}{2} \\ \text{Duty cycle } b &= \left(\frac{2\mathrm{v_B}}{\mathrm{V_{DC}}}+1\right)\frac{1}{2} \\ Dutycyclec &= \left(\frac{2v_C}{V_{DC}}+1\right)\frac{1}{2} \end{aligned} \qquad \text{(C-1)}$$

where V_{DC} is DC link voltage, $v_A,\ v_B,\ v_C$ are the modulation signals, values are in Volts.