PROCESS DEVELOPMENT OF NANOIMPRINT LITHOGRAPHY FOR SELECTIVE AREA GROWTH OF III-V MATERIALS ON SILICON

by

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ABSTRACT

Heteroepitaxy of III-V semiconductors on Si substrates is inherently challenging due to the mismatch of various material properties that lead to the formation of dislocations and defects which plague device efficiencies. In an effort to pave a cost-competitive pathway to integrate high quality III-V materials on Si, I report here how an inexpensive nanoimprint lithography (NIL) process was developed to enable nanoscale selective-area growth (SAG) of III-V materials on Si by metalorganic chemical vapor deposition. Nanoscale vias in silica (SiO_x) with aspect ratios (height:width) > 1 on Si substrates are expected to enable aspect ratio trapping (ART) of extended defects and reduce dislocation densities resulting from heteroepitaxial growth of lattice mismatched III-V materials. The substrate conformal NIL process that I have developed using bi-layer polydimethylsiloxane (PDMS) stamps was successfully employed to pattern polished (001) Si substrates on the nanoscale with an SiO_x sol-gel imprint resist and enable SAG of thin film GaAs. The film qualities and dislocation densities resulting from SAG of GaAs on NIL-patterned Si substrates were investigated using scanning electron microscopy, transmission electron microscopy, and x-ray diffraction analysis and compared to heteroepitaxial growth of GaAs on planar (001) Si substrates. Our results show that NIL-patterned SiO_x templates can enable selective-area epitaxial growth of single crystal GaAs on Si; however, the template geometries used for SAG thus far have not effectively reduced dislocation densities by ART compared to heteroepitaxial growth of GaAs on planar Si. We conclude that further optimization of SAG is possible at low cost using the NIL technique, but will require further process development and an expanded variety of Si master pattern geometries containing decreased feature sizes (below 100 nm) and increased aspect ratios (above 1.4).

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CHAPTER 1

INTRODUCTION & MOTIVATION

Since 1858, the American Association for the Advancement of Science has been aware of published findings regarding the global warming effects that a carbon dioxide (CO_2) rich atmosphere can cause [1]. It is no coincidence that in parallel with record breaking global surface temperatures, the CO_2 concentrations that are present in our atmosphere have never been so high in hundreds of thousands of years, as shown below in Figure 1-1 [2]–[4]**.** After decades of rigorous research, in 2014 a world-wide scientific consensus was reached declaring a greater than 95% certainty that the historically catastrophic climate changes we are currently observing are a consequence of human activity and the unprecedented levels of CO_2 and greenhouse gasses we produce [5], [6].

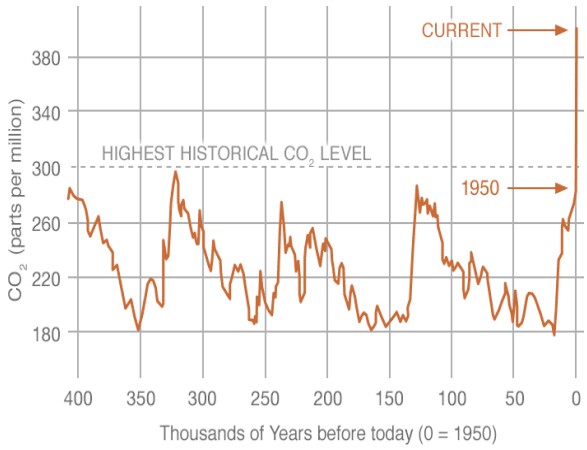

Figure 1-1 Timeline of CO_2 levels indicate a rapid increase in the last 50 years [4]

Knowing the largest source of the US's CO_2 emissions are from the electricity sector [7], the US Department of Energy (DOE) has been working aggressively to decrease CO_2 emissions via research programs like the SunShot Initiative in order to advance solar energy technology as a low-cost electricity source for all Americans [8]. The maturity of the silicon (Si) processing

industry has paved the path for crystalline Si-based cells to be among the most competitive in terms of balancing both cost and efficiency [9]. Although gallium arsenide (GaAs) based solar cells are the most efficient, integrating this material with Si requires further innovative research and development to drive down the cost such that this technology can be made an affordable resource to power not only international space stations, but also US homes and businesses [10].

1.1 Integration of III-V Semiconductors on Si

Combining the impressive electronic and photonic properties of III-V semiconductor materials with the low-cost and high-volume appeal of Si substrates has been extensively explored over decades for applications in microprocessing, optoelectronics, and nanophotonics [11]–[14]. In addition, the integration of wide bandgap III-V materials such as GaAs or $In_{0.5}Ga_{0.5}P$ on Si substrates is a promising path to building high efficiency photovoltaic (PV) devices [15]. However, heteroepitaxial growth of high quality III-V materials on Si is still inherently challenging due to the mismatch of various material properties such as lattice constants, crystal symmetry, and thermal expansion [16].

A problem encountered during heteroepitaxial growth of lattice mismatched polar material on non-polar substrates, such as GaAs on (001) Si, is the formation of planar defects such as stacking faults, twinning, and antiphase domains (APDs). In addition, a high density of misfit and threading dislocations can plague device efficiencies [17]. Growth techniques such as molecular beam epitaxy and metal-organic vapor deposition have served as key tools in research efforts attempting to overcome these challenges and realize the commercial production of III-V-on-Si devices. To address these challenges, the work presented in this thesis explores the use of template-assisted heteroepitaxial growth on the nanoscale to support the integration of high

quality III-V materials on Si and drive down the cost of building high-efficiency tandem solar cell architectures.

1.1.1 Template Assisted Heteroepitaxy

After a critical thickness of growth of lattice mismatched materials, it becomes energetically favorable to relieve strain and allow for relaxation by the formation of misfit dislocations that glide to, or near, the mismatched interface. Accompanying misfit dislocations are threading dislocations, which can run through the thickness of the heteroepitaxial layer until they either terminate at an exterior surface, meet another threading dislocation to annihilate, or glide to the edge of a sample. Although compositionally-graded III-V metamorphic buffer layers, like $GaAs_yP_{1-y}$ help to reduce threading dislocation density for III-V/Si integration [18], they also increase the complexity and cost of building multijunction PV device architectures. Manufacturing cost analysis relevant to single- and dual-junction PV cells fabricated from III-V materials on Si identifies the thick, 3-5 micrometer (μm), metamorphic buffer layer as a major cost driver making this approach impractical for residential or utility-scale applications [19]. Therefore, before tandem PV device architectures can be considered economically viable for large-scale applications, further research and innovation are imperative to minimize buffer layer thickness and processing required for the successful integration of high-quality III-V materials on Si [20].

As an alternative, template assisted selective area growth (SAG) on the micron scale of GaAs on Si has been shown to reduce defect densities from $1x10^8$ cm^{-2} to $1x10^6$ cm^{-2} by decreasing the width of the nucleation area from over 100 μm to 10 μm; in this case, the ultimate reduction in dislocation density was concluded to be due to stress relief provided by SAG [21]. Furthermore, numerical analysis by Yamaguchi et al. suggests that dislocation densities below

10^6 cm^{-2} are possible with optimization of SAG in decreased pattern widths below 10 µm, and can be further reduced when combined with thermal cycle annealing. In addition, it has been demonstrated that SAG on the nanoscale can also be used to reduce the thickness of growth required to relax lattice-mismatched III-V materials on exact (001) Si substrates [22]–[24].

A reduction in nucleation area towards the nanoscale has been recently shown to support the growth of high quality III-Vs on Si by aspect ratio trapping (ART) of stacking faults and threading dislocations that originate near the mismatched interface and travel along the densely packed {111} family of planes [23], [24]. By reducing the nucleation area in selective area growth to the nanoscale and increasing the height of the walls of the template, as shown in Figure 1-2, any defects that originate near the interface and travel along the {111} family of planes can terminate at the walls of the template. The {111} family of planes are 54.7 degrees from the (001) plane, therefore a specific aspect ratio (height divided by width of the opening provided for epitaxial growth) of 1.4 or greater is necessary to significantly reduce defect densities in individual islands by ART. While reduced defect densities by ART has been demonstrated for heteroepitaxial growth of islands or nanowires, the result in the case of lateral

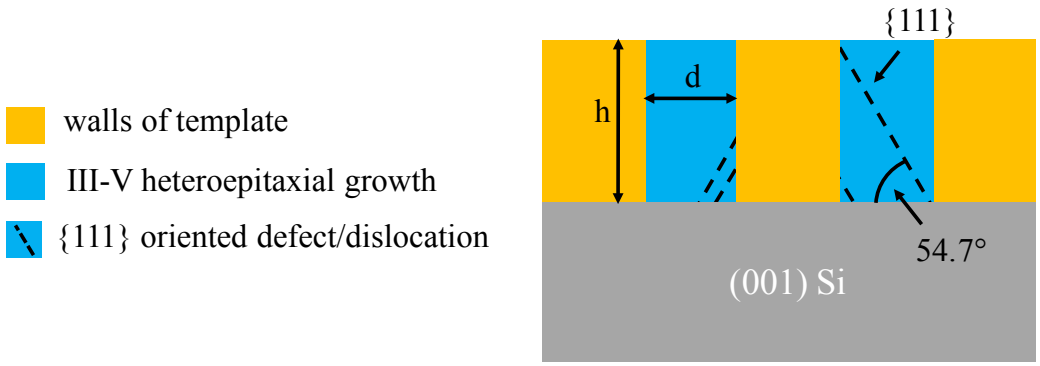

Figure 1-2 Schematic diagram illustrating how defects and dislocations that originate near the interface and travel along {111} planes can be terminated and trapped by aspect ratios (h:d) of 1.4 that are provided by the selected area growth (SAG) template

epitaxial overgrow is far less understood, considering the formation of threading dislocations may be necessary as islands merge during growth of a thin film.

Nanoscale selective area growth of III-Vs on Si has the potential to address key materials science challenges in tandem PV device architectures by eliminating the need for an expensive metamorphic buffer layer and reducing the III-V top cell thickness [25]. However, the nanoscale patterned templates with aspect ratios over 1.4 require high resolution patterning techniques such as electron-beam (e-beam) lithography which are exceedingly expensive with low throughput. Therefore, innovative solutions are required to reduce the cost of fabricating nanoscale templates before defect reduction by SAG and ART can be a viable and cost-competitive approach for III-V integration on Si and meeting the goals of the SunShot Initiative.

1.2 Nanoimprint Lithography

Imprint lithography is a relatively low-cost patterning technique that is capable of transferring macroscale to nanoscale patterns from one surface, called a stamp, to another by mechanical deformation of an imprint resist layer on a substrate. In 1996, nanoimprint lithography (NIL) made its debut with 25 nanometer (nm)-scale resolution using a rigid patterned surface (SiO_2) as a stamp for pattern transfer by thermal-compression molding of polymethylmethacrylate (PMMA) on Si substrates [26]. The generic thermal embossed NIL patterning method using rigid stamps (i.e. patterned Si and SiO_2 surfaces) has since evolved to include ultraviolet (UV) and soft-NIL using polydimethylsiloxane (PDMS) stamps to allow for conformal contact when imprinting into resist layers over large areas and irregular non-planar substrates [27]–[29]. In the last decade, extensive research efforts towards the process development and commercialization of substrate conformal NIL using PDMS stamps have

enabled great strides addressing the defect challenges that accompanied rigid stamp methods, such as substrate bow and particulate contaminants [30]–[32].

Substrate conformal NIL enables wafer-scale pattern transfer, complex over-lay designs, and 10 nm resolution, lending itself for applications in nanophotonics, optoelectronics, lasers, and solar [33]–[38]. A variety of thermal and UV curing polymer based imprint resists are commercially available, however such materials are not compatible with high temperature III-V growth environments and thus cannot be used to serve directly as a SAG template on Si [39]. Alternatively, a silicon oxide (silica) based sol-gel imprint resist can simplify the nanoscale template fabrication procedure as it enables imprinting at room temperature without the use of UV-light, and offers stability in high temperature and harsh chemical environments required for MOCVD of III-Vs on Si [36]. Traditional processing steps required to enable SAG on Si such as thermal oxide growth of SiO_2 and traditional lithographic patterning with nanoscale resolution can be eliminated by substrate conformal NIL using a silica (SiO_x) based sol-gel resist.

The substrate conformal NIL process (Figure 1-3), can be broken down into two parts, A. Stamp Fabrication, and B. Imprint Lithography. The general NIL process described here was developed using PDMS stamps and a SiO_x based sol-gel resist solutions that were fabricated and sythesized in-house, described in detail later in Chapter 2. To fabricate PDMS stamps for NIL, first the surface of a Si wafer, called the Si master, is patterned using traditional techniques such as e-beam lithography or deep ultraviolet (DUV) lithography to achieve nanoscale resolution features. Next, PDMS material is then allowed to conform to the patterned surface of the master and cure before being released, creating an inverse patterned PDMS replica of the Si master, referred to as a PDMS stamp. Once the PDMS stamp materials are cured and released, many

more stamps can be made from the same Si master to allow for high throughput of identically patterned substrates using the NIL process shown in Figure 1-3(B).

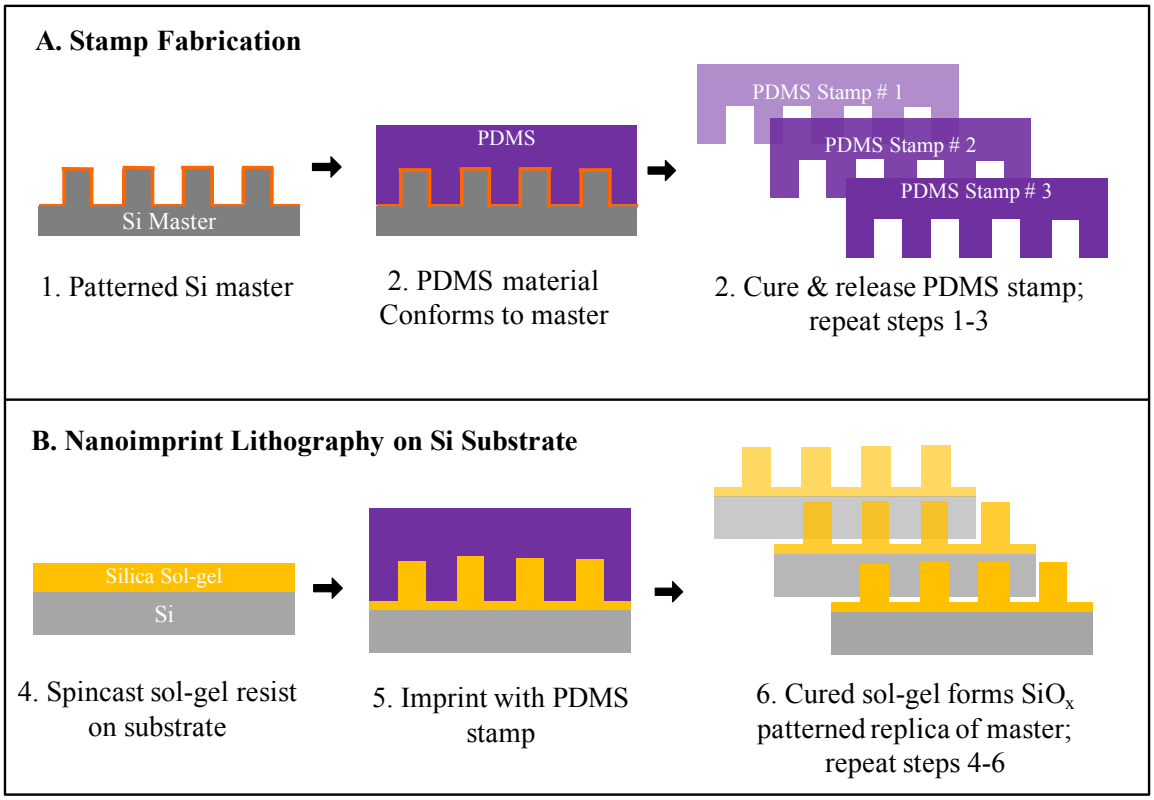

Figure 1-3 Schematic diagram for generic nanoimprint lithography procedure using soft polydimethylsiloxane (PDMS) stamps and a silica based sol-gel imprint resist

The SiO_x sol-gel resist solution can be spin-coated onto Si substrates to form a 100 nm-thick layer of imprint resist. A soft PDMS stamp is then brought into conformal contact with the substrate and physically displaces the layer of sol-gel material and capilary forces drive the resist to flow in and around the features of the PDMS stamp. While in contact, the silica sol-gel cures over time as it undergoes hydrolysis and condenstation reactions resulting in the formation of a solid SiO_x network. Once the sol-gel is cured, the PDMS stamp is carefully released from the substrate leaving behind a patterned SiO_x replica of the original master pattern. This process can

be repeated many times in order to generate identically patterned SiO_x templates on Si substrates for the SAG of III-V materials.

1.2.1 Imprint Lithography for Selective Area Growth

Because NIL and substrate conformal imprint lithography (SCIL) are still emerging as commercialized techniques to achieve low-cost nanoscale patterning, the successful process development on a research scale at NREL lends itself to many applications yet to be explored within the renewable energy technology field. With imprint lithography, nanoscale regions of Si can be exposed to enable template assisted SAG of high quality III-V materials. With the potential to reduce the cost of epitaxial growth by 60% and total tandem solar cell cost by 17% [25], template assisted selective area growth using NIL can revolutionize the fabrication-cost of integrating high efficiency III-V materials on Si by replacing the thick and expensive metamorphic buffer layers commonly used to combat lattice mismatch.

In an effort to meet the goals of the DOE's SunShot Initiative, the cost competitive nature and high throughput capabilities of NIL paves a new avenue to investigate, understand, and optimize nanoscale SAG of III-Vs on Si substrates. The following content presented in Chapter 2 describes the process and development of substrate conformal NIL and the additional challenges that were addressed for research scale applications at NREL. Using the optimized process described in Section 2.4, Chapter 3 presents how nanoscale patterned SiO_x templates on Si substrates were used to enable the SAG of GaAs on Si substrates by metal-organic chemical vapor deposition (MOCVD).

CHAPTER 2

PROCESS DEVELOPMENT FOR SUBSTRATE CONFORMAL NIL

A densely patterned dielectric template with sub-100 nm wide openings and aspect ratios (height:width) of 1.4 or greater are predicted to successfully reduce relaxation thickness and achieve aspect ratio trapping of threading dislocations that are formed near the interface of lattice mismatched III-V materials on Si [21], [22]. Such pattern geometries pose unique challenges in developing the NIL process at a reasonable cost. Chapter 2 of this thesis focuses on the process development that was required to optimize pattern transfer fidelity, large area uniformity, and reproducibility of substrate conformal NIL, as characterized by a variety of techniques such as ellipsometry, profilometry, field effect scanning electron microscopy (FESEM), and atomic force microscopy (AFM).

First, Section 2.1 describes how a variety of Si master patterns were fabricated and prepared for NIL stamp fabrication. Next, the materials and process development required to optimize bi-layer PDMS stamp fabrication in-house is described in section 2.2. Section 2.3 offers the detailed procedure and materials that were used to synthesize a silica sol-gel imprint resist in-house. Finally, Section 2.4 and 2.5 present how the substrate conformal NIL process was optimized using bi-layer PDMS stamps to manually imprint the silica based sol-gel resist on Si substrates and deliver high pattern transfer fidelity for research scale applications in SAG of III-Vs on Si, discussed in Chapter 3.

2.1 Patterned Si Masters

In collaboration with the University of Santa Barbra's Nanofabrication Facility, several Si masters were designed and patterned with feature sizes ranging from the micron-scale to the nano-scale using DUV or electron-beam (e-beam) lithography. To optimize the NIL process

including stamp fabrication and synthesis of a silica based sol-gel resist, 4" Si wafers were patterned over their full area by DUV lithography with an array of circles ranging in size from 150 nm to 2.5 μm. In a single stamp fabrication or imprint process, pattern transfer fidelity could be characterized for a variety of feature sizes using this DUV pattern. To maintain reasonable cost, a few Si masters were patterned with a small 1 cm^2 area by e-beam lithography to achieve sub-100 nm size features. Additionally, full-area nanoscale patterns on a 4" Si wafer were fabricated by DUV lithography and uniformly coated with SiO_2 to achieve line features down to 140 nm with a 280 nm pitch and an aspect ratio approaching 1.4.

2.1.1 Preparation and Anti-Stick Treatment of Si Masters

Before any PDMS materials are allowed to come into contact with the patterned Si master, the surface of the Si master was treated with an anti-stick layer (ASL), shown in Figure 2-1(a) in order to facilitate the release of the fully cured bi-layer PDMS stamp materials. The ASL coatings are accomplished by reducing the surface energy of the patterned Si surface by vapor deposition of 1H,1H,2H,2H-perfluorooctyl trichlorosilane (F_{13}-OTCS) that bonds to the surface to form a self-assembled monolayer [40]. Without a uniform and securely bonded anti-stick layer (ASL) across the nanoscale patterned Si surface, the PDMS material can bond to the Si surface and cause defects to form when the nanoscale, high aspect ratio PDMS features are released from the surface of the Si master (Figure 2-1). A uniform deposition and securely bonded self-assembled monolayer of F_{13}-OTCS requires a thorough cleaning process and surface preparation of the Si master to ensure good pattern transfer fidelity after releasing a PDMS stamp [41].

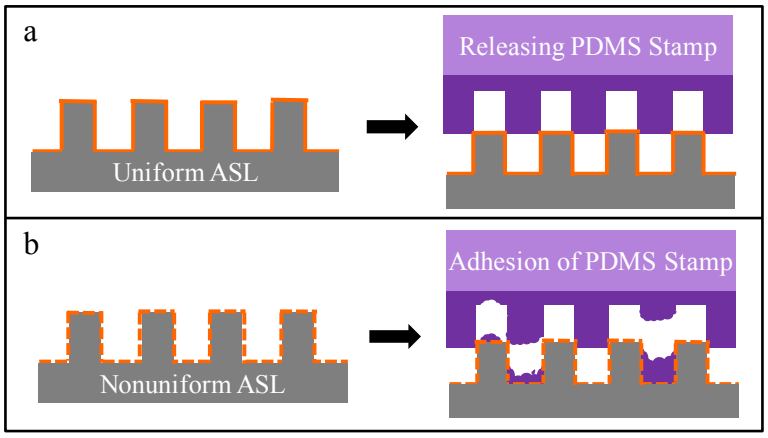

Figure 2-1 Schematic diagram of how uniformity and stability of anti-stick layer (ASL) deposition on Si master affects pattern transfer fidelity from Si master to the PDMS stamp

To prepare the Si surface for a uniform and stable ASL deposition, the Si masters are first cleaned in a mixture of tetrabutylammonium fluoride (TBAF) and Microposit™ 1165 Remover in a ratio of 1:3 by volume for 1-8 hours. This TBAF bath treatment of the Si master aided in the removal of any residual PDMS material remaining from previous stamp fabrication processes. After the TBAF bath, the Si masters were rinsed using acetone, isopropyl alcohol, and deionized water before they were dried with N_2. The Si masters, after they were cleaned from prior fabrication processes, were submerged in a piranha cleaning solution (a mixture of sulfuric acid and hydrogen peroxide in a ratio of 4:1 by volume) to dissolve any trace organics or particulates. After 15 minutes, the Si masters were thoroughly rinsed in a deionized water bath for 1 minute. Finally, the Si masters were then cleaned and oxidized in an ozone atmosphere using a Novascan PSD Pro Series Ozone system for 5 minutes at room temperature to generate a thin nonstoichiometric silicon oxide and hydroxyl groups on the surface of the Si master to aid in the bonding of a self-assembled monolayer of the F_{13}-OTCS [40]–[42] formed by vapor deposition.

After ozone treatment, 60 microleters (μL) of F_{13}-OTCS was placed in a glass vial and placed inside of a large desiccator next to the Si master and pumped under vacuum, from 816

mbar (at a mile-high altitude), to about 210 mbar at room temperature for 12 - 24 hours. Under vacuum, the F_{13}-OTCS molecules were deposited onto the surface of the Si master by vapor deposition. The reduction in surface energy for a sufficient ASL coating was verified by a water contact angle measurement of 118° on the surface of a patterned Si master [40].

After PDMS stamp fabrication, discussed in Section 2.2, the PDMS materials are cured and released from an ASL coated Si master and then characterized by top-down SEM imaging of a heavily gold-coated surface of the PDMS stamp. If the surface preparation and ASL deposition process lead to a uniform and stable binding of a self-assembled monolayer, the resulting PDMS stamp surface did not show any signs of delamination due to adhesion to the Si surface while it was released. However, if the Si master surface preparation and subsequent ASL deposition failed to promote a uniform and stable self-assembled monolayer defects, possibly due to adhesion such as delamination of PDMS features, can be observed in SEM (Figure 2-2).

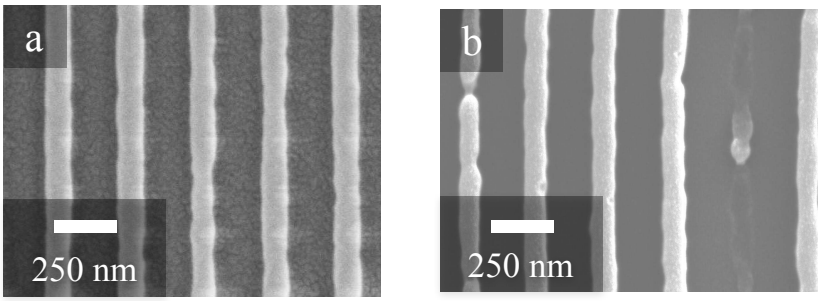

Figure 2-2 Scanning electron microscope (SEM) image characterization of two PDMS stamps made from the same Si master are patterned with 140 nm lines wide lines that are 200 nm tall (a) good pattern transfer fidelity (b) poor pattern transfer fidelity

The amount of water content present at the time of ASL deposition has been shown to significantly influence the quality and stability of the self-assembled monolayer that forms on the surface of Si [41]; water content on the surface left over from cleaning processes, or in ambient, reacts with the silane while binding to the Si surface takes place and HCl is formed. With too

much water content, the reaction can be enhanced causing bulk polymerization between adjacent silane molecules and increased roughness of the Si surface. Meanwhile, extremely dehydrated surfaces would not allow the binding reaction to take place. The SEM images shown by Figure 2-2 are of two stamps that were made from the same Si master which underwent virtually the same preparation and ASL deposition processes as described above. However, the pattern transfer fidelity was found to vary. Although this could be a product of changing functionality of PDMS precursors over time, described in Section 2.2.1, lack of humidity control at the time of deposition, combined with varying time and exposure to atmosphere between ozone treatment and deposition could have also caused variations in the resulting quality of ASL.

Moving forward, the ASL deposition process could gain reproducibility in a few different ways. The stability and uniformity of the final self-assembled monolayer could be optimized with more precise control of water content present during each ASL deposition. Water content can be controlled by the addition of a dehydrating step prior to UV-Ozone treatment and co-evaporation of water with F_{13}-OTCS at elevated vacuum levels (75-35 mbar) [41]. Process optimization can be characterized by water contact angle measurements as a function of vacuum level and amount of co-evaporated water. Alternatively, the cleaning and ASL treatment of Si masters is a service that is offered commercially by companies like NIL Technologies (NILt). Because the prices for these services from NILt range around $2,000/Si Master, this option is not economically sustainable for research scale applications. In contrast, improved reproducibility of ASL treatments can be offered by molecular vapor deposition (MVD) of trichlorosilanes at UCSB, with improved control over humidity and vacuum level. Furthermore, this ASL treatment can be carried out immediately after Si master fabrication and cleaning by their nanofabrication team.

2.2 Bi-Layer PDMS Stamps

To replicate densely packed nanoscale features with aspect ratios greater than 1, a bi-layer composite PDMS stamp structure varying in Young's modulus offers many advantages over using the commonly used and commercially available Sylgard 184 PDMS (S-PDMS) [43]. With a lower modulus of <10 megapascal (MPa), nanoscale features with high aspect ratios made from S-PDMS are vulnerable to feature collapse and permanent deformation throughout the NIL process [44] ; this is exacerbated by poor control of imprint pressures applied by hand. For example, for nanoscale features 50 nm wide, 100 nm tall and 50 nm apart, a Young's modulus of about 40-80 MPa has been shown to offer good feature stability [30]. Although PDMS with such an increased Young's modulus (X-PDMS) is not yet commercially available, it can be fabricated in-house as described later in Section 2.2.1.

To get the best of both worlds, a bi-layer PDMS stamp was fabricated by combining both X-PDMS and S-PDMS layers as shown in Figure 2-3. First, an anti-stick layer (ASL) treatment of the nanoscale patterned Si master, as discussed in Section 2.1.1, was applied to facilitate the release of PDMS stamp materials after they have crosslinked. The first layer of the bi-layer PDMS stamp was fabricated from an X-PDMS mixture that was prepared and spin-coated onto the Si master to form a thin layer of 40-50 μm, as described Section 2.2.1. The thin X-PDMS layer was used to facilitate high aspect ratio, nanoscale pattern transfer fidelity from the Si master. The X-PDMS layer was then backed with a thick layer of S-PDMS in order to allow conformal contact to the substrate and provide tolerance for some surface irregularities such as particulates or non-planar surfaces. After the PDMS materials have cured over time, the bi-layer PDMS stamp can be released from the Si master and used for subsequent NIL processing.

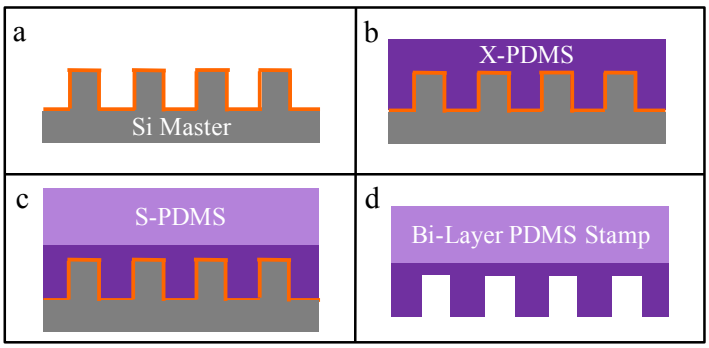

Figure 2-3 Bi-layer PDMS stamp fabrication procedure (a) ASL treatment of nanoscale patterned Si master (b) Spin-coat Si master with thin high modulus X-PDMS (c) Add thick softer S-PDMS backing (d) Cure PDMS materials and release from Si master

2.2.1 Bi-layer PDMS Stamp Fabrication

An increased Young's modulus of PDMS material was achieved by introducing a highly branched vinyl Q-Siloxane, shown in Figure 2-4 [45], to a mixture of linear and hydride siloxanes in a specific ratio by weight as described in **Error! Reference source not found.** [30]. he amount of platinum (Pt) catalyst and organosilane moderator (M) are added in specific amounts to expand the window of workability to about 10-15 minutes such that the viscous materials can be thoroughly mixed, degassed, and spin-coated before beginning to crosslink. With a large window of workability, the final X-PDMS mixture can be spin-coated onto the surface of a patterned Si master, allowing the material to flow and conform to the features on the

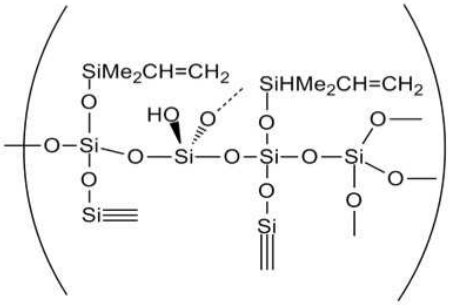

Figure 2-4 Material structure of highly branched Vinyl Q-Siloxane Resin [45]

Si master before the PDMS network forms.

The SpeedMixer™ by FlackTek, Inc. is a specially designed centrifuge that uses both on-axis and revolutionary-axis of rotations of a sterile mixing cup. Additionally, the SpeedMixer™ enables the mixing of viscous materials under vacuum in order to degas and remove entrapped air from the mixture. The mixing of X-PDMS siloxane materials described in Table 2-1 can be broken down into two parts (A and B) and six steps as shown in Figure 2-5 [30]. For duplicating a standard 4" Si master, first, 4.80 grams of Vinyl Q-siloxane (Q) was added to 3.00 grams of Vinyl Linear Siloxane (L) to accomplish an (L:Q) ratio of (1:0.8) by weight of solid Q content. These materials are mixed and degassed together inside of a max-20 gram mixing cup with a perforated closed lid under vacuum (around 300-400 torr) at 3000 RPM for 30 seconds using the SpeedMixer™. Next, 0.075 grams of the platinum (Pt) catalyst and 0.135 grams of the organosilane moderator (M) are carefully measured and added to the mixture of L and Q using a micropipette for precise control of their relative ratios by weight. Again, all of these precursors are thoroughly mixed and degassed together under mild vacuum to form Part A of the X-PDMS mixture. Once Part A is thoroughly mixed and degassed, Part B, 1.755 grams of the Hydride Linear Siloxane (R), can be added to Part A and mixed together under vacuum once more to form the final X-PDMS mixture as shown in Figure 2-5.

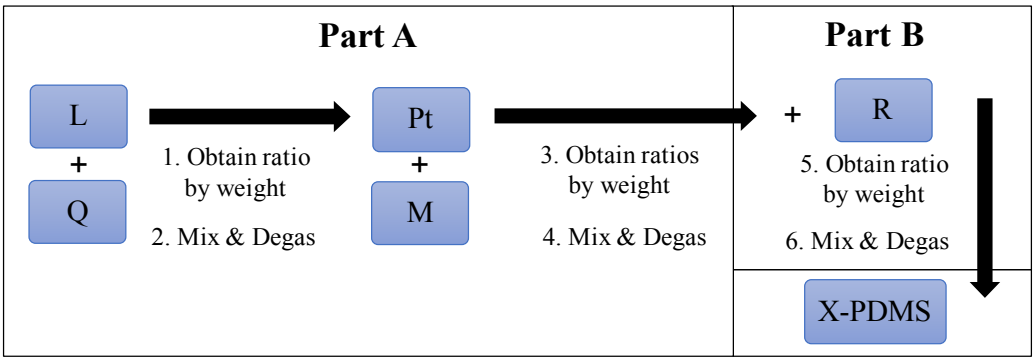

Figure 2-5 X-PDMS material fabrication procedure to achieve an increased Young's modulus using vinyl linear (L), Q-siloxane (Q), catalyst (Pt), moderator (M), and linear siloxane (R)

Table 2-1 X-PDMS precursurs and relative amounts used to achieve an increased Young's modulus. Measured weights noted here are typical for a 4" Si master

Part A					
Material Type	**Label**	**Chemical Name**	**Company Product No.**	**Ratio by Weight**	**Measured Weight (g)**
Vinyl Linear Siloxane	**L**	7-8% (vinylmethylsiloxane) (dimethylsyloxane), copolymer, trimethylsilyl terminated	Gelest Inc. VDT-731	(L:L) 1 : 1	3.000
Vinyl Q-Siloxane	**Q**	vinyl modified Q-silica resin, 50 wt% in xylene	Gelest Inc. VQX-221	(L:Q) 1 : 0.8	4.800
Organosilane Moderator	**M**	1,3,5,7-tetravinyltetramethylcyclotetrasil siloxane	Gelest Inc. SIT7900.0	(L:M) 1 : .045	0.1350
Platinum Catalyst	**Pt**	Platinum – divinyltetramethyldisiloxane complex in xylene	Sigma Aldrich® SIP6831.LC	(L:Pt) 1 : 0.025	0.0750
Part B					
Hydride Linear Siloxane	**R**	50-55% (methylhydrosiloxane) 45-50%(dimethylsiloxane) copolymer	Gelest Inc. HMS-501	(L:R) 1: .585	1.755

The final mixture of X-PDMS is spin-coated onto a Si master at 500 RPM for 30 seconds to form a 40-50 μm thick layer. The spin-coated layer of X-PDMS on the Si master is allowed to sit in ambient conditions for 5 minutes before it is placed on a hotplate at 50 °C for 10 minutes while the S-PDMS mixture is prepared. The S-PDMS mixture is fabricated from the Sylgard 184 Elastomer kit by Dow Corning where the elastomer base and curing agent are mixed together in a ratio of 10:1 by weight using the SpeedMixer™ and then degassed inside of a desiccator for 2 minutes. The X-PDMS coated Si master is then laid flat in an aluminum foil lined petri dish, and the S-PDMS mixture is poured over the top, resulting in an S-PDMS layer that is anywhere between 0.25 to 1.0 centimeter (cm) thick depending on the amount that is mixed and poured. The S-PDMS filled petri dish containing the submerged X-PDMS coated Si master are then

degassed together once more for 10-20 minutes until there are no visible bubbles formed due to outgassing of the S-PDMS.

The petri dish mold containing the Si master and PDMS materials are then cured together in a traditional convection oven at 50 °C and atmospheric pressure. After 5 days, the X-PDMS layer is fully cured and is successfully bonded to the S-PDMS material. To release the bi-layer PDMS stamp from the Si master, a scalpel is used to carefully cut away the excess material to expose the outer edge of the Si master. With the help of an anti-stick layer coated on the surface of the Si master, the bi-layer composite stamp can be gently peeled away from the Si master without causing damage to the PDMS patterned features as they are separated from the Si surface over the course of a few minutes.

Scanning electron microscopy (SEM) and atomic force microscopy (AFM) are used to properly characterize the pattern transfer fidelity of nanoscale features from a Si master to a PDMS stamp, as discussed in Section 2.4 and 2.5. As a preliminary measure of successful and uniform pattern transfer from a Si master to a bi-layer PDMS stamp surface, patterned arrays of micron and nanoscale features result in visible diffraction of light on the surface of the stamp; the color of the diffraction pattern observed depends on the feature scales and pitches that are present. For example, the Si masters that were patterned with DUV lithography were patterned with 3 by 4 arrays of squares where each square has a different feature size and pitch ranging from over a micron to just under 200 nm. The array of patterned squares results in a systematic array of colors which can be seen on the master and an inverted image of which can be seen by eye on a successfully fabricated bi-layer PDMS stamp, as shown in Figure 2-6.

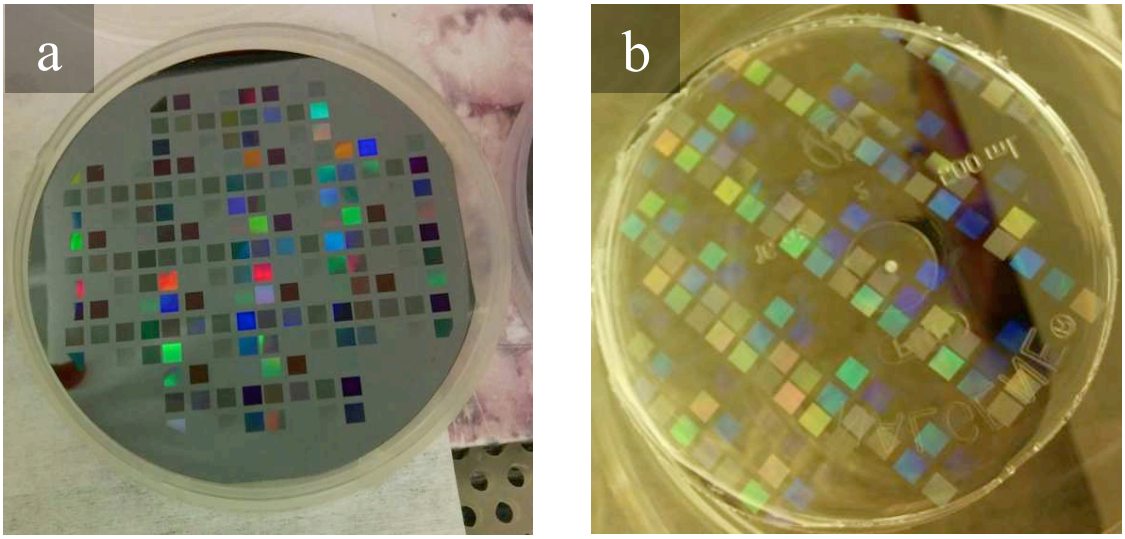

Figure 2-6 Photograph of (a) DUV interference patterned Si master demonstrates visible diffraction from patterned square regions (b) a PDMS stamp, molded from the Si master, demonstrates pattern transfer with visible diffraction pattern

2.2.2 Prevention of Q-Siloxane Aggregates

Near Denver, CO where the atmospheric pressure is 20% less than at sea level, the xylene used for dispersion of Q-Siloxanes can easily evaporate, leaving behind crystalized aggregates of Q-Siloxanes. The Q-Siloxane aggregates that appear during the mixing of X-PDMS precursors were found to disrupt the uniform spin-coating of the final X-PDMS mixture onto the Si master, as shown in the photograph in Figure 2-7. The formation of Q-Siloxane aggregates was difficult to avoid at elevation, and as a result, careful consideration was taken when handling, sealing, and storing the Q-Siloxane dispersion to prevent prematurely evaporated xylenes. As an additional measure to prevent a large number of these aggregates from being introduced, a syringe and 0.20 μm filter was used to prevent particle transmission while dispensing the Q-Siloxane suspension to the X-PDMS mixture of precursors.

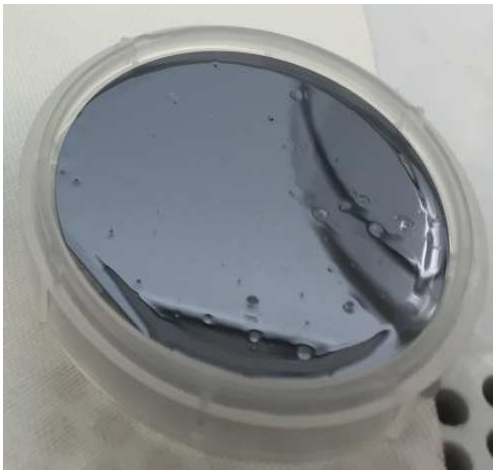

Figure 2-7 A photograph of the Q-Siloxane aggregates that can impede the uniform coating of X-PDMS layers on the surface of Si masters

2.3 Silica Sol-gel Imprint Resist

A silica (SiO_x) sol-gel imprint resist has been shown to demonstrate nanoscale pattern transfer fidelity with high aspect ratios using substrate conformal NIL [30], [36]. The SiO_x sol-gel resist is made from a mixture of liquid alkoxides, e.g. $Si\text{-}(O\text{-}CH_3)_x$, that react with water and alcohol to form an Si-O-Si (silica) network through careful control of hydrolysis and condensation reactions, described for a single ligand on the silicon by equations (2.1) and (2.2), respectively. After spin-coating a layer of SiO_x sol-gel resist onto a substrate and imprinting with a PDMS stamp, the Si-OH products of hydrolysis are allowed to fully react through condensation to form a solid silica network; the remaining alcohol and water products of each reaction are removed by diffusion into the PDMS stamp and later evaporated.

$$Si\text{-}\left(O\text{-}CH_3\right) + H_2O \leftrightarrow Si\text{-}OH + H\text{-}OCH_3 + \Delta_{heat} \quad (2.1)$$

$$Si\text{-}OH + OH\text{-}Si \rightarrow Si\text{-}O\text{-}Si + H_2O + \Delta_{heat} \quad (2.2)$$

2.3.1 Fabrication of SiO_x Sol-gel Imprint Resist

The porosity, stability, and time required to form the final Si-O-Si network after spin-coating is dependent on the degrees of hydrolysis and condensation that are reached in the sol-gel resist mixture throughout synthesis, storage, and the NIL process. The degree of hydrolysis and condensation reactions are determined primarily by the exact concentration of reactants and products that are present, including heat, throughout the synthesis and storage of the final SiO_x sol-gel mixture (before imprinting). For example, in order to regulate the concentration of reactive alkoxides during synthesis, methyltrimethoxysilane (MTMS), shown in Figure 2-8(b) was mixed with tetramethylorthosilicate (TMOS), shown in Figure 2-8(a), in a specific molar ratio with careful control of solution temperature.

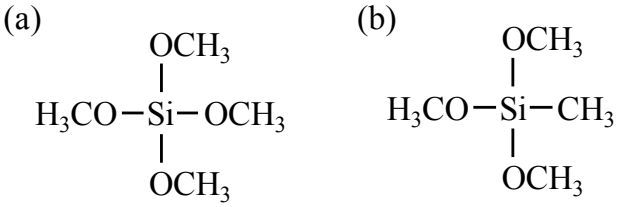

Figure 2-8 Molecular structure of alkoxides (a) Tetra-methyl-ortho-silicate (TMOS), $(Si\text{-}OCH_3)_4$ and (b) Methyl-tri-methoxy-silane (MTMS), $CH_3\text{-}Si(OCH_3)_3$

The fabrication process of SiO_x sol-gel imprint resist was developed according to a recipe which reports the optimization of substrate wettability, time to imprint, and pattern transfer fidelity by careful control of molar ratios between reactants and products during synthesis, storage, and NIL processing. The final SiO_x sol-gel imprint resist is fabricated by mixing two parts, (A) the base hydrolysis solution and (B) a dilution solution, in a controlled ratio of 1:1 by weight [30]. First, the base hydrolysis solution (Part A) is synthesized using the exact amount of materials listed in Table 2-2and following the detailed procedure shown in Figure 2-9.

Table 2-2 List of precursors and their relative amounts required for the synthesis of parts A and B to SiO_x sol-gel imprint resist mixture

Part A: SiO_x Sol-gel Base Hydrolysis Solution			
Label	**Chemical Name & Molecular Formula**	**Sigma Aldrich ® Product No.**	**Volume (mL)**
TMOS	Tetramethylorthoslicate $(Si\text{-}OCH_3)_4$	341436	7.4
MTMS	methyltrimethoxysilane $CH_3\text{-}Si(OCH_3)_3$	679232	7.1
n-prop	n-propanol (1-propanol) C_3H_8O	402893	121
Acidified Water	0.2 mL formic acid + 6.3 mL DI $CH_2O_2 + H_2O$ (1 mol/L)	-	6.5
DI	deionized water H_2O	-	9.9
Part B: SiO_x Sol-gel Dilution Solution			
Label	**Chemical Name & Molecular Formula**	**Sigma Aldrich ® Product No.**	**Weight (g)**
BEEA	2-(2-Butoxyethoxy)ethyl acetate $C_{10}H_{20}O_4$	537535	1.0 - 1.5
n-prop	1-propanol (n-propanol) C_3H_8O	402893	49.0 - 48.5

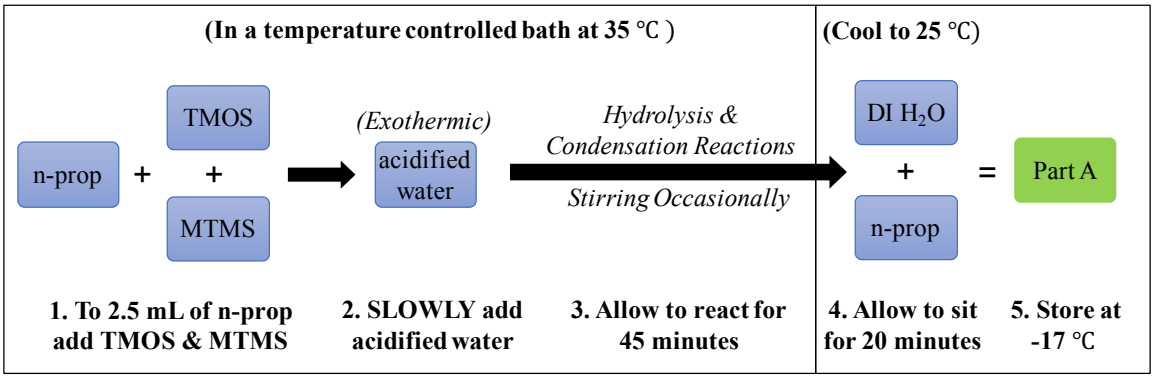

Figure 2-9 Procedure for the synthesis of the SiO_x base hydrolysis solution (Part A of SiO_x sol-gel imprint resist) using tetramethylorthosilicate (TMOS), methyltrimethylsiloxane (MTMS) and n-propanol

The temperature during synthesis of Part A, the base hydrolysis solution, was maintained by a heated water bath at 35 °C which surrounded the reaction vessel, a 250 mL round bottom flask where the silica sol-gel precursors were allowed to react. The first three precursors (n-propanol, TMOS, and MTMS) were heated to over 30 °C as measured using a traditional mercury thermometer before acidified water was thoroughly mixed into solution to catalyze the hydrolysis reaction. As discussed in Section 2.3.2, the exothermic nature of hydrolysis and condensation reactions make temperature control and uniform mixing during the addition of acidified water critical to control the degree of hydrolysis and prevent early network formation. After 45 minutes of reaction time in a heated water bath, the hydrolysis solution is allowed to cool to room temperature and sit for 20 minutes. Finally, deionized water and n-propanol were added to complete the final mixture of Part A and suspend the condensation reactions while stored in a freezer at -17 °C

Next, the dilution solution (Part B of the SiO_x sol-gel resist) was made from a mixture of n-propanol with 2-3% by weight of 2-(2-Butoxyethoxy)ethyl acetate (BEEA), as described in Table 2-2, and stored in a refrigerator at ~4 °C. The addition of a dilution solution to the hydrolysis base solution prevents hydrolysis and condensation reactions from proceeding during storage and lowers the viscosity of the SiO_x sol-gel resist such that it can be spin-coated and imprinted before the condensation reactions take place to form the solid patterned SiO_x network. The final sol-gel resist solution was made by adding Part A and Part B together immediately before imprinting in a ratio of (1:1) by weight with 2-3 grams of each depending on the total surface area or number of imprints intended to be imprinted that day.

2.3.2 Temperature Control & Early SiO_x Network Formation

During synthesis of Part A, the hydrolysis base solution, two key observations indicate the onset of hydrolysis reactions taking place upon the mixture of acidified water; the transparent mixture of TMOS and MTMS becomes cloudy with the formation of Si-OH compounds, while the temperature of solution increases due to the exothermic reactions taking place. The amount of increased temperature and extent of reaction was dependent on the initial temperature of solution before the addition of acidified water and the rate which the acidified water was added to solution. Therefore, to maintain control of the extent of hydrolysis reaction, the temperature of solution in the reaction vessel was controlled by the heated water bath above room temperature at 35 °C. Additionally, the acidified water was slowly added and thoroughly mixed into solution over the course of 1-2 min, rather than all at once, to prevent a drastic spike in temperature caused by a sudden increase in localized concentration of hydrolysis reactants in the vessel.

While hydrolysis reactions are taking place, the reactants required for condensation are naturally produced and present in solution, therefore condensation reactions can occur during synthesis and early network formation can be observed. Because the vessel hosting the synthesis of the SiO_x hydrolysis solution is predominately made of silica, the formation and bonding of an SiO_x film on the sidewalls during synthesis can be observed making it difficult to clean for re-use. A simple ASL vapor deposition of F_{13}-OTCS for 1 hour, like that done for Si masters and PDMS stamps, was found to aid in removing SiO_x films that form on the sidewalls during synthesis of the hydrolysis base solution.

Early SiO_x network formation during synthesis can also result in strings or particulates of SiO_x suspended in the hydrolysis base solution (Part A). As a result, a smooth uniform coating of the final imprint resist can be disrupted by the presence of these particulates after it is mixed with

Part B and spin-coated onto a Si substrate. To reduce the number of particulates, a 0.2 μm filter was used to dispense the SiO_x sol-gel resist mixture onto Si substrates prior to spin-coating for NIL (Figure 2-10).

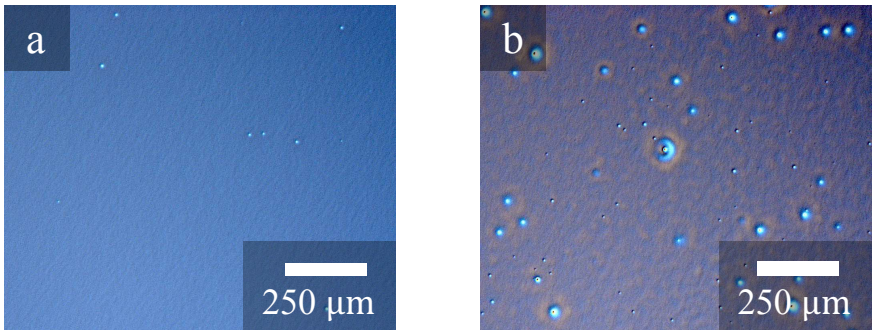

Figure 2-10 Optical image taken at 5X magnification compares an SiO_x sol-gel film dispensed and spin-coated (a) with a 0.2 μm filter and (b) without a filter, after baking

2.4 Optimization of NIL procedure

ASL treatment of Si masters, Bi-layer composite PDMS stamps fabrication, and synthesis of SiO_x sol-gel imprint resist solutions were all completed in-house as described in Sections 2.1, 2.2, and 2.3 respectively. After fabricating bi-layer PDMS from Si masters, they were subsequently used for substrate conformal imprint lithography with a silica sol-gel imprint resist to generate patterned SiO_x templates on the surface of polished Si substrates. Microscale- and nanoscale-patterned bi-layer PDMS stamps and the resulting patterned SiO_x layers on Si substrates were imaged using SEM and AFM to characterize and optimize the NIL process for maximum pattern transfer fidelity. With the following optimized procedures described below, polished Si surfaces were coated with SiO_x sol-gel resist, patterned by NIL using bi-layer PDMS stamps, and etched using a combination of wet chemical and reactive ion etching to expose patterned areas of Si for the SAG of III-Vs.

2.4.1 PDMS and Substrate Surface Preparations

Without a uniform and stable ASL, high aspect ratio features of PDMS are subject to defects caused by forces due to adhesion from imprinted layers of SiO_x after NIL processing. Without proper surface treatments of PDMS stamps and Si substrates before NIL processing, adhesion of SiO_x to the PDMS stamp and delamination of SiO_x from the Si surface can be observed for nanoscale features after imprint lithography. AFM and SEM image characterization of a PDMS stamp and imprinted SiO_x on Si with 200 nm size features after imprinting, shown in Figure 2-11, demonstrates how adhesion and delamination of sol-gel results when the PDMS and Si surface are not properly treated.

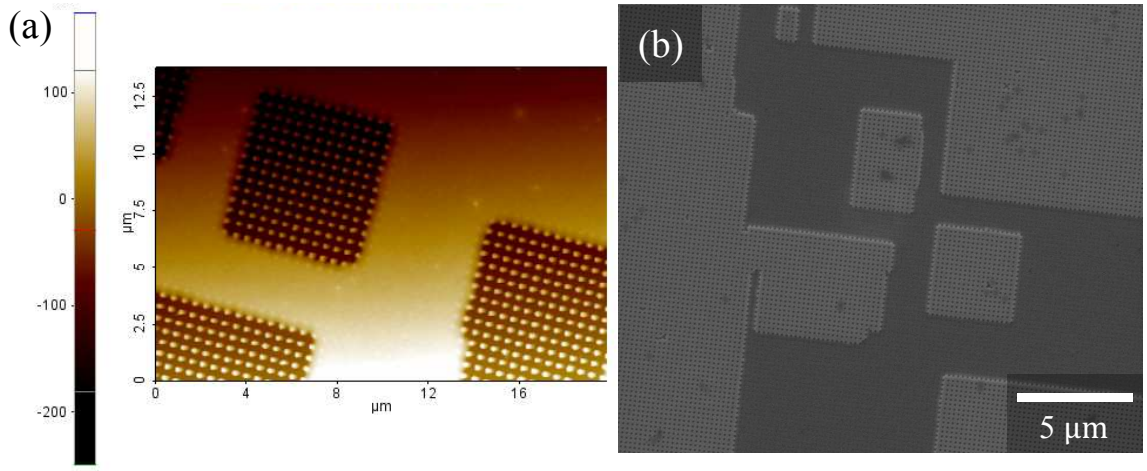

Figure 2-11 (a) AFM image characterization of nanoscale PDMS stamp surface after imprinting and (b) SEM of imprinted Si substrate; without proper surface treatments of Si substrate or PDMS stamp [AFM by Arrelaine Dameron and SEM by Emily Warren]

To optimize nanoscale pattern transfer fidelity from a bi-layer PDMS stamp to a layer of SiO_x sol-gel on Si substrates, the surfaces of Si substrates and PDMS stamps required different surface treatments prior to NIL processing, as shown schematically by Figure 2-12. An anti-stick layer (ASL) treatment on the surface of PDMS stamps was used to aid in the release from

imprinted SiO_x sol-gel resist layers on the surface of Si. An ASL coating was deposited onto patterned bi-layer PDMS stamp surfaces by vapor deposition immediately after they were released from the patterned Si masters [42]. For ASL treatment of PDMS stamps, a stamp is placed inside of a desiccator with its patterned surface face up next to a glass vial containing 60 µL of F_{13}-OTCS. Together, the PDMS stamp and vial of F_{13}-OTCS were held under vacuum (300-400 torr) at room temperature for 1-2 hours. While under vacuum, the F_{13}-OTCS molecules are deposited onto the surface of the PDMS stamp to prevent adhesion to the sol-gel resist material while the SiO_x network begins to form during contact with the stamp.

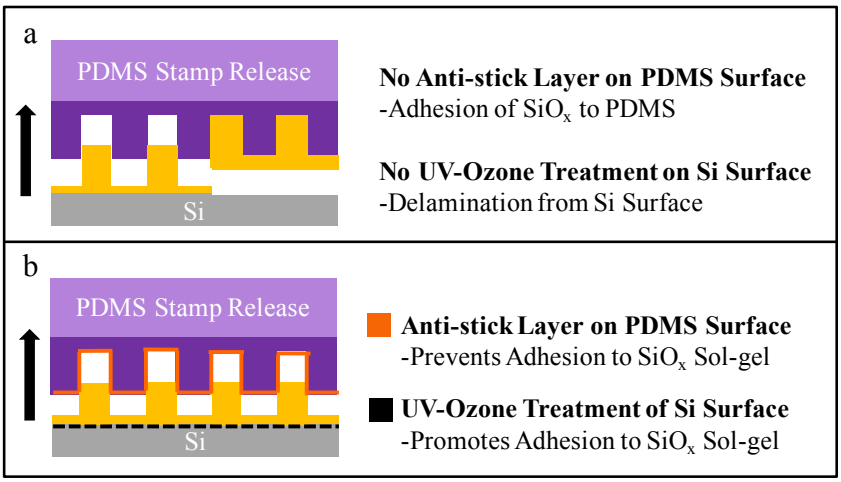

Figure 2-12 Schematic diagram illustrating the release of a PDMS stamp from an imprinted SiO_x sol-gel layer on the surface of Si (a) without and (b) with surface treatments of PDMS stamp and Si substrate

Before any Si substrates were used for MOCVD processing, they were first cleaved into 4 cm^2 pieces and cleaned by a standard RCA clean procedure to prevent the in-diffusion of contaminants while exposed to the high temperature environments required for the SAG growth of III-V's after imprinting. To clean, promote wetting of the sol-gel resist, and prevent delamination of SiO_x patterned layers during NIL, a Novascan PSD Pro Series UV Ozone system

was used to treat the surface of all Si substrates at 20 °C for 20 minutes. While cleaning the surface from any organic residue, the ozone treatment also produces a thin nonstoichiometric silicon oxide and hydroxyl (OH) groups on the surface of Si, which the silica sol-gel can easily wet and bond to. This UV-Ozone treatment was carried out immediately before the substrates were spin-coated with SiO_x sol-gel for substrate conformal imprint lithography processing, described in Section 2.4.2.

2.4.2 Substrate Conformal Imprint Processing

After a standard RCA clean procedure and UV-Ozone treatment, layers of SiO_x sol-gel resist were spin-coated onto the surface of Si substrates using a programmable spin-coater called Delta80 Resist Coater by SUSS MicroTec Inc. The Delta 80 resist coater was programed with a 7-step recipe described in Table 2-3 to accomplish a uniform coating of sol-gel resist with the help of a co-rotating lid which maintained a uniform vapor pressure throughout the spin-coat recipe. The resulting thickness of SiO_x sol-gel from this recipe was ~100 nm, as measured by ellipsometry after curing at 200 °C for 1 hour; variations of 5% in SiO_x thickness were observed between sample sets of imprints due to small variations in the measured weights while mixing Part A and Part B of the resist.

Table 2-3 Spin-coating recipe used to accomplish a uniform 100 nm-thick SiO_x sol-gel layer for Si substrates with minimal edge beading

Step	Lid status	Speed (RPM)	Acceleration (RPM/sec)	Duration (s)
1	open	100	150	8
2	close	100	230	6
3	close	600	1000	10
4	close	1500	1000	2
5	close	300	1000	3
6	open	0	500	1
7	open	0	230	0

Within 2 minutes of spin-coating a layer of SiO_x sol-gel resist onto a UV-Ozone treated Si substrate, an ASL coated bi-layer PDMS stamp was carefully brought into contact with the coated substrate by hand. The flexibility of the PDMS stamp materials allowed for one area of the stamp to come into contact with one side of the Si substrate to start. The point of contact is then brought across the substrate as the PDMS stamp is gently lowered to make full area contact without air inclusions, as shown in Figure 2-13(a). Because imprinting was done at atmospheric pressures, if the stamp was brought into contact with multiple sides of the substrate at once, shown in Figure 2-13(b) the intersection of multiple capillary fronts resulted in trapped air between the stamp preventing full area pattern transfer. In addition to prevent air inclusions and provide a uniform amount of imprint pressure for conformal contact to the substrate, a glass slide was also used to gently guide the stamp's point of contact as it was lowered onto the substrate.

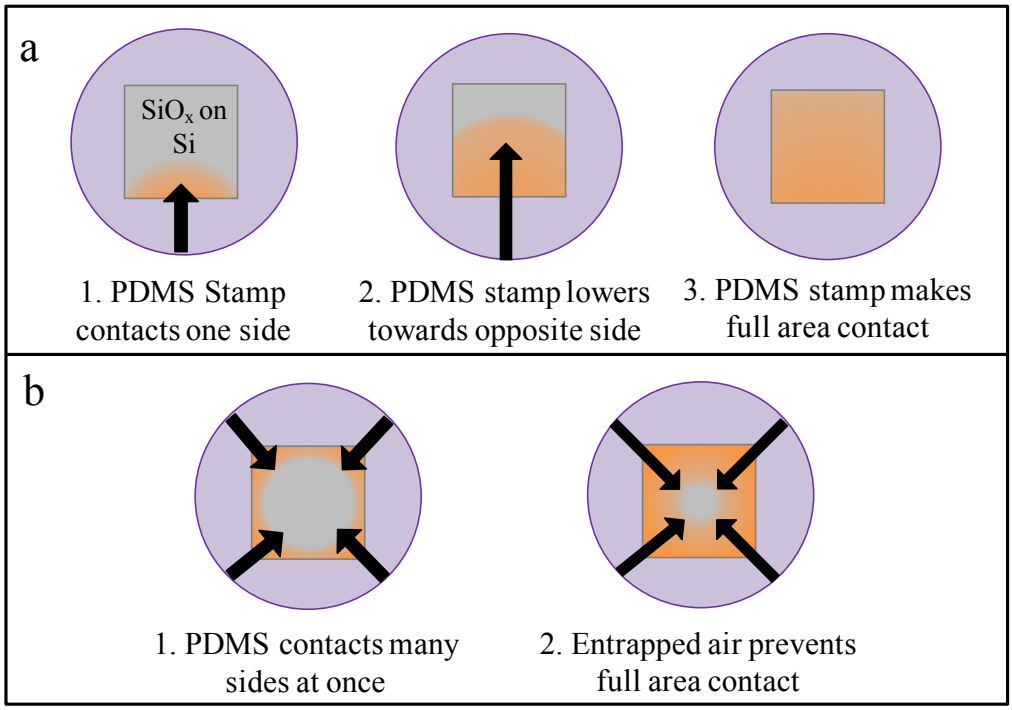

Figure 2-13 Illustration of how to contact PDMS stamp to SiO_x coated Si Substrate (a) without air inclusions and (b) with air inclusions

2.4.3 Exposing Si for III-V Heteroepitaxy

Although substrate conformal imprint lithography was developed to make conformal contact with the Si substrate, a small 10-50 nm residual layer of sol-gel typically remained beneath the PDMS features in the imprinted layer on the surface of the Si substrate. This is because the patterned surfaces of PDMS stamps have a specific amount of volume that sol-gel is able to flow into during the NIL process. The amount of volume offered by any PDMS stamp depends on the dimensions of the imprint pattern. With a standard 100 nm-thick layer of resist, the amount of residual sol-gel remaining below a given imprinted pattern depended primarily on the dimensions of the pattern being used for that imprint and the imprint pressures applied.

For example, after spin-coating a standard 100 nm-thick layer of sol-gel on a Si substrate, the total volume of sol-gel that is available to flow into the space offered by the pattern on a PDMS stamp is equal to $9x10^6$ nm^3 (over any $9x10^3$ nm^2 area of a Si). If a PDMS stamp pattern offers a volume less than the $9x10^6$ nm^3 of sol-gel that is available, once that space is filled during the imprint, there is nowhere for the remaining volume of sol-gel to flow. The residual volume remains below the patterned layer unless enough pressure is applied to force the sol-gel to flow out from under the stamp.

Each imprinted sample shown in Figure 2-14, was patterned by a different PDMS stamp with similar imprint pressures applied by hand. The PDMS stamp used to imprint the sample shown by Figure 2-14(b) provides just over $9x10^6$ nm^3 of space for sol-gel to flow over a $9x10^3$ nm^2 square area on the substrate; as a result the residual sol-gel observed after imprinting was less than 10 nm. Meanwhile, the PDMS stamp used to imprint the sample shown in Figure 2-14(a), provides only ~$4.4x10^6$ nm^3 of volume for sol-gel to flow into, which resulted in a

significant increase in the amount of residual sol-gel, 50 nm, observed below the pattern after imprinting.

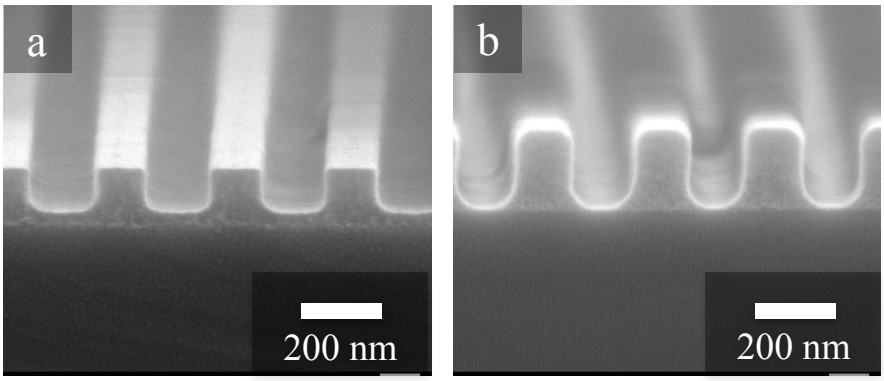

Figure 2-14 Cross sectional SEM micrographs of Au coated imprinted SiO_x layers on Si using different PDMS pattern geometries shows (a) 50 nm of residual sol-gel and (b) less than 10 nm of residual sol-gel

Because the amount of residual sol-gel also depends on the imprint pressure applied and the imprint process is done by hand, the exact amount of residual sol-gel that remained across the area of any patterned sample varied from one imprinted sample to another. In addition, for imprinting on larger substrate areas, such as on full 3- and 4-inch Si wafers, a uniform amount of imprint pressure by hand became more difficult with increasing area. As a result, a non-uniform amount of residual sol-gel across larger areas of substrates was also observed.

In order to remove the residual sol-gel and effectively expose regions of Si for selective area growth of III-Vs, the amount of residual sol-gel for any particular imprint intended for growth needed to be characterized. For characterization, a similar sized control sample was also patterned by NIL in parallel with the substrate intended for growth. The control sample patterned by NIL was then cleaved and a thin layer of gold was deposited for SEM characterization of the dielectric layer on Si. High resolution cross sectional images were taken using a FESEM with

low accelerating voltages and low current levels to reduce charging of the patterned layer of SiO_x and measure the residual thickness that remained under the patterned features after imprinting.

If the amount of residual sol-gel was less than 10 nm, a simple wet chemical etch was carried out with a hydrofluoric (HF) solution (1% concentration by volume for 55 seconds) to ensure that all residual sol-gel is removed to re-expose the atomic (001) surface of Si for heteroepitaxy. However, because a wet chemical etch is highly isotropic, if the residual sol-gel was much greater than 20 nm, a wet chemical etch alone would significantly increase the width of the features thereby decreasing the aspect ratio of the pattern. To maintain high aspect ratios, a more anisotropic dry reactive ion etch (RIE) was used to remove bulk SiO_x residual layers until less than 10 nm remained above the surface of Si.

In order to provide accurate control of the etch depth, the RIE recipe was optimized at 30 Watts using a CF_4 gas with 40 standard cubic centimeters per minute (sccm) flow to achieve an etch rate of SiO_x at 25 nm/minute. With a slow RIE etch rate, a 10 nm layer of SiO_x was left behind and later removed with an HF etch as described earlier in order to preserve the atomically smooth morphology of the Si substrate for heteroepitaxial growth. Etch rate calibrations were carried out on SiO_x, planar films that were spin-coated on Si substrates and baked at 200 °C for 1 hour. Relative etch rates, summarized in Table 2-4, were characterized using ellipsometry after exposure to wet and dry chemistries.

Table 2-4 Summary of SiO_x sol-gel etch rates by wet and dry processing, as measured by ellipsometry of planar films spin-coated and bake at 200 °C for 1 hour

Etch Method	Etch Parameters	Etch Rate (nm/min)
HF	1%	~12
RIE (Slow)	CF_4 | 30 W | 40 sccm	~25
RIE (Fast)	CF_4 | 60 W | 40 sccm	~80

2.4.4 Summary of Optimized NIL process

The final optimized NIL procedure can be broken down into three components; A. Bi-layer PDMS Stamp Fabrication, B. Nanoimprint Lithography on Si Substrates, and C. Preparation of NIL-patterned Si for SAG of III-V's. For each component to the optimized NIL process, there are several steps to insure good pattern transfer fidelity from the patterned Si master, to the Bi-Layer PDMS stamp, to the NIL-patterned SiO_x layer on Si substrates that are summarized by the schematic diagram shown in Figure 2-15. Using the optimized procedures for NIL, pattern transfer fidelity from a Si master to a patterned SiO_x replica was characterized by cross sectional SEM images taken from both the Si master and an NIL-patterned Si substrate and is discussed in Section 2.5.

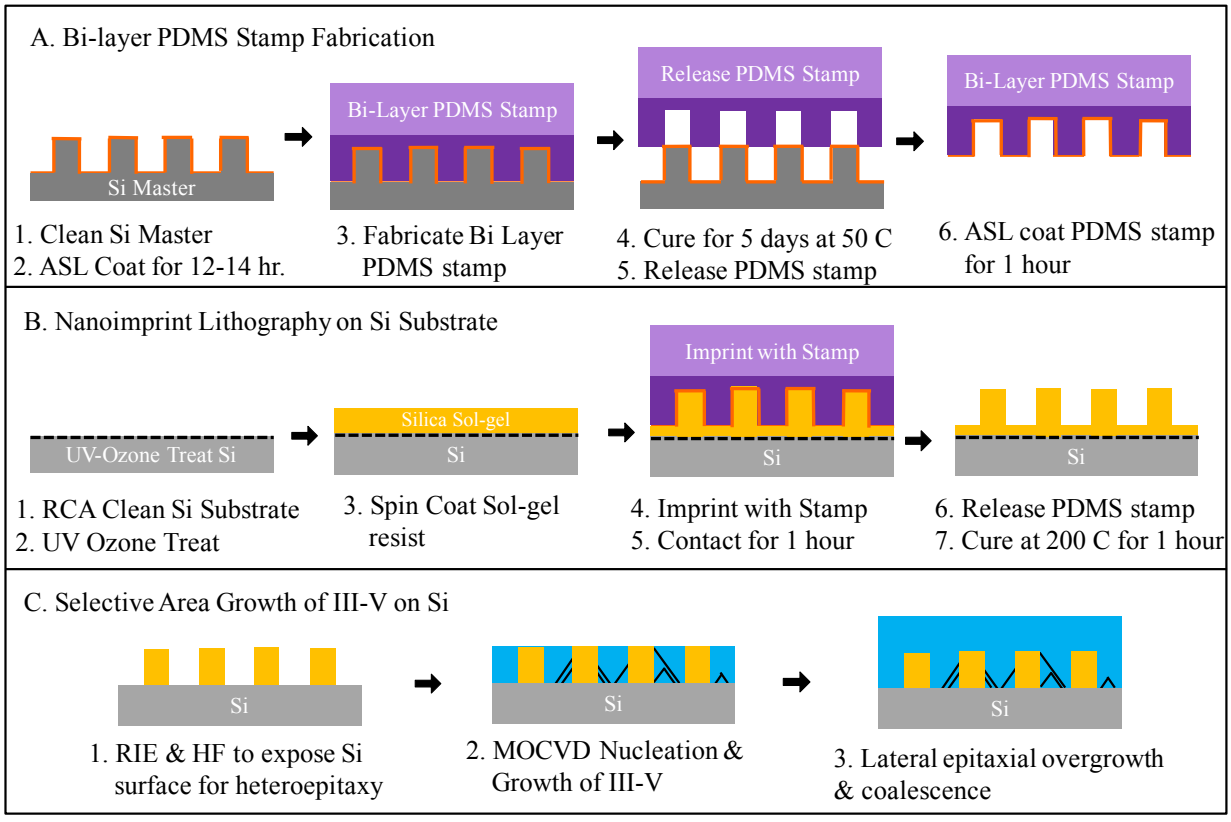

Figure 2-15 Summary of optimized NIL processing for substrate conformal NIL using bi-layer PDMS stamps and silica sol-gel imprint resist on Si substrates for SAG of III-Vs by MOCVD

2.5 Characterization of Pattern Transfer Fidelity

Because Si masters need to be kept clean for PDMS stamp fabrication, a limited number of Si masters were fabricated in identical pairs such that one could be used for characterization and the other could be used for PDMS stamp fabrication. For example, for one Si master containing line patterns, a duplicate Si master was fabricated in parallel such that it could be cleaved and imaged by cross-sectional SEM. The pattern transfer fidelity from the Si master to an SiO_x replica on Si, patterned by NIL, was characterized by cross-sectional SEM imaging and compared to that of the duplicate Si master (Figure 2-16).

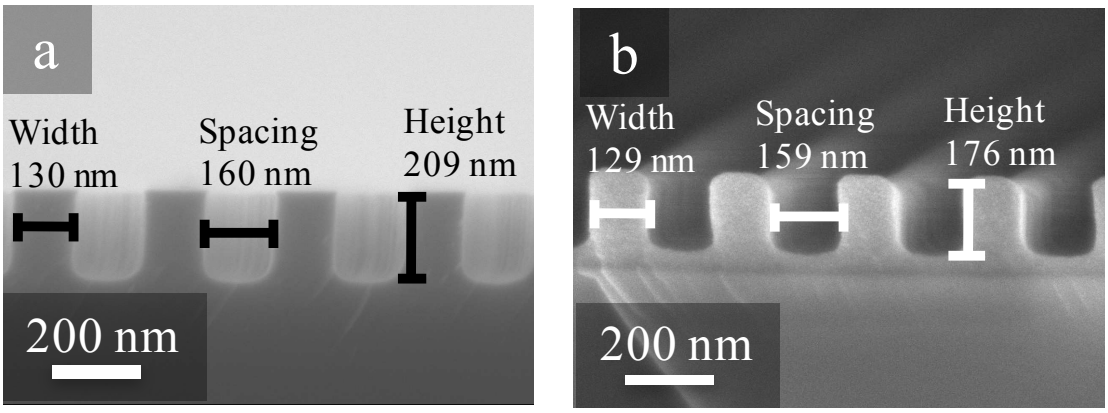

Figure 2-16 Cross-sectional SEM images used for characterization of pattern transfer fidelity from (a) the Si master pattern and (b) SiO_x on Si patterned by NIL

ImageJ software was used to measure and analyze the pattern geometry of the Si Master compared to the SiO_x replica on Si patterned by NIL (Figure 2-17). While the width and spacing of the NIL patterned lines varied by only 1% compared to the master, the aspect ratio of the openings (height/spacing) decreased from 1.3 on the master to 1.1 on the NIL patterned replica. The decreased aspect ratio of the NIL patterned replica can be attributed to a number of things. First, it is important to remember that the image characterization, shown in Figure 2-16, is not of

the actual master that was used to mold the PDMS replica. Variations in the final pattern transferred by NIL could be due to variations between the actual Si master and duplicate Si master that was characterized. However, assuming the two masters were truly identical, there are two other reasonable sources for the change in aspect ratio; the PDMS material may not have been able to completely fill in the features of the Si master during stamp fabrication, or the sol-gel imprint resist may not have been able to completely fill in the features of the PDMS mold during NIL; either, or a combination of both could result in a decreased height of features after imprinting into the sol-gel. In addition, although the original sol-gel resist chemistry has been optimized to minimize sol-gel shrinkage [30], the sol-gel solution has a limited shelf life; overtime the degree of hydrolysis reached during storage and can result in variations of the final crosslink density after imprinting and shrinkage of features can be observed as a result.

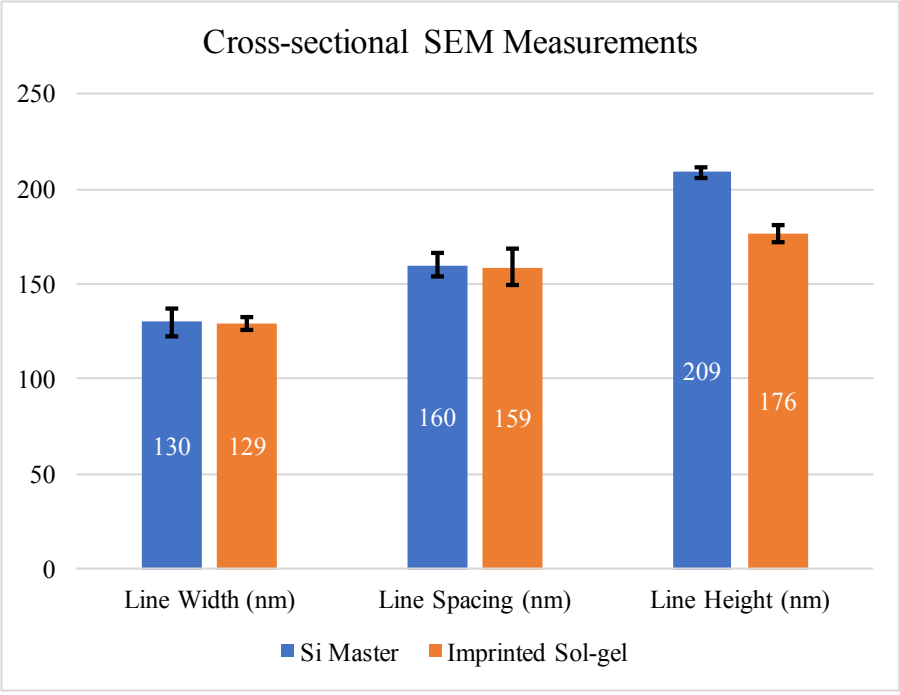

Figure 2-17 Summary line measurements recorded by ImageJ analysis of the cross-sectional SEM images shown in Figure 2-16 of the Si master and imprinted sol-gel sample

Further characterization of the PDMS stamps is required to gain information about the height of the PDMS features after stamp fabrication and definitively conclude the source of the decreased aspect ratio after NIL pattern transfer. We were unable to perform a simple cross-sectional cut of a PDMS stamp using a scalpel without damaging the soft nanoscale PDMS features. Therefore, we were not able to take a cross-sectional image of the PDMS stamp by SEM to determine the height of the features. Atomic force microscopy of the PDMS stamp should be used in future pattern transfer characterizations with careful consideration in choice of cantilever with an optimal aspect ratio and stiffness to accomplish a true profile of the nanoscale high-aspect-ratio patterned surface of the PDMS stamp.

CHAPTER 3

SELECTIVE AREA GROWTH OF III-VS ON SI

While progress has been made towards imprinting sub-100 nm feature sizes with increased aspect ratios, uniformity, and reproducibility, the successful development of NIL patterning of sol-gel SiO_x has paved a cost-effective avenue to investigate how selective area growth on the nanoscale can promote high-quality growth of III-V materials like GaAs on Si. Chapter 3 of this thesis walks through the process in which NIL-patterned SiO_x templates on Si have enabled the selective area nucleation and coalescence of single crystal GaAs grown by metal-organic vapor deposition (MOCVD). First described in Section 3.1 , the MOCVD growth parameters were optimized by Emily Warren and were used to investigate the viability of NIL-patterned SiO_x templates as a means to promote high quality of GaAs growth on Si.

As shown in Section 3.2, selective area epitaxial nucleation of GaAs on Si substrates coated with NIL-patterned SiO_x templates were characterized by various members of our research group using a number of techniques such as SEM, electron dispersive analysis x-ray (EDAX) spectroscopy, and transmission electron microscopy (TEM). Later in Section 3.3, the film quality and dislocation densities resulting from SAG on NIL-patterned silicon were characterized by TEM (in bright field, dark field, and high resolution imaging mode) by Andrew Norman and x-ray diffraction (XRD) by Adele Tamboli [46]–[48]. The preliminary results for accomplished SAG of III-Vs on patterned Si by NIL are presented here and compared to that of a planar (001) silicon substrate, both with and without a 3 or 4 degree offcut towards the [111] direction.

3.1 MOCVD Processing Parameters

Optimization of GaAs growth by MOCVD was performed by Emily Warren using two different reactors, one operated at a low pressure reactor of 50 torr, and another at atmospheric pressure; in general, both reactors were used to carry out a standard growth recipe described here [25]. First, samples were annealed under AsH_3 at ~900-1000 °C for 2 min to form a single domain As/Si terminated surface and suppress the formation of APDs [49]. In the first step of growth, islands of GaAs were nucleated on exposed regions of the Si substrate at a low temperature of ~450-500 °C and a low V/III ratio of 30 using AsH_3 and triethylgallium (TEG) precursors. After that short nucleation step, the V/III ratios were kept constant while the temperature was increased to 600 °C and the islands of GaAs were grown to fill in the patterned features. During the last step of growth, the V/III ratio was then increased to 200 at 600 °C to form a film that is typically 1.5 to 2 microns thick. For each template-assisted growth carried out on an NIL-patterned Si substrate, an identical Si substrate with no pattern was grown in the same reactor to investigate the effect that a template has on the formation of defects during nucleation and morphology of the final film. Optimization of NIL template processing and characterization of the selective area nucleation are described in detail below in Section 3.2. The investigation and characterization of final quality of GaAs films are described later in Section 3.3

3.2 Selective Area Nucleation of GaAs on Silicon

Using an optimized nanoimprint lithography process described in Section 2.4 and summarized in Section 2.4.4, SiO_x patterned templates on the surface of polished (001) Si substrates were fabricated for selective area heteroepitaxial growth of III-Vs. Various template geometries containing circles and lines have been produced with feature sizes ranging from 75 nm to over 2 microns. With a combination of wet and dry etch processing described in Section

2.4.3, micron to nanoscale areas of (001) Si substrates were exposed to generate templates to investigate selective area nucleation of GaAs as grown by MOCVD.

3.2.1 Characterization of Selective Area Epitaxial Nucleation

To optimize the first step of nucleation during the MOCVD growth process, micron scale and nanoscale patterned Si templates were prepared by NIL, and epitaxial growth was performed with planar Si substrates as a control sample. Top-down and cross-sectional SEM image characterization, shown in Figure 3-1, reveals the nanoscale patterned silica layer is capable of standing up to the high temperature MOCVD growth conditions. However, incomplete removal of residual silica sol-gel remaining on the surface of Si resulted in nucleation of GaAs islands on the SiO_x surface of the patterned substrate. Results such as this motivated the optimized two-step etch process that combined both dry and wet etching discussed earlier in Section 2.4.3 to ensure that the Si at the bottom of the vias were exposed.

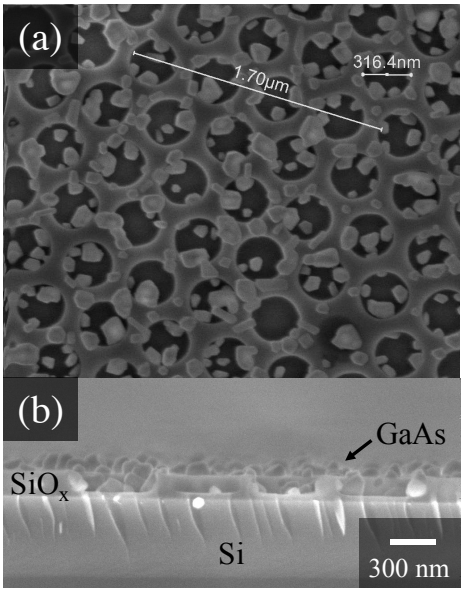

Figure 3-1 (a) Top down [By E.Warren] and (b) cross-sectional SEM imaging demonstrates random nucleation of GaAs on NIL patterned silica with 300 nm holes when Si substrate is not properly exposed; (Growth No. PD393)

For planar Si, the nucleation events of GaAs occurred across the surface of the substrate as expected, as shown by Figure 3-2(a). To confirm that SiO_x patterned templates could enable selective area nucleation, SiO_x templates with 2.5 µm scale features were patterned by traditional photolithography and the nucleation events after MOCVD growth were found to be selective to the exposed areas of Si as shown by Figure 3-2(b). Furthermore, EDAX was used to measure the composition of Ga, As, Si, and O across the large micron-scale features, as shown in Figure 3-3 and confirmed that the SiO_x templates were successfully used to promote truly selective area nucleation and growth of GaAs.

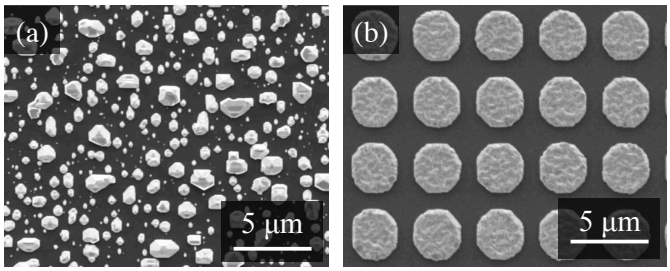

Figure 3-2 Top-down SEM image reveals (a) random GaAs nucleation on planar Si substrate and (b) 2.5 µm patterned SiO_x template enables selective area nucleation on exposed Si [Patterning of SiO_x by A. Tamboli; SEM image Characterization by E. Warren] ; (Growth No. PD369)

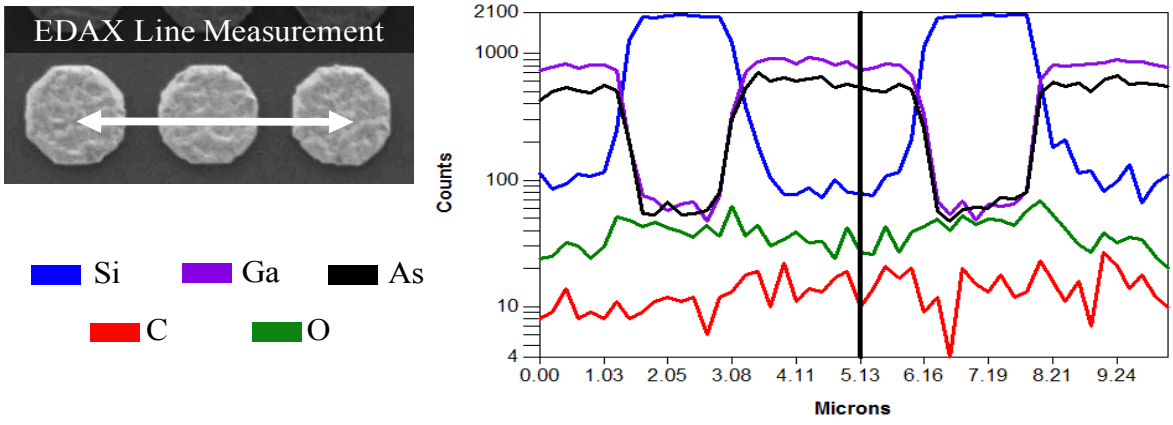

Figure 3-3 Electron dispersive analysis x-ray line characterization across 2.5 micron scale selective area growth of GaAs [by E. Warren]; (Growth No. PD369)

3.2.2 Characterization of Nulceation Events and Defect Formation

By decreasing the feature size of imprinted dots from 600 nm to 250 nm, the number of nucleation events that occurred within each exposed area of Si was observed to decrease (Figure 3-4). By restricting the nucleation area in size, the epitaxial growth of single crystal GaAs was observed and characterized by selected area electron diffraction (SAED) (Figure 3-5(a)). The electron diffraction pattern of selective area nucleation on an NIL-patterned Si surface revealed a partially relaxed zinc blend crystal structure of GaAs resulting from epitaxial growth on the surface of the crystalline (001) Si substrate. Although SAG of single crystal GaAs on Si was confirmed, high resolution transmission electron microscopy, shown in Figure 3-5(b) also revealed that the nucleation and subsequent growth filling the NIL patterned features are compromised by a variety of defects such as threading dislocations, stacking faults, and twins.

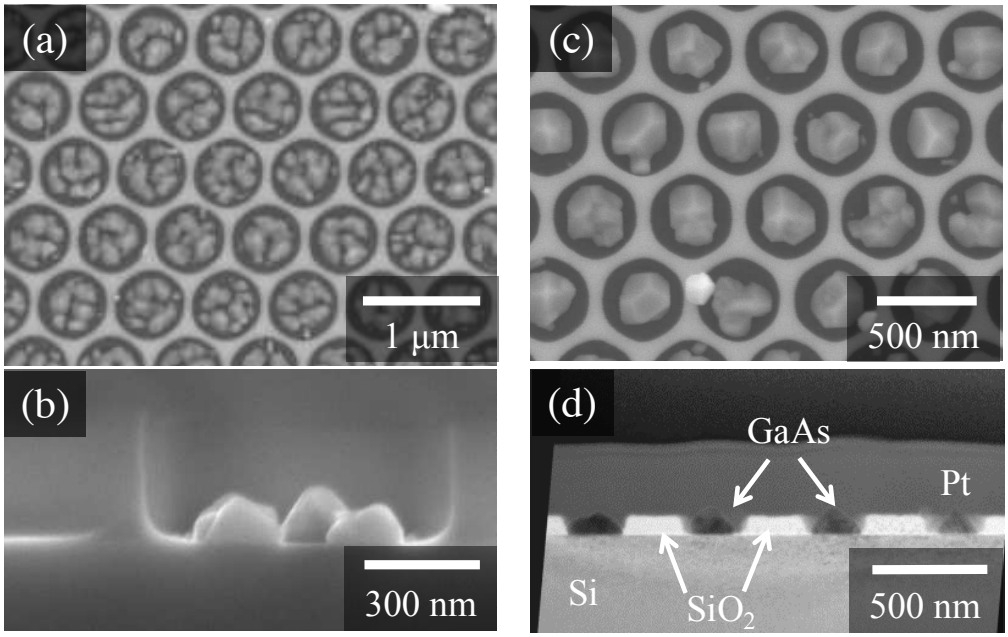

Figure 3-4 Selective area nucleation of GaAs (a) top down view and (b) cross-sectional view of growth within 600 nm wide features (c) top down view of growth within 400 nm wide features; all taken by SEM; (Growth No. PD390) and (d) cross-sectional view by bright field TEM of SAG within 200 nm wide features[by Andrew Norman] ; (Growth No PD399)

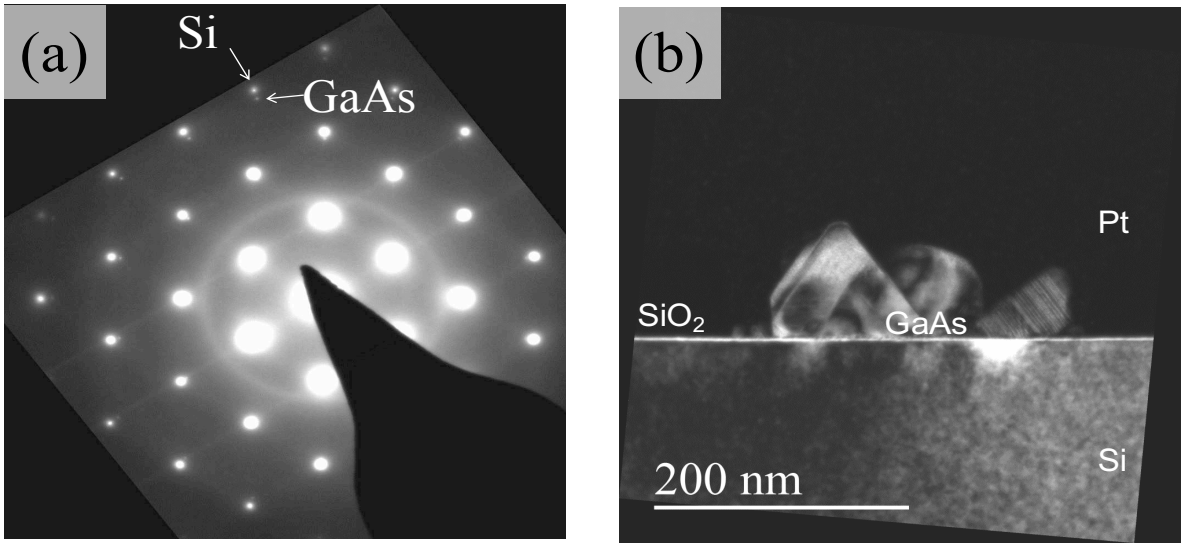

Figure 3-5 Characterization of selective area epitaxial growth on the nanoscale of GaAs on Si by (a) selected area electron diffraction (SAED) and (b) Dark Field [110] cross sectional TEM imaging [by A. Norman]; (Growth No. PD399)

Additionally, the optimization of NIL patterning and GaAs nucleation was also done with line-patterned templates. Although one master provided an NIL template with an aspect ratio (height/width) approaching 1.4, this also posed additional challenges for accomplishing reproducible and uniform pattern transfers due to NIL processing that lacked precise and accurate control of uniform imprint pressures. Despite these challenges, line patterns with aspect ratios greater than 1 were achieved and used to expose areas of Si for the SAG of GaAs (Figure 3-6). However, a deeper investigation of the defect formation and quality of growth after coalescence are discussed and compared to that achieved from dot patterns and planer Si in Section 3.3.

3.3 Coalesced SAG of GaAs

After the selective area nucleation and growth of single crystal GaAs islands, the islands undergo lateral epitaxial overgrowth and coalesce during the last step of the MOCVD growth

process described in Section 3.1. Examples of the resulting thin films of GaAs grown on Si patterned with lines and dots by NIL are shown in Figure 3-7. Before investigating defect formation and relative quality of growth by TEM and XRD, SEM image characterization was used to verify that the template was successfully transferred and that the Si surface was successfully exposed for epitaxial growth.

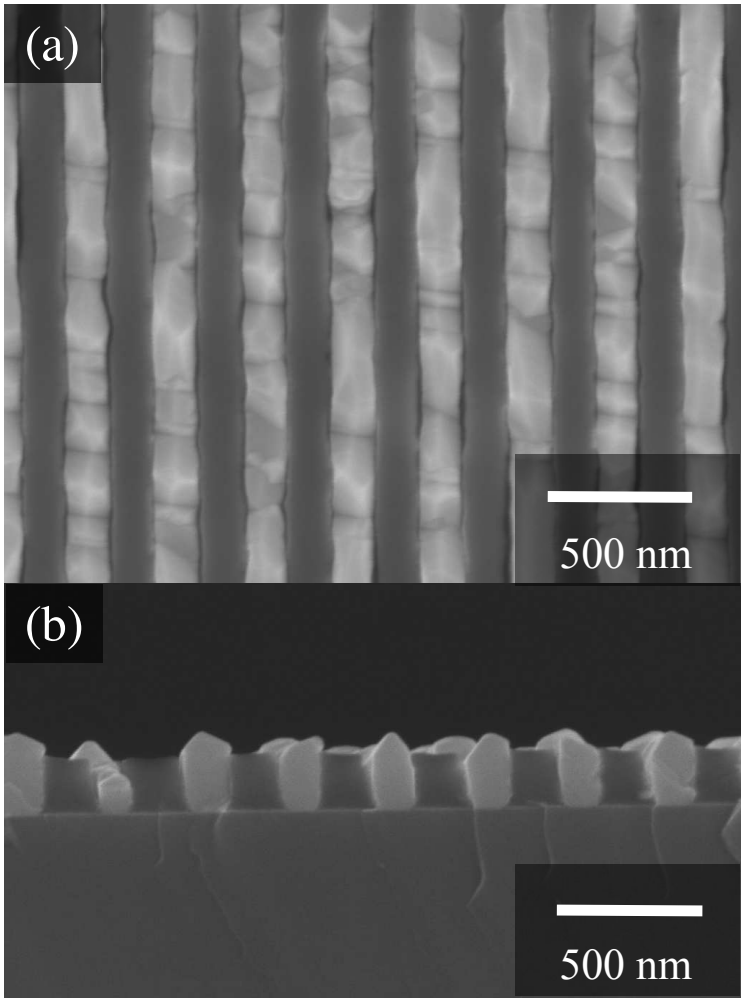

Figure 3-6 SEM image characterization [by E.Warren] of selective area nucleation of GaAs on line pattern template (a) top down view (b) cross-sectional view (Growth No. PD442)

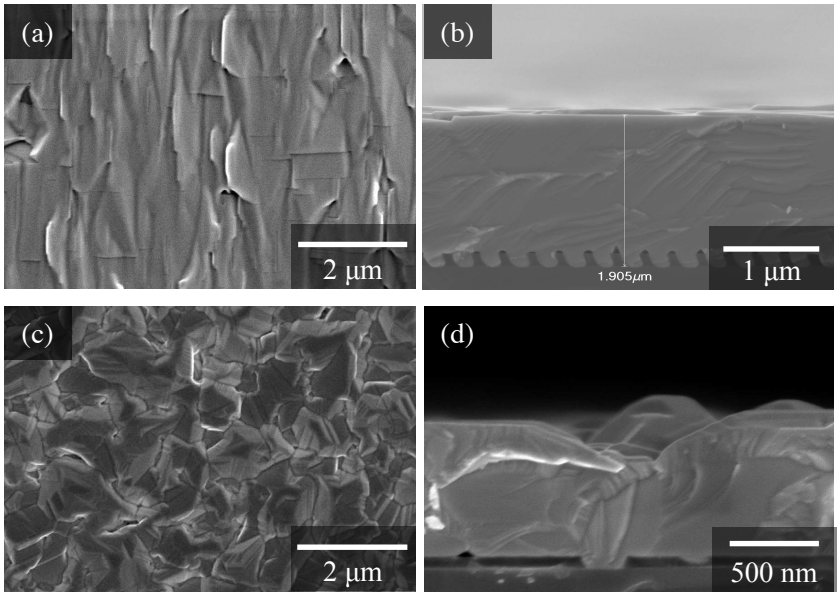

Figure 3-7 SEM characterization of GaAs thin films grown by SAG using 140 nm line template (a) top down view (b) cross-sectional view (Growth No. MP597); SAG using 200 nm dot template (c) top-down view (d) cross-sectional view [by E.Warren] (Growth No. PD427)

3.3.1 XRD & TEM Characterization of Relative Film Quality

After 1.5 to 2 microns of GaAs growth, defect formation and propagation into the coalesced thin films was investigated by cross-sectional TEM. With bright-field cross-sectional TEM imaging of GaAs thin films grown on NIL patterned Si, a high threading dislocation density (TDD) at the patterned interface can be qualitatively observed (Figure 3-8). In addition to threading dislocations, stacking faults in the {111} planes are observed and often accompanied by twinning. Because the NIL and SAG process has not yet been optimized to produce low defect densities, there are simply too many to be counted and quantified by plan-view TEM. Therefore, XRD analysis was employed instead to investigate relative film quality and quantitatively analyze relative dislocation densities for dot pattern geometries, line pattern

geometries, and planar Si by measurement of the full-width-half-maximum (FWHM) of the (004) peak for GaAs.

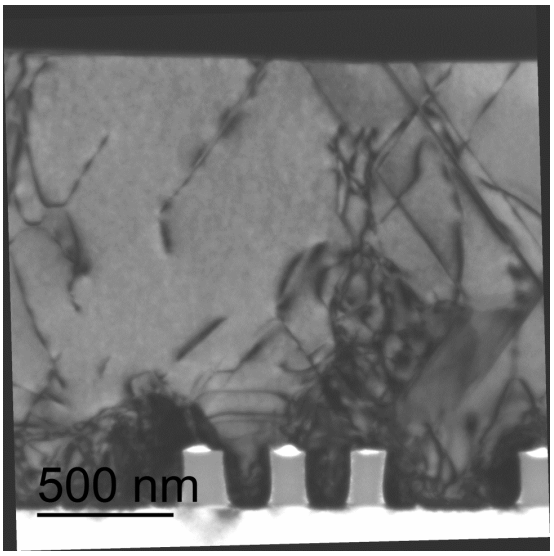

Figure 3-8 Bright field cross-sectional TEM image view in <220> direction (parallel to direction of imprinted lines) reveals high density of threading dislocations at Si interface while line imprint pattern used for SAG was not uniform across interface (Growth No. MP317)

XRD analysis of reciprocal space maps about the (004) peak for GaAs were used to determine relative film quality and dislocation densities across various samples. Selective area growth on patterned SiO_x templates were compared to that grown on planar Si with the same growth parameters. If the NIL patterned SiO_x template was able to reduce dislocation density by ART the during SAG of GaAs, a measureable decrease in peak broadening about the (004) peak for GaAs compared to that grown on planar Si would be expected. From the Ayers method [50], the measured FWHM of the (004) peak is proportional to the dislocation density of a given film. However, Ayers et al. also showed that misfit dislocations are not dominant in the (004) peak broadening, thus this method is measure of dislocation density that is predominately attributed to threading dislocations [51].

The relative film qualities and TDD's after SAG and planar growth were qualitatively deduced and compared by their measured FWHM of (004) peak for GaAs by XRD analysis of reciprocal space maps using a triple axis configuration. The measured FWHM for the (004) peak of SAG of GaAs on SiO_x patterned-Si (exposed 140 nm wide regions of Si along the [110] direction) was found to be almost 2 times larger, around 1050 arcseconds, compared to GaAs grown on planar Si substrates without SAG, around 570 arcseconds. The measured FWHM was not found to decrease for any given patterned substrate, regardless of pattern geometry (lines vs dots) or uniformity.

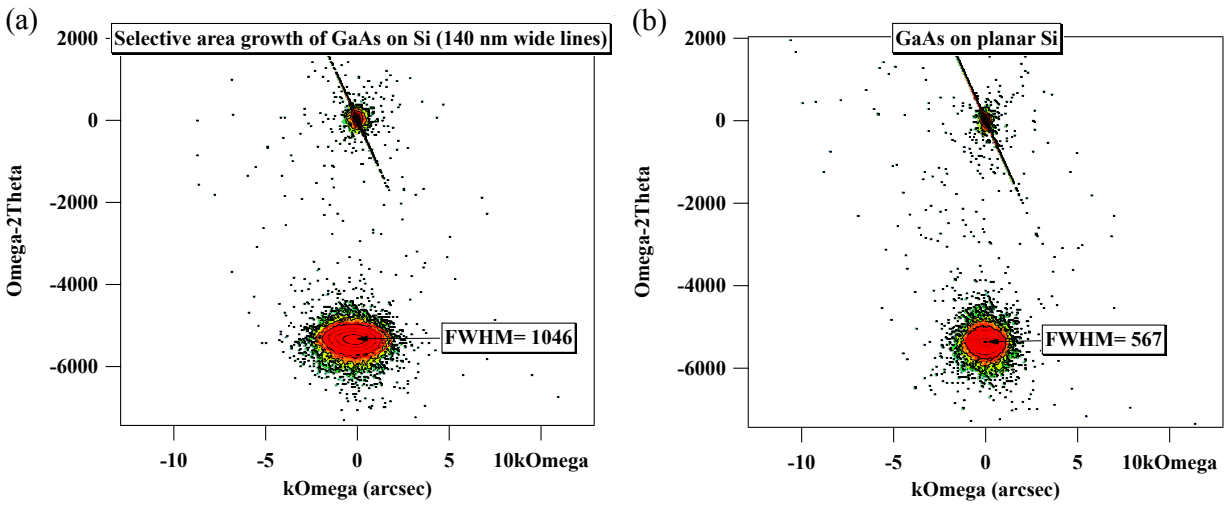

Figure 3-9 Reciprocal Space Map plots the peak broadening about (004) peak and measured FWHM in Omega direction for (a) SAG of thin-film GaAs on Si patterned with lines compared to (b) GaAs grown on planar Si. (Growth No. MP315) [XRD & analysis by Adele Tamboli]

3.4 Summary for SAG of III-V on Si using NIL

Substrate conformal nanoimprint lithography was used to successfully generate nano-patterned SiO_x templates with features sizes from of 140 and 200 nm in the form of lines and holes to expose regions of Si substrates for SAG of GaAs thin films on Si by MOCVD. The

resulting epitaxial nucleation and growth of thin films, characterized by SEM, TEM, and XRD analysis, were found to be worse in terms of the relative defect densities compared to that of GaAs grown on both exact (001) and offcut planar Si, as indicated by peak broadening and the measured FWHM of the (004) peak for GaAs in ω-rocking curve analysis. The pattern geometries predicted to achieve reduced defect densities by SAG and ART have not yet been realized primarily due to a limited availability of Si mater pattern geometries which do not provide aspect ratios (height:width) above 1.4 or sub-100 nm wide regions of Si to be exposed. We conclude that in order for NIL patterned Si substrates to be used for SAG and aspect ratio trapping of the TDs that form along the {111} planes, the NIL template fabrication process will require a number of improvements; to start, the variety of Si master pattern geometries used in the NIL process should be expanded to contain features that are decreased in nucleation size below 100 nm as well as increased aspect ratios greater than 1.4.

Although aspect ratio trapping has been shown to reduce threading dislocation densities by allowing some threading dislocations, which travel along the {111} family of planes, to annihilate at the sidewalls of the template [23], [24], it is noteworthy to highlight that some dislocations can still be formed above the plane of the patterned template during lateral epitaxial overgrowth. Threading dislocations can form when three regions of growth coalesce during lateral epitaxial overgrowth without exact crystallographic registry. Realizing reduced defect densities of III-V heteroepitaxy on Si by SAG will require additional understanding of dislocation generation, propagation, mobility, and interactions to inform the continued optimization of template geometries and orientations that should be used.

CHAPTER 4

CONCLUSIONS & FUTURE WORK

The process development of soft-nanoimprint lithography was successfully employed to achieve selective area growth of GaAs on Si substrates. While reduced dislocation densities by SAG on NIL-patterned Si substrates compared to planar Si were not yet realized, we recognize a wide variety of improvements to the NIL process would be required in order to achieve the predicted defect density reduction through aspect ratio trapping of threading dislocations which travel along {111} family of planes. In order to replicate densely packed sub-100 nm feature sizes with high aspect ratio features above 1.4, the template fabrication process by soft-NIL will require further process development to enable improved reproducibility, pattern transfer fidelity without loss of aspect ratio, and control over crystallographic alignment with respect to the Si substrate. With such improvements, soft-NIL can pave economical pathways for further investigation of SAG on the nanoscale to realize reduced defect densities and successful integration of high-quality III-V semiconductors on Si.

The integration of III-V semiconductors on low-cost silicon (Si) substrates is a promising path to reduce the cost of building high efficiency photovoltaic (PV) devices. Realizing reduced threading dislocation densities by ART would help reduce potential recombination centers and degradation of minority carrier lifetime of III-V top-cell absorbers [17]. However, despite methods to improve quality of III-V growth on Si, degradation of minority carrier lifetime has been observed in Si substrates due to exposure to the MOCVD and MBE III-V growth environments [52]–[54]. In a tandem solar cell architecture with an active Si bottom cell, we must also pay attention to whether this approach maintains high minority carrier lifetimes within

the Si substrate throughout the various processing steps from template fabrication by NIL to III-V growth by MOCVD.

With a slow pulse of light to generate minority carriers in a substrate, Sinton Instruments are able to determine the recombination lifetime within a substrate using the Eddy-current method to sense changes in the conductivity due to changes in the carrier density over time; this is referred to as the quasi-steady-state photoconductive decay, or "Sinton lifetime", technique [55]. Preliminary studies using the Sinton lifetime technique indicate the patterned interface fabricated by NIL and transferred into passivating layers such as Al_2O_3 or silicon nitrides on Si could reduce surface recombination and prevent fast-diffusing contaminants from reducing minority carrier lifetime in the Si sub-cell [25]. However, there have not been in-depth studies on the effects that a partially protected Si:III-V interface may have on the Si minority carrier lifetime throughout MOCVD processing. Over the course of optimizing III-V integration onto Si by SAG using NIL, surface passivation quality of nano-patterned templates on Si and its bulk lifetime throughout fabrication steps should be studied further using the Sinton lifetime technique. The passivation effects on Si using a SAG template will be a key parameter in determining the viability of this approach to realizing the next low-cost generation of high performance III-V based devices on Si.

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